Complete 16-Bit CCD/CIS Signal Processor

AD80066

FEATURES

16-bit, 24 MSPS analog-to-digital converter (ADC)
4-channel operation up to 24 MHz (6 MHz/channel)
3-channel operation up to 24 MHz (8 MHz/channel)
Selectable input range: 3 V or 1.5 V peak-to-peak
Input clamp circuitry
Correlated double sampling
1×~6× programmable gain
±300 mV programmable offset
Internal voltage reference
Multiplexed byte-wide output
Optional single-byte output mode
3-wire serial digital interface
3 V/5 V digital I/O compatibility
Power dissipation: 490 mW at 24 MHz operation
Reduced power mode and sleep mode available
28-lead SSOP package

APPLICATIONS

Flatbed document scanners
Film scanners
Digital color copiers
Multifunction peripherals

GENERAL DESCRIPTION

The AD80066 is a complete analog signal processor for imaging applications. It features a 4-channel architecture designed to sample and condition the outputs of linear charged coupled device (CCD) or contact image sensor (CIS) arrays. Each channel consists of an input clamp, correlated double sampler (CDS), offset digital-to-analog converter (DAC), and programmable gain amplifier (PGA), multiplexed to a high performance 16-bit ADC. For maximum flexibility, the AD80066 can be configured as a 4-channel, 3-channel, 2-channel, or 1-channel device.

The CDS amplifiers can be disabled for use with sensors that do not require CDS, such as CIS and CMOS sensors.

The 16-bit digital output is multiplexed into an 8-bit output word, which is accessed using two read cycles. There is an optional single-byte output mode. The internal registers are programmed through a 3-wire serial interface and enable adjustment of the gain, offset, and operating mode. The AD80066 operates from a 5 V power supply, typically consumes 490 mW of power, and is packaged in a 28-lead SSOP.

FUNCTIONAL BLOCK DIAGRAM

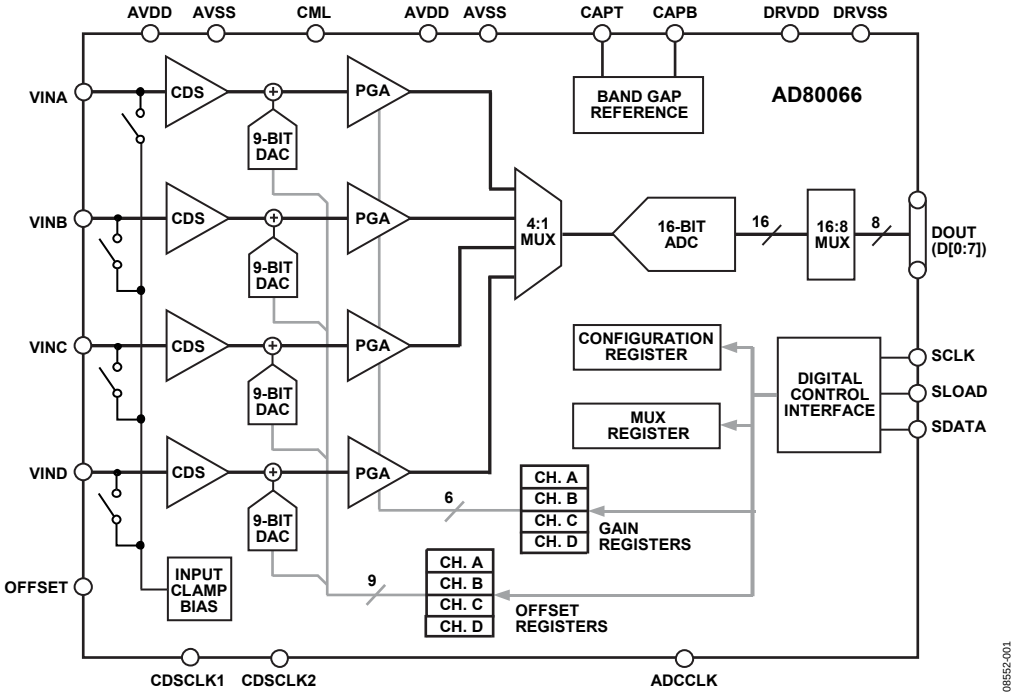


Figure 1.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 2
Specifications ... 3
  Analog Specifications ... 3
  Digital Specifications ... 4
  Timing Specifications ... 5
Absolute Maximum Ratings ... 9
  Thermal Resistance ... 9
  ESD Caution ... 9
Pin Configuration and Function Descriptions ... 10
Typical Performance Characteristics ... 11
Terminology ... 12
Theory of Operation ... 13
  4-Channel CDS Mode ... 13
  4-Channel SHA Mode ... 13
  1-Channel CDS Mode ... 13
  1-Channel SHA Mode ... 13
Internal Register Map ... 14
Internal Register Details ... 15
  Configuration Register ... 15
  Mux Register ... 15
  PGA Gain Registers ... 15
  Offset Registers ... 15
Circuit Operation ... 17
  Analog Inputs—CDS Mode ... 17
  External Input Coupling Capacitors ... 17
  Analog Inputs—SHA Mode ... 18
  Programmable Gain Amplifiers (PGA) ... 18
Applications Information ... 19
  Circuit and Layout Recommendations ... 19
Outline Dimensions ... 20
  Ordering Guide ... 20

REVISION HISTORY

4/10—Revision A: Initial Version

SPECIFICATIONS

ANALOG SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS mode, f_{ADCCLK} = 24 MHz, $f_{CDSCLK1}$ = $f_{CDSCLK2}$ = 6 MHz, PGA gain = 1, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
MAXIMUM CONVERSION RATE				
4-Channel Mode with CDS		24		MSPS
3-Channel Mode with CDS		24		MSPS
2-Channel Mode with CDS		24		MSPS
1-Channel Mode with CDS		12		MSPS
ACCURACY (ENTIRE SIGNAL PATH)				
ADC Resolution		16		Bits
Integral Nonlinearity (INL)		+20/−5		LSB
Differential Nonlinearity (DNL)		±0.5		LSB
No Missing Codes		Guaranteed		
ANALOG INPUTS				
Input Signal Range[1]		1.5/3.0		V p-p
Allowable Reset Transient[1]		2.0		V
Input Limits[2]	AVSS − 0.3		AVDD + 0.3	V
Input Capacitance		10		pF
Input Bias Current		10		nA
AMPLIFIERS				
PGA Gain Range	1		5.9	V/V
PGA Gain Resolution[2]		64		Steps
PGA Gain Monotonicity		Guaranteed		
Programmable Offset Range	−305		+295	mV
Programmable Offset Resolution		512		Steps
Programmable Offset Monotonicity		Guaranteed		
NOISE AND CROSSTALK				
Total Output Noise at PGA Minimum		9.5		LSB rms
Total Output Noise at PGA Maximum		35		LSB rms
Channel-to-Channel Crosstalk				
@ 24 MSPS		70		dB
@ 12 MSPS		90		dB
POWER SUPPLY REJECTION				
AVDD = 5 V ± 0.25 V		0.1		% FSR
VOLTAGE REFERENCE (T_A = 25°C)				
CAPT − CAPB		0.75		V
TEMPERATURE RANGE				
Operating	0		70	°C
Storage	−65		+150	°C
POWER SUPPLIES				
AVDD	4.5	5.0	5.25	V
DRVDD	3.0	3.3	5.25	V
OPERATING CURRENT				
AVDD		95		mA
DRVDD		4		mA
Power-Down Mode Current		300		µA

Parameter	Min	Typ	Max	Unit
POWER DISSIPATION				
4-Channel Mode at 24 MHz		490		mW
1-Channel Mode at 12 MHz		300		mW
4-Channel Mode at 8 MHz, Slow Power Mode[3]		165		mW

[1] The linear input signal range is up to 3 V p-p when the CCD reference level is clamped to 3 V by the AD80066 input clamp (see Figure 2).
[2] The PGA gain is approximately linear-in-dB but varies nonlinearly with register code (see the Programmable Gain Amplifiers (PGA) section for more information).
[3] Measured with Bit D1 of the configuration register set high for 8 MHz, low power operation.

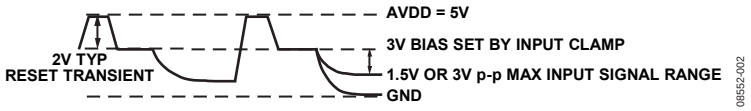


Figure 2. Input Signal with the CCD Reference Level Clamped to 3 V

DIGITAL SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V, CDS mode, f_{ADCCLK} = 24 MHz, $f_{CDSCLK1} = f_{CDSCLK2}$ = 6 MHz, C_L = 10 pF, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.0			V
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (DRVDD = 5 V)					
High Level Output Voltage (I_{OH} = 2 mA)	V_{OH}	4.5			V
Low Level Output Voltage (I_{OL} = 2 mA)	V_{OL}			0.5	V
LOGIC OUTPUTS (DRVDD = 3 V)					
High Level Output Voltage (I_{OH} = 2 mA)	V_{OH}	2.5			V
Low Level Output Voltage (I_{OL} = 2 mA)	V_{OL}			0.5	V

TIMING SPECIFICATIONS

T_{MIN} to T_{MAX}, AVDD = 5 V, DRVDD = 5 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK PARAMETERS					
4-Channel Pixel Rate	t_{PRA}	166			ns
1-Channel Pixel Rate	t_{PRB}	83			ns
ADCCLK Pulse Width	t_{ADCCLK}	20			ns
CDSCLK1 Pulse Width	t_{C1}	15			ns
CDSCLK2 Pulse Width	t_{C2}	15			ns
CDSCLK1 Falling[1] to CDSCLK2 Rising	t_{C1C2}	0			ns
ADCCLK Falling to CDSCLK2 Rising	t_{ADC2}	0			ns
CDSCLK2 Rising to ADCCLK Rising	t_{C2ADR}	5			ns
CDSCLK2 Falling[1] to ADCCLK Falling	t_{C2ADF}	20			ns
CDSCLK2 Falling[1] to CDSCLK1 Rising	t_{C2C1}	5			ns
Aperture Delay for CDS Clocks	t_{AD}		2		ns
SERIAL INTERFACE					
Maximum SCLK Frequency, Write Operation	f_{SCLK}	50			MHz
Maximum SCLK Frequency, Read Operation	f_{SCLK}	25			MHz
SLOAD to SCLK Setup Time	t_{LS}	5			ns
SCLK to SLOAD Hold Time	t_{LH}	5			ns
SDATA to SCLK Rising Setup Time	t_{DS}	2			ns
SCLK Rising to SDATA Hold Time	t_{DH}	2			ns
SCLK Falling to SDATA Valid	t_{RDV}	10			ns
DATA OUTPUT					
Output Delay	t_{OD}		8		ns
Latency (Pipeline Delay)			3 (fixed)		Cycles

[1] CDSCLKx falling edges should not occur within the first 10 ns following an ADCCLK edge.

Timing Diagrams

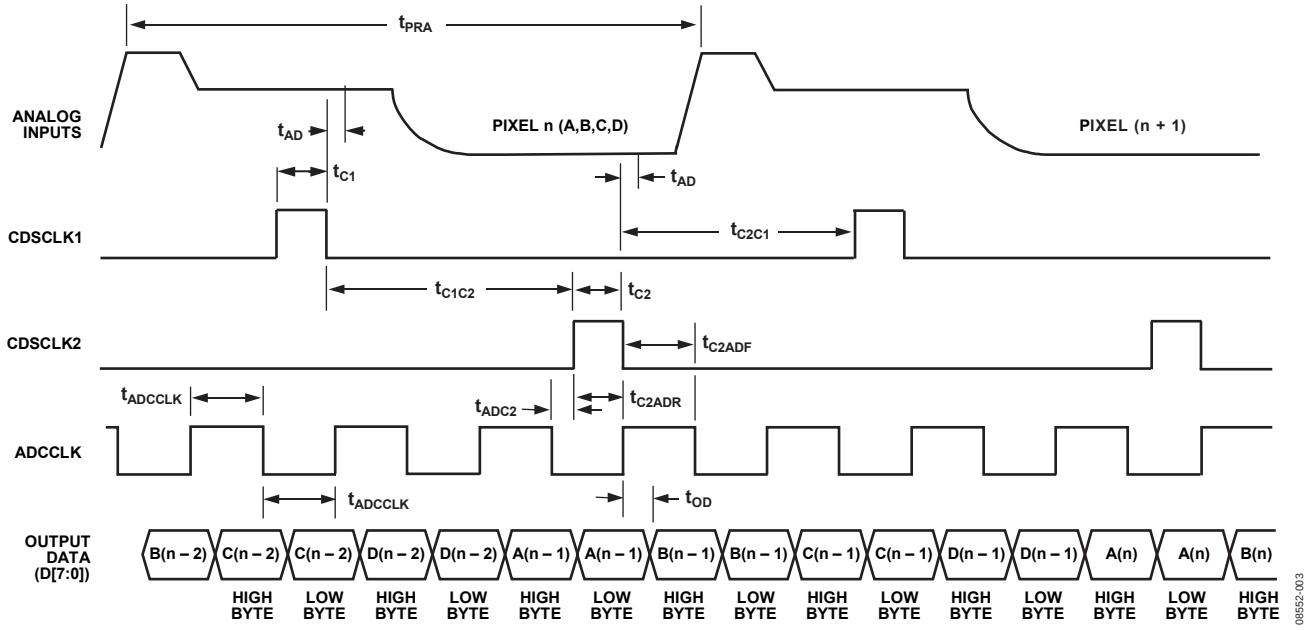


Figure 3. 4-Channel CDS Mode Timing

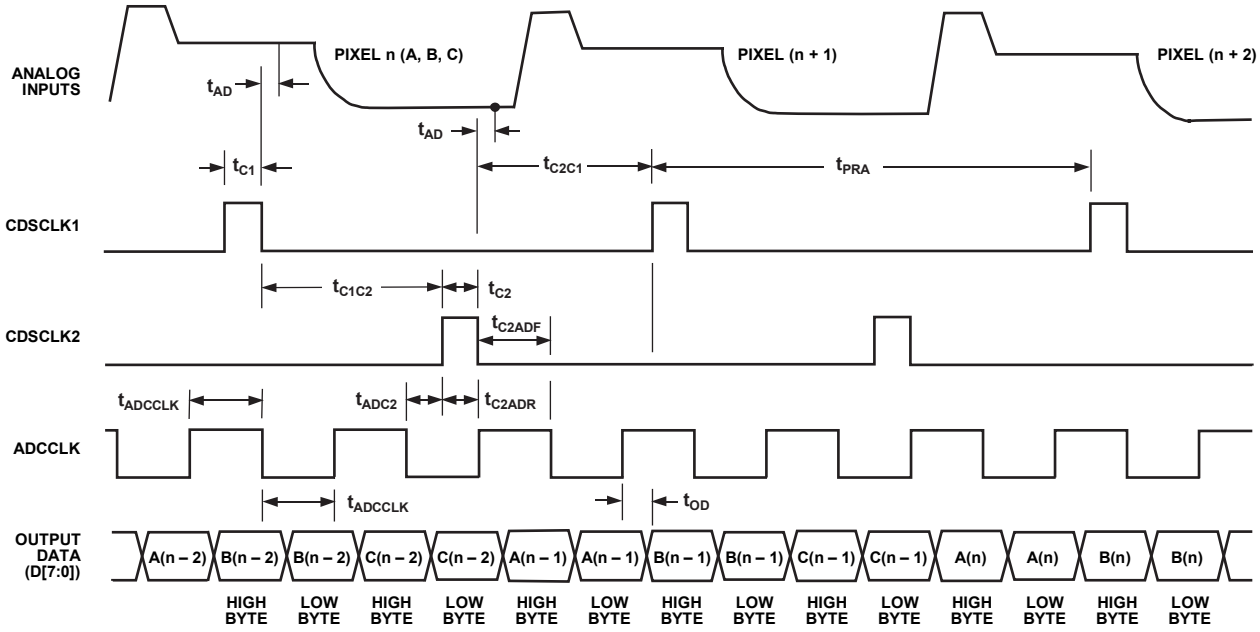


Figure 4. 3-Channel CDS Mode Timing

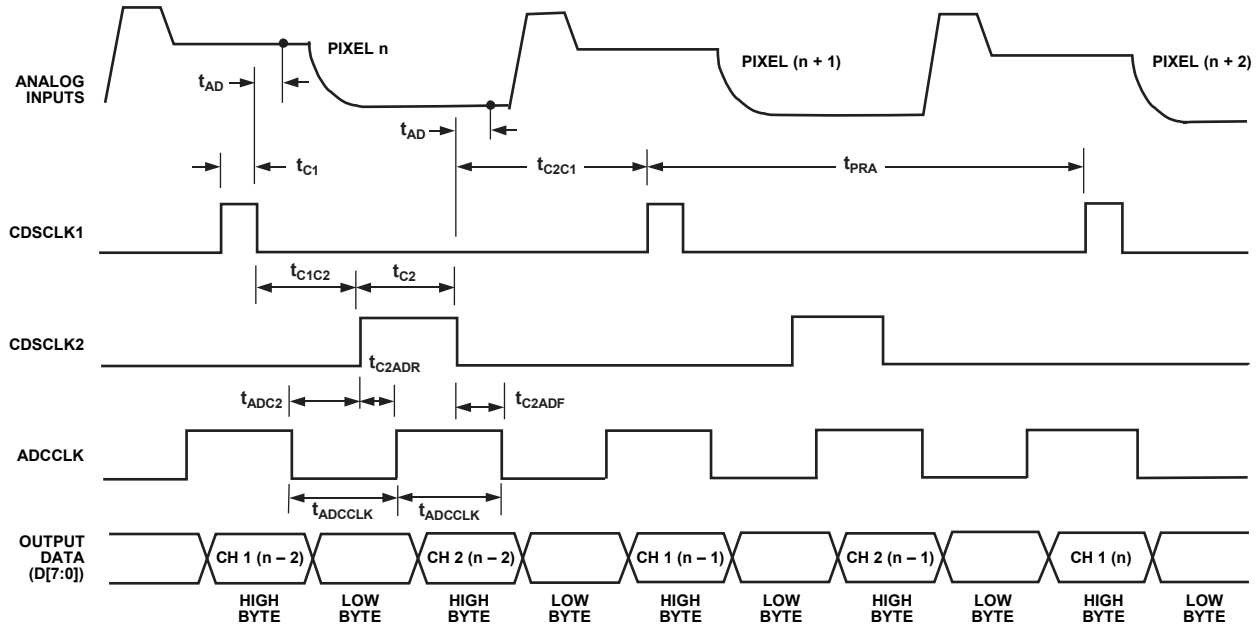
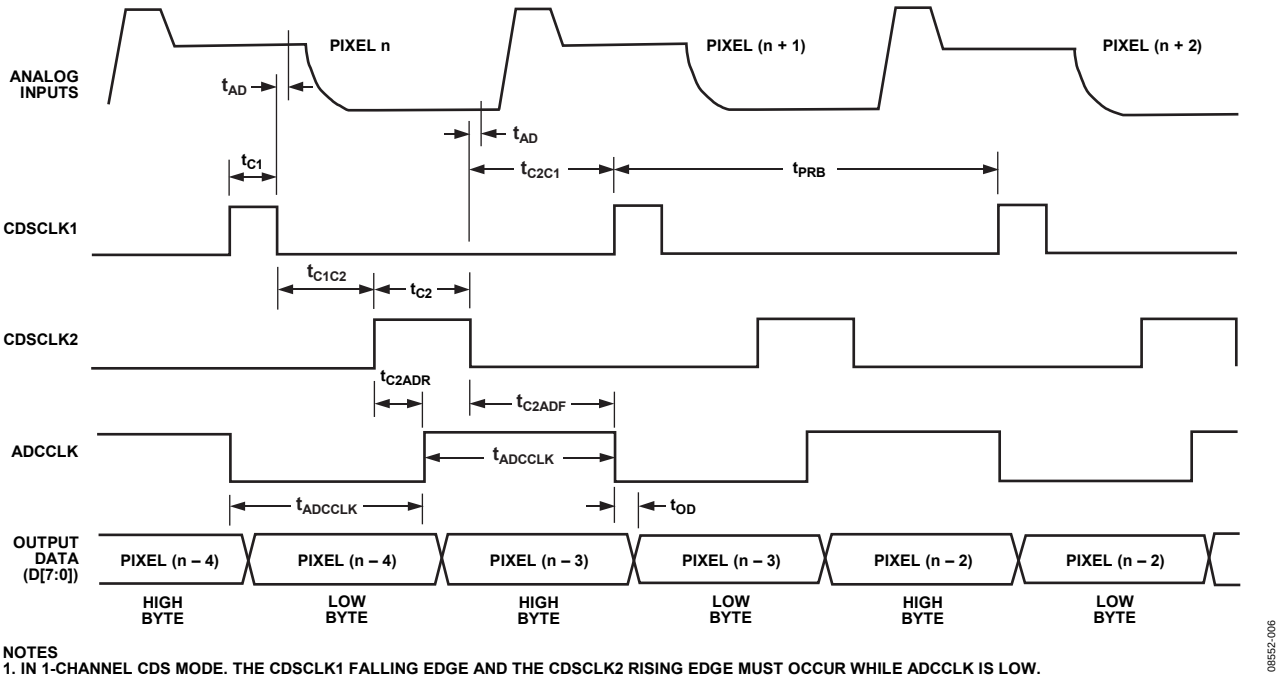


Figure 5. 2-Channel CDS Mode Timing



NOTES
1. IN 1-CHANNEL CDS MODE. THE CDSCLK1 FALLING EDGE AND THE CDSCLK2 RISING EDGE MUST OCCUR WHILE ADCCLK IS LOW.

Figure 6. 1-Channel CDS Mode Timing

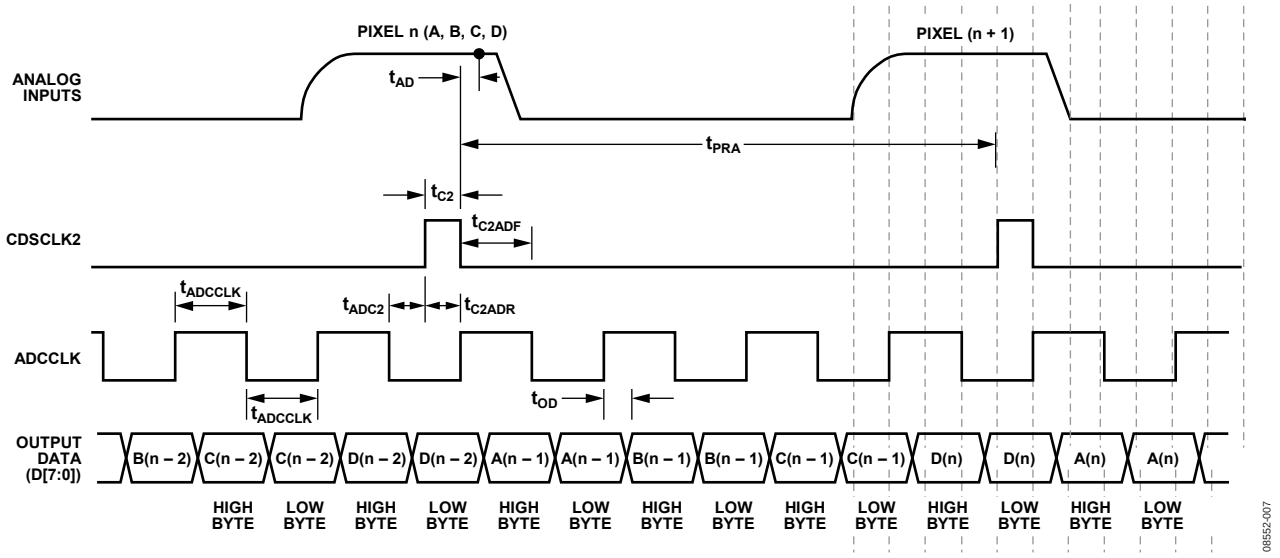


Figure 7. 4-Channel SHA Mode Timing

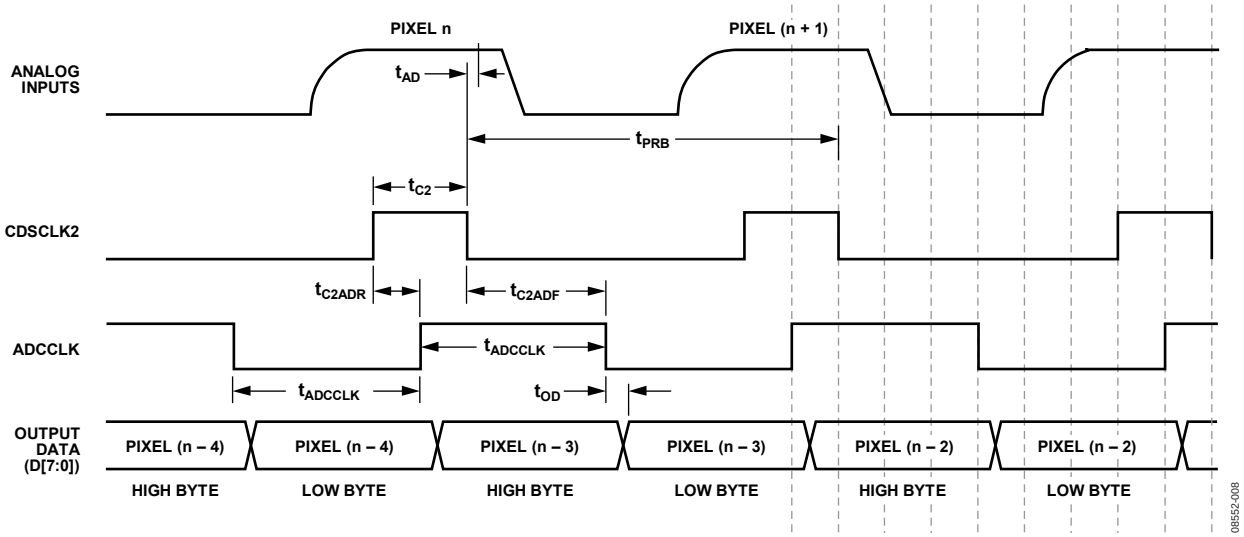


Figure 8. 1-Channel SHA Mode Timing

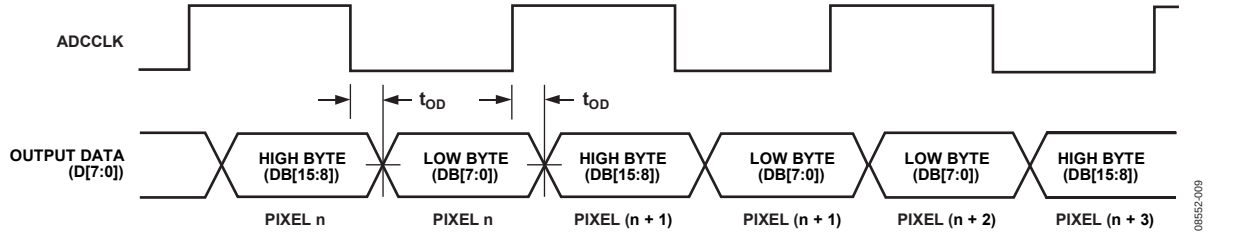


Figure 9. Digital Output Data Timing

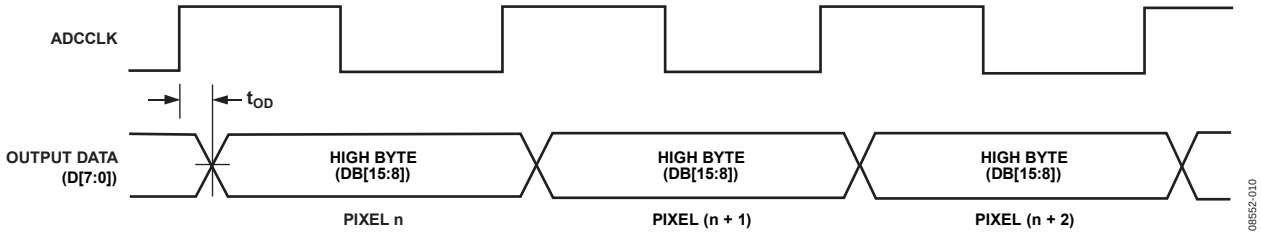


Figure 10. Single-Byte Mode Digital Output Data Timing

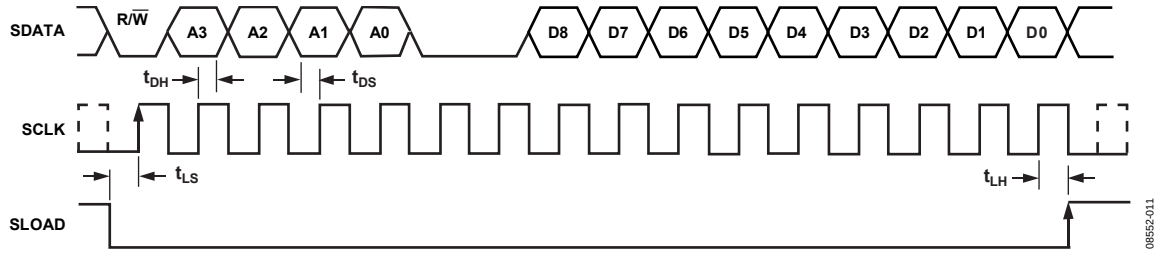


Figure 11. Serial Write Operation Timing

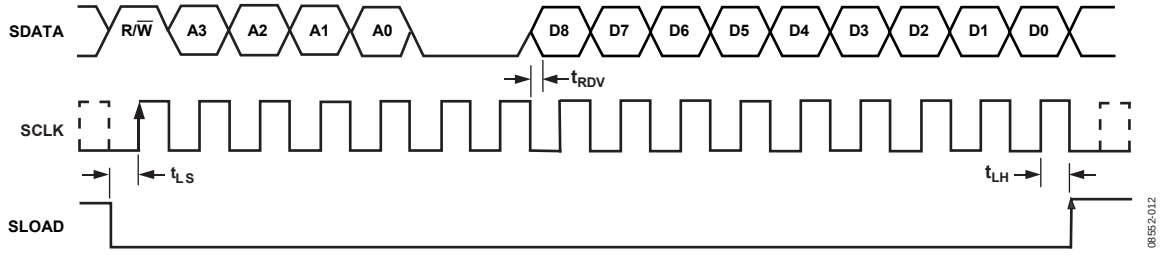


Figure 12. Serial Read Operation Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	With Respect To	Rating
VINx, CAPT, CAPB	AVSS	−0.3 V to AVDD + 0.3 V
Digital Inputs	AVSS	−0.3 V to AVDD + 0.3 V
SDATA	DRVSS	−0.3 V to DRVDD
AVDD	AVSS	−0.5 V to +6.5 V
DRVDD	DRVSS	−0.5 V to +6.5 V
AVSS	DRVSS	−0.3 V to +0.3 V
Digital Outputs (D[7:0])	DRVSS	−0.3 V to DRVDD + 0.3 V
Temperature		
Junction		150°C
Storage		−65°C to +150°C
Lead (10 sec)		300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead, 5.3 mm SSOP	109	39	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

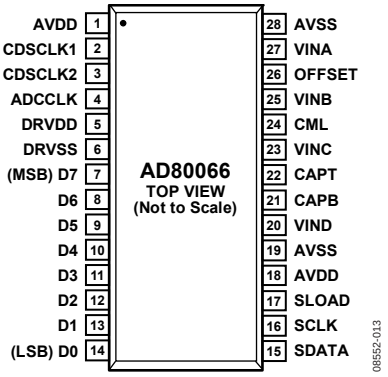


Figure 13. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AVDD	P	5 V Analog Supply.
2	CDSCLK1	DI	CDS Reference Level Sampling Clock.
3	CDSCLK2	DI	CDS Data Level Sampling Clock.
4	ADCCLK	DI	ADC Sampling Clock.
5	DRVDD	P	Digital Output Driver Supply (3 V or 5 V).
6	DRVSS	P	Digital Output Driver Ground.
7	D7 (MSB)	DO	Data Output MSB. ADC DB15 high byte; ADC DB7 low byte.
8	D6	DO	Data Output. ADC DB14 high byte; ADC DB6 low byte.
9	D5	DO	Data Output. ADC DB13 high byte; ADC DB5 low byte.
10	D4	DO	Data Output. ADC DB12 high byte; ADC DB4 low byte.
11	D3	DO	Data Output. ADC DB11 high byte; ADC DB3 low byte.
12	D2	DO	Data Output. ADC DB10 high byte; ADC DB2 low byte.
13	D1	DO	Data Output. ADC DB9 high byte; ADC DB1 low byte.
14	D0 (LSB)	DO	Data Output LSB. ADC DB8 high byte; ADC DB0 low byte.
15	SDATA	DI/DO	Serial Interface Data Input/Output.
16	SCLK	DI	Serial Interface Clock Input.
17	SLOAD	DI	Serial Interface Load Pulse.
18	AVDD	P	5 V Analog Supply.
19	AVSS	P	Analog Ground.
20	VIND	AI	Analog Input, D Channel.
21	CAPB	AO	ADC Bottom Reference Voltage Decoupling.
22	CAPT	AO	ADC Top Reference Voltage Decoupling.
23	VINC	AI	Analog Input, C Channel.
24	CML	AO	Internal Bias Level Decoupling.
25	VINB	AI	Analog Input, B Channel.
26	OFFSET	AO	Clamp Bias Level Decoupling.
27	VINA	AI	Analog Input, A Channel.
28	AVSS	P	Analog Ground.

[1] AI = analog input, AO = analog output, DI = digital input, DO = digital output, and P = power.

TYPICAL PERFORMANCE CHARACTERISTICS

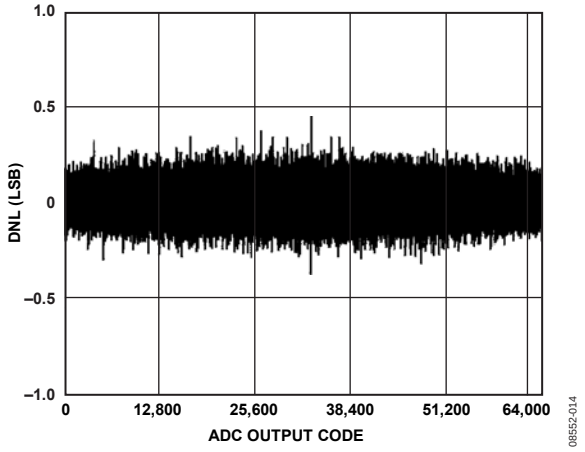


Figure 14. Typical DNL Performance

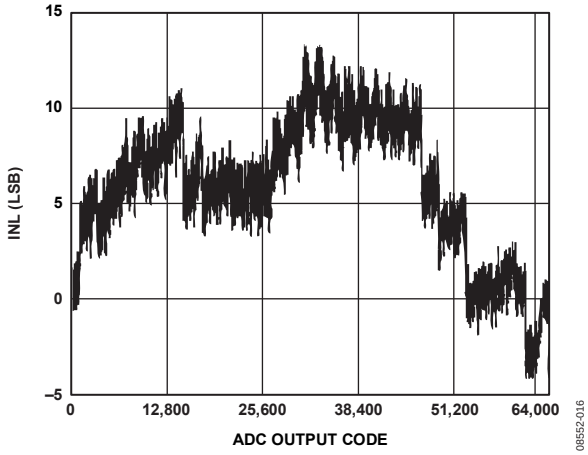


Figure 16. Typical INL Performance

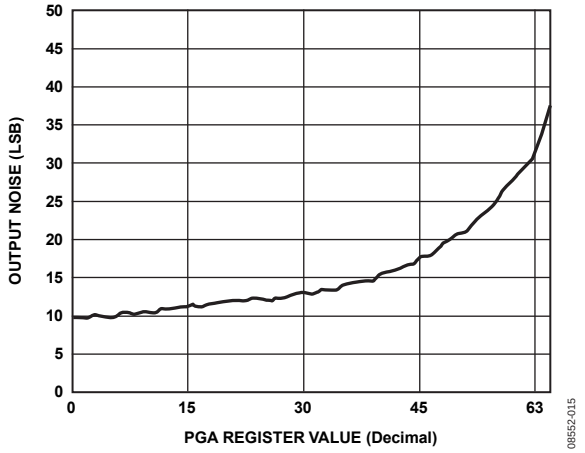


Figure 15. Output Noise vs. PGA Gain

TERMINOLOGY

Integral Nonlinearity (INL)
Integral nonlinearity error refers to the deviation of each individual code from a line drawn from zero scale through positive full scale. The point used as zero scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value; therefore, every code must have a finite width. No missing codes guaranteed to 16-bit resolution indicates that all 65,536 codes must be present over all operating ranges.

Offset Error
The first ADC code transition should occur at a level ½ LSB above the nominal zero-scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

Gain Error
The last code transition should occur for an analog value 1½ LSB below the nominal full-scale voltage. Gain error is the deviation of the actual difference between the first and last code transitions and the ideal difference between the first and last code transitions.

Input-Referred Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and converted to an equivalent voltage, using the relationship 1 LSB = 1.5 V/65,536 = 23 μV. The noise is then referred to the input of the AD80066 by dividing by the PGA gain.

Channel-to-Channel Crosstalk
In an ideal 3-channel system, the signal in one channel does not influence the signal level of another channel. The channel-to-channel crosstalk specification is a measure of the change that occurs in one channel as the other two channels are varied. In the AD80066, one channel is grounded and the other two channels are exercised with full-scale input signals. The change in the output codes from the first channel is measured and compared with the result when all three channels are grounded. The difference is the channel-to-channel crosstalk, stated in LSB.

Aperture Delay
The aperture delay is the delay that occurs from when a sampling edge is applied to the AD80066 until the actual sample of the input signal is held. Both CDSCLK1 and CDSCLK2 sample the input signal during the transition from high to low; therefore, the aperture delay is measured from each falling edge of the clock to when the internal sample is taken.

Power Supply Rejection
The power supply rejection specifies the maximum full-scale change that occurs from the initial value when the supplies are varied over the specified limits.

THEORY OF OPERATION

The AD80066 can be operated in several different modes, including 4-channel CDS mode, 4-channel SHA mode, 1-channel CDS mode, and 1-channel SHA mode. Each mode is selected by programming the configuration register through the serial interface. For more information on CDS or SHA mode operation, see the Circuit Operation section.

4-CHANNEL CDS MODE

In 4-channel CDS mode, the AD80066 simultaneously samples the A, B, C, and D input voltages from the CCD outputs. The sampling points for each CDS are controlled by CDSCLK1 and CDSCLK2 (see Figure 17 and Figure 18). The CDSCLK1 falling edge samples the reference level of the CCD waveform, and the CDSCLK2 falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD reference level and the data level. The output voltage of each CDS amplifier is then level-shifted by an offset DAC. The voltages are scaled by the four PGAs before being multiplexed through the 16-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The offset and gain values for the A, B, C, and D channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the mux register.

Timing for this mode is shown in Figure 3. The falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK. However, this is not required to satisfy the minimum timing constraints. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is 3 ADCCLK cycles.

4-CHANNEL SHA MODE

In 4-channel SHA mode, the AD80066 simultaneously samples the A, B, C, and D input voltages. The sampling point is controlled by CDSCLK2. The falling edge of CDSCLK2 samples the input waveforms on each channel. The output voltages from the three SHAs are modified by the offset DACs and then scaled by the four PGAs. The outputs of the PGAs are then multiplexed through the 16-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin (see Figure 19). With the OFFSET pin grounded, a 0 V input corresponds to the zero-scale output of the ADC. The OFFSET pin can also be used as a coarse offset adjustment pin. A voltage applied to this pin is subtracted from the voltages applied to the A, B, C, and D inputs in the first amplifier stage of the AD80066. The input clamp is disabled in this mode. For more information, see the Analog Inputs—SHA Mode section.

The offset and gain values for the A, B, C, and D channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the mux register.

Timing for this mode is shown in Figure 7. The CDSCLK1 pin should be grounded in this mode. Although not required, the falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by t_{ADC2}. The output data latency is 3 ADCCLK cycles.

1-CHANNEL CDS MODE

The 1-channel CDS mode operates in the same way as the 4-channel CDS mode, except the multiplexer remains fixed. Only the channel specified in the mux register is processed.

Timing for this mode is shown in Figure 6.

1-CHANNEL SHA MODE

The 1-channel SHA mode operates in the same way as the 4-channel SHA mode, except the multiplexer remains fixed. Only the channel specified in the mux register is processed.

Timing for this mode is shown in Figure 8. The CDSCLK1 pin should be grounded in this mode of operation.

INTERNAL REGISTER MAP

Table 7. Internal Register Map

	Address				Data Bits								
Register Name	**A3**	**A2**	**A1**	**A0**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Configuration	0	0	0	0	0	0	0	VREF	2/1 byte	CDS on	Input range	Fast/slow	Power on
Mux	0	0	0	1	0	0	0	0	Ch. order	Ch. A	Ch. B	Ch. C	Ch. D
Gain A	0	0	1	0	0	0	0	MSB					LSB
Gain B	0	0	1	1	0	0	0	MSB					LSB
Gain C	0	1	0	0	0	0	0	MSB					LSB
Gain D	0	1	0	1	0	0	0	MSB					LSB
Offset A	0	1	1	0	MSB								LSB
Offset B	0	1	1	1	MSB								LSB
Offset C	1	0	0	0	MSB								LSB
Offset D	1	0	0	1	MSB								LSB

INTERNAL REGISTER DETAILS

CONFIGURATION REGISTER

The configuration register controls the AD80066 operating mode and bias levels. The D8, D7, and D6 bits should always be set low. Bit D2 sets the full-scale input voltage range of the AD80066 ADC to either 3 V (high) or 1.5 V (low). Bit D5 controls the internal voltage reference. If the AD80066 internal voltage reference is used, this bit is set low. Setting Bit D5 high disables the internal voltage reference, allowing an external voltage reference to be used. Setting Bit D3 low enables the CDS mode of operation and setting this bit high enables the SHA mode of operation. If Bit D4 is set high, the 16-bit ADC output is multiplexed into two bytes. The most significant byte is output on the ADCCLK rising edge, and the least significant byte is output on the ADCCLK falling edge (see Figure 10). If Bit D1 is set high, the AD80066 is configured for slow operation (8 MHz) to reduce power consumption. Bit D0 controls the power-down mode. Setting Bit D0 low places the AD80066 into a very low power sleep mode. All register contents are retained while the AD80066 is in the power-down state.

MUX REGISTER

The mux register controls the sampling channel order in the AD80066. The D8, D7, D6, and D5 bits should always be set low. Bit D4 is used when operating in 4-channel mode. Setting Bit D4 low sequences the multiplexer to sample the A channel first, and then the B, C, and D channels. When in this mode, the CDSCLK2 pulse always resets the multiplexer to sample the A channel first. When Bit D4 is set high, the channel order is reversed to D, C, B, and A. The CDSCLK2 pulse always resets the multiplexer to sample the D channel first. Bits D[3:0] are used when operating in 1-channel mode. Bit D3 is set high to sample the A channel. Bit D2 is set high to sample the B channel. Bit D1 is set high to sample the C channel. Bit D0 is set high to sample the D channel. The multiplexer remains stationary in 1-channel mode.

PGA GAIN REGISTERS

There are four PGA registers for individually programming the gain for the A, B, C, and D channels. The D8, D7, and D6 bits in each register must be set low, and the D5 through D0 bits control the gain range in 64 increments. See Figure 22 for the PGA gain vs. the PGA register value. The coding for the PGA registers is straight binary, with a word of all 0s corresponding to the minimum gain setting (1×) and a word of all 1s corresponding to the maximum gain setting (5.9×).

OFFSET REGISTERS

There are four offset registers for individually programming the offset in the A, B, C, and D channels. The D8 through D0 bits control the offset range from −300 mV to +300 mV in 512 increments. The coding for the offset registers is sign magnitude, with D8 as the sign bit. Table 11 shows the offset range as a function of the D8 through D0 bits.

Table 8. Configuration Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 0	Internal voltage reference	2/1 byte output	CDS operation	Input range	Fast/slow	Power mode
			1 = disabled	1 = one byte	1 = SHA mode	1 = 3 V	1 = 8 MHz	1 = on (normal)
			0 = enabled[1]	0 = two bytes[1]	0 = CDS mode[1]	0 = 1.5 V[1]	0 = 24 MHz[1]	0 = off[1]

[1] Power-on default.

Table 9. Mux Register Settings

D8	D7	D6	D5	D4	D3	D2	D1	D0
Set to 0	Set to 0	Set to 0	Set to 0	Mux order	Channel A	Channel B	Channel C	Channel D
				1 = D, C, B, A	1 = channel used	1 = channel used	1 = channel used	1 = channel used
				0 = A, B, C, D[1]	0 = not used[1]	0 = not used[1]	0 = not used[1]	0 = not used[1]

[1] Power-on default.

Table 10. PGA Gain Register Settings

D8[1]	D7[1]	D6[1]	(MSB) D5	D4	D3	D2	D1	(LSB) D0	Gain (V/V)	Gain (dB)
0	0	0	0	0	0	0	0	0[2]	1.0	0.0
0	0	0	0	0	0	0	0	1	1.013	0.12
…	…	…	…	…	…	…	…	…	…	…
0	0	0	1	1	1	1	1	0	5.56	14.9
0	0	0	1	1	1	1	1	1	5.9	15.56

[1] Must be set to 0.
[2] Power-on default.

Table 11. Offset Register Settings

(MSB) D8	D7	D6	D5	D4	D3	D2	D1	(LSB) D0	Offset (mV)
0	0	0	0	0	0	0	0	0[1]	0
0	0	0	0	0	0	0	0	1	+1.2
…	…	…	…	…	…	…	…	…	…
0	1	1	1	1	1	1	1	1	+300
1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1	−1.2
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1	−300

[1] Power-on default value.

CIRCUIT OPERATION

ANALOG INPUTS—CDS MODE

Figure 17 shows the analog input configuration for the CDS mode of operation. Figure 18 shows the internal timing for the sampling switches. The CCD reference level is sampled when CDSCLK1 transitions from high to low, opening S1. The CCD data level is sampled when CDSCLK2 transitions from high to low, opening S2. S3 is then closed, generating a differential output voltage that represents the difference between the two sampled levels.

The input clamp is controlled by CDSCLK1. When CDSCLK1 is high, S4 closes and the internal bias voltage is connected to the analog input. The bias voltage charges the external 0.1 µF input capacitor, level-shifting the CCD signal into the input common-mode range of the AD80066. The time constant of the input clamp is determined by the internal 5 kΩ resistance and the external 0.1 µF input capacitance.

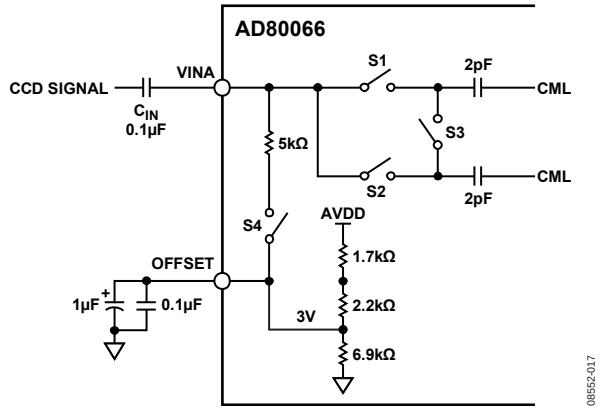


Figure 17. CDS Mode Input Configuration (All Four Channels Are Identical)

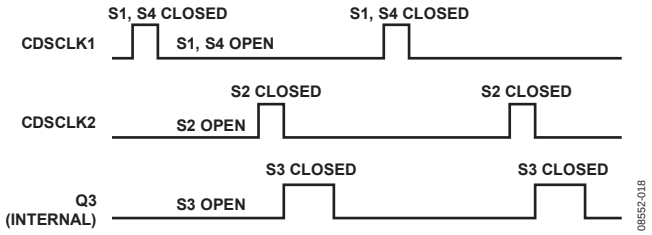


Figure 18. CDS Mode Internal Switch Timing

EXTERNAL INPUT COUPLING CAPACITORS

The recommended value for the input coupling capacitors is 0.1 µF. Although it is possible to use a smaller capacitor, this larger value is preferable for several reasons:

- Signal attenuation: The input coupling capacitor creates a capacitive divider using the input capacitance from an integrated CMOS circuit, which, in turn, attenuates the CCD signal level. CIN should be large relative to the 10 pF input capacitance of the IC in order to minimize this effect.
- Linearity: Some of the input capacitance of a CMOS IC is junction capacitance, which varies nonlinearly with applied voltage. If the input coupling capacitor is too small, the attenuation of the CCD signal varies nonlinearly with signal level. This degrades the system linearity performance.
- Sampling errors: The internal 2 pF sampling capacitors retain a memory of the previously sampled pixel. There is a charge redistribution error between CIN and the internal sample capacitors for larger pixel-to-pixel voltage swings. As the value of CIN is reduced, the resulting error in the sampled voltage increases. With a CIN value of 0.1 µF, the charge redistribution error is less than 1 LSB for a full-scale, pixel-to-pixel voltage swing.

ANALOG INPUTS—SHA MODE

Figure 19 shows the analog input configuration for the SHA mode of operation. Figure 20 shows the internal timing for the sampling switches. The input signal is sampled when CDSCLK2 transitions from high to low, opening S1. The voltage on the OFFSET pin is also sampled on the falling edge of CDSCLK2, when S2 opens. S3 is then closed, generating a differential output voltage that represents the difference between the sampled input voltage and the OFFSET voltage. The input clamp is disabled during SHA mode operation.

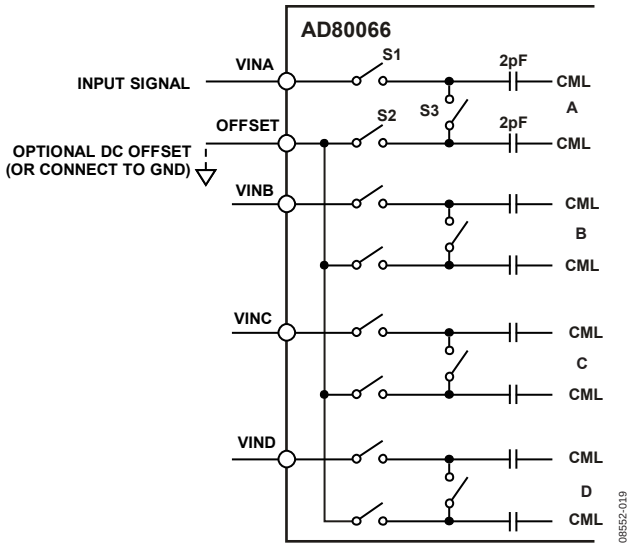


Figure 19. SHA Mode Input Configuration (All Four Channels Are Identical)

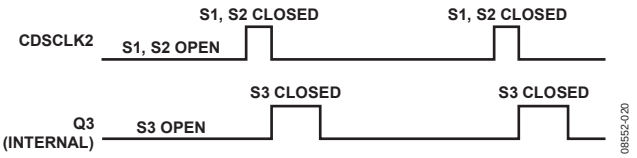


Figure 20. SHA Mode Internal Switch Timing

Figure 21 shows how the OFFSET pin can be used in a CIS application for coarse offset adjustment. Many CIS signals have dc offsets ranging from several hundred millivolts to more than 1 V. By connecting the appropriate dc voltage to the OFFSET pin, the large dc offset is removed from the CIS signal. Then, the signal can be scaled using the PGA to maximize the dynamic range of the ADC.

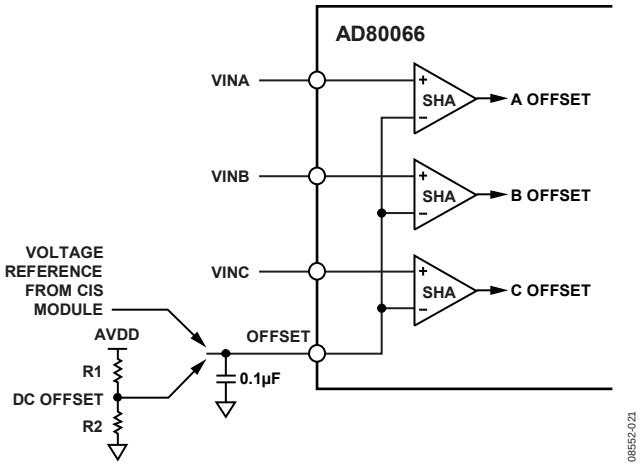


Figure 21. SHA Mode Used with External DC Offset

PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The AD80066 uses one PGA for each channel. Each PGA has a gain range from 1× (0 dB) to 5.8× (15.5 dB), adjustable in 64 steps. Figure 22 shows the PGA gain as a function of the PGA register value. Although the gain curve is approximately linear-in-dB, the gain in V/V varies nonlinearly with register code, following the equation

$$Gain = \frac{5.9}{1 + 4.9\left[\frac{63 - G}{63}\right]}$$

where G is the decimal value of the gain register contents and varies from 0 to 63.

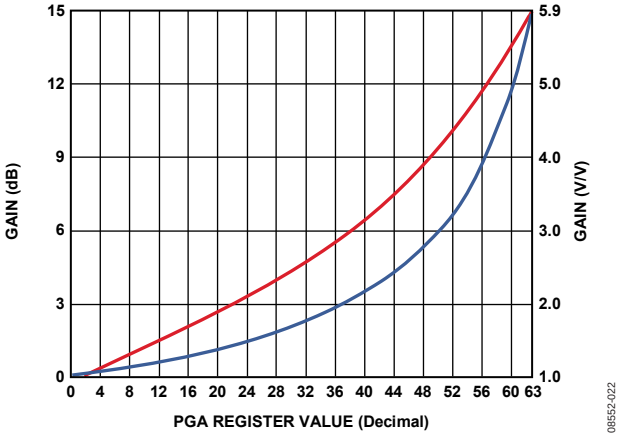


Figure 22. PGA Gain Transfer Function

APPLICATIONS INFORMATION

CIRCUIT AND LAYOUT RECOMMENDATIONS

Figure 23 shows the recommended circuit configuration for 4-channel CDS mode operation. The recommended input coupling capacitor value is 0.1 µF (see the Analog Inputs—CDS Mode section). A single ground plane is recommended for the AD80066. A separate power supply can be used for DRVDD, the digital driver supply, but this supply pin should still be decoupled to the same ground plane as the rest of the AD80066. The loading of the digital outputs should be minimized, either by using short traces to the digital ASIC or by using external digital buffers. To minimize the effect of digital transients during major output code transitions, the falling edge of CDSCLK2 should occur coincident with or before the rising edge of ADCCLK (see Figure 3 through Figure 8 for timing). All 0.1 µF decoupling capacitors should be located as close as possible to the AD80066 pins. When operating in 1-channel mode, the unused analog inputs should be grounded.

Figure 24 shows the recommended circuit configuration for 4-channel SHA mode. All of the previously explained considerations also apply to this configuration, except that the analog input signals are directly connected to the AD80066 without the use of coupling capacitors. Before connecting the signals, the analog input signals must be dc-biased between 0 V and 1.5 V or 3 V (see the Analog Inputs—SHA Mode section).

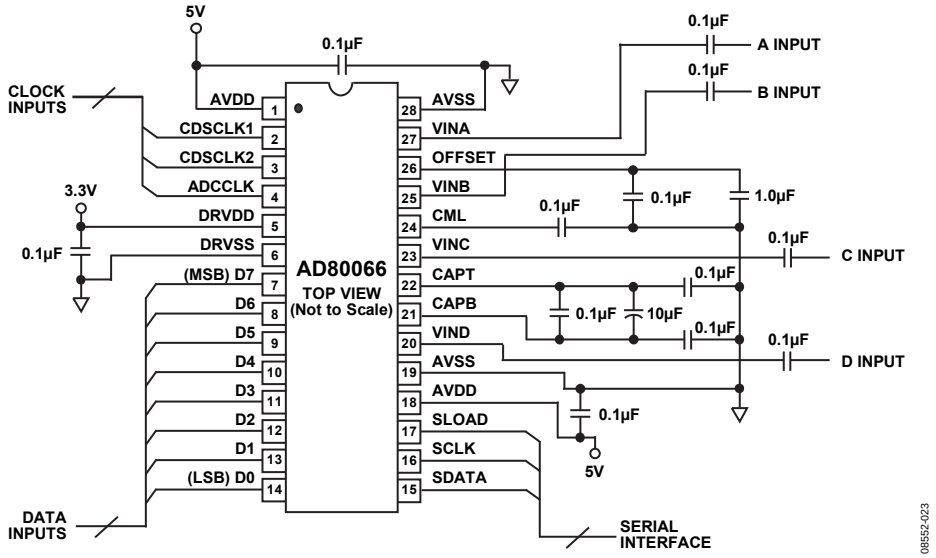


Figure 23. Recommended Circuit Configuration, 4-Channel CDS Mode

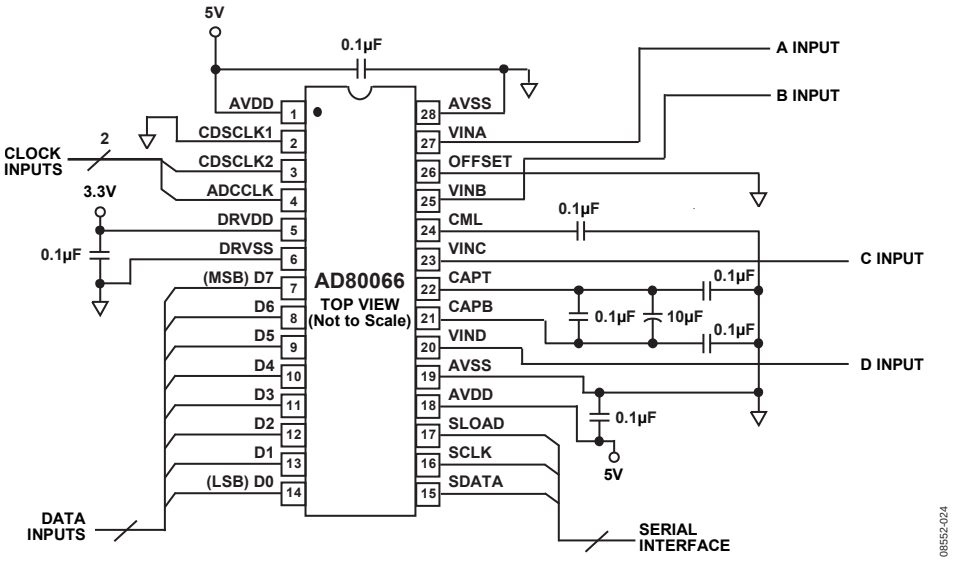
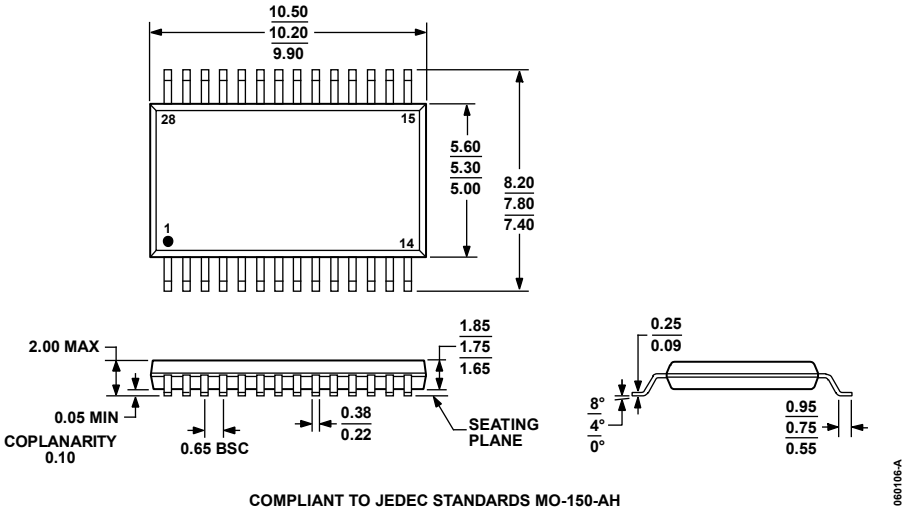


Figure 24. Recommended Circuit Configuration, 4-Channel SHA Mode (Analog Inputs Sampled with Respect to Ground)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AH

Figure 25. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD80066KRSZ	0°C to 70°C	28-Lead SSOP	RS-28
AD80066KRSZRL	0°C to 70°C	28-Lead SSOP	RS-28

[1] Z = RoHS Compliant Part.

D08552-0-4/10(A)