*Designer's™ Data Sheet*

# TMOS E-FET ™

# High Energy Power FET

## N–Channel Enhancement–Mode Silicon Gate

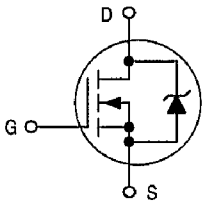
**MTP3N60E**

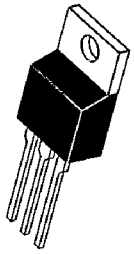
Motorola Preferred Device

**TMOS POWER FET**
**3.0 AMPERES**
**600 VOLTS**
**$R_{DS(on)}$ = 2.2 OHMS**

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



**CASE 221A–06, Style 5**
**TO-220AB**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 600 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 600 | Vdc |
| Gate–Source Voltage — Continuous<br>— Non–repetitive | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current — Continuous<br>— Pulsed | $I_D$<br>$I_{DM}$ | 3.0<br>14 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |

**UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS** ($T_J$ < 150°C)

| | | | |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche Energy — $T_J$ = 25°C<br>— $T_J$ = 100°C<br>Repetitive Pulse Drain–to–Source Avalanche Energy | $W_{DSR(1)}$<br><br>$W_{DSR(2)}$ | 290<br>46<br>7.5 | mJ |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance — Junction to Case<br>— Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

(1) $V_{DD}$ = 50 V, $I_D$ = 3.0 A
(2) Pulse Width and frequency is limited by $T_J$(max) and thermal response

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

**REV 1**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 250 µAdc) | $V_{(BR)DSS}$ | 600 | — | — | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 600 V, $V_{GS}$ = 0) | $I_{DSS}$ | — | — | 0.25 | mAdc |
| ($V_{DS}$ = 480 V, $V_{GS}$ = 0, $T_J$ = 125°C) | | — | — | 1.0 | |
| Gate–Body Leakage Current — Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | $I_{GSSF}$ | — | — | 100 | nAdc |
| Gate–Body Leakage Current — Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | $I_{GSSR}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS*** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc) | $V_{GS(th)}$ | 2.0 | — | 4.0 | Vdc |
| ($T_J$ = 125°C) | | 1.5 | — | 3.5 | |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 A) | $R_{DS(on)}$ | — | 2.1 | 2.2 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 3.0 A) | $V_{DS(on)}$ | — | — | 9.0 | Vdc |
| ($I_D$ = 1.5 A, $T_J$ = 100°C) | | — | — | 7.5 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 1.5 A) | $g_{FS}$ | 1.5 | — | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | $C_{iss}$ | — | 770 | — | pF |
| Output Capacitance ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | — | 105 | — | |
| Transfer Capacitance | $C_{rss}$ | — | 19 | — | |
| **SWITCHING CHARACTERISTICS*** | | | | | |
| Turn–On Delay Time | $t_{d(on)}$ | — | 23 | — | ns |
| Rise Time | $t_r$ | — | 34 | — | |
| Turn–Off Delay Time ($V_{DD}$ = 300 V, $I_D$ ≈ 3.0 A, $R_L$ = 100 Ω, $R_G$ = 12 Ω, $V_{GS(on)}$ = 10 V) | $t_{d(off)}$ | — | 58 | — | |
| Fall Time | $t_f$ | — | 35 | — | |
| Total Gate Charge | $Q_g$ | — | 28 | 31 | nC |
| Gate–Source Charge ($V_{DS}$ = 420 V, $I_D$ = 3.0 A, $V_{GS}$ = 10 V) | $Q_{gs}$ | — | 5.0 | — | |
| Gate–Drain Charge | $Q_{gd}$ | — | 17 | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage | $V_{SD}$ | — | — | 1.4 | Vdc |
| Forward Turn–On Time ($I_S$ = 3.0 A, di/dt = 100 A/µs) | $t_{on}$ | — | ** | — | ns |
| Reverse Recovery Time | $t_{rr}$ | — | 400 | — | |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) | $L_d$ | — | 3.5 | — | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | — | 4.5 | — | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | $L_s$ | — | 7.5 | — | |

* Pulse Test: Pulse Width = 300 µs, Duty Cycle ≤ 2.0%.
** Limited by circuit inductance.

## TYPICAL ELECTRICAL CHARACTERISTICS

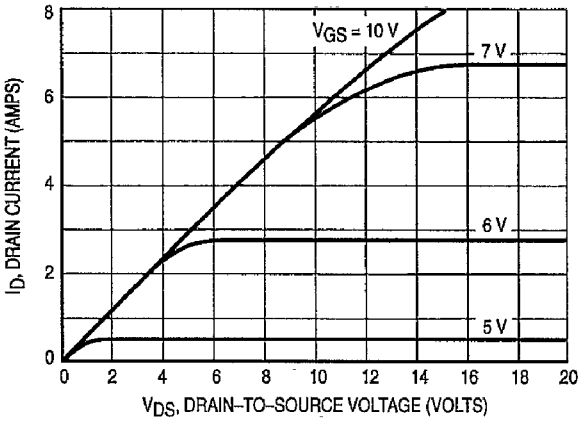



**Figure 1. On–Region Characteristics**

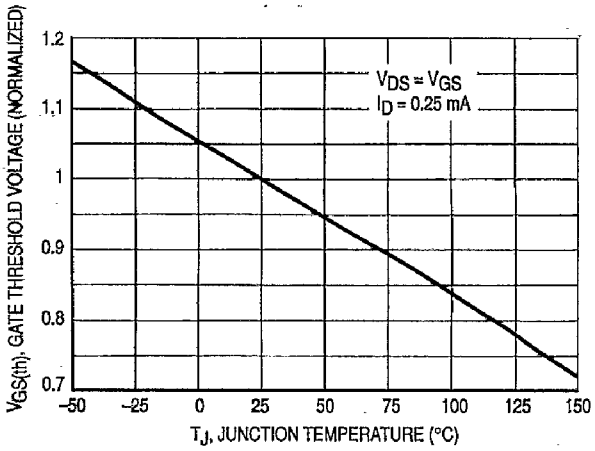



**Figure 2. Gate–Threshold Voltage Variation With Temperature**

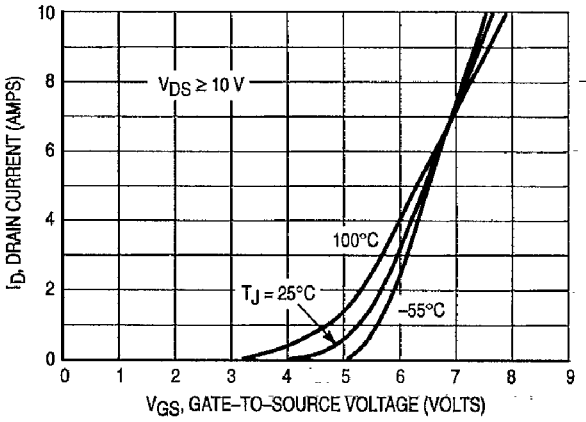



**Figure 3. Transfer Characteristics**

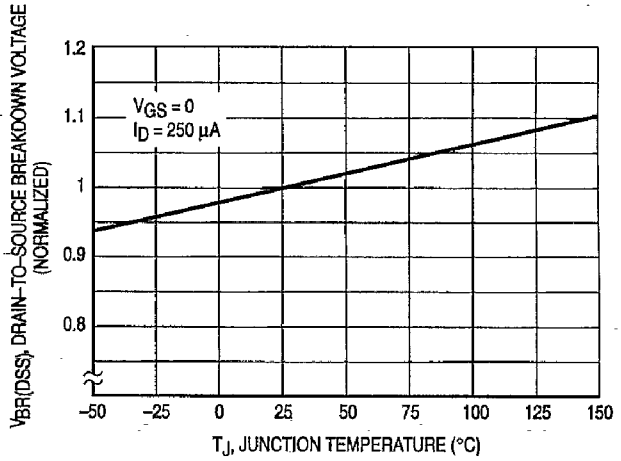



**Figure 4. Breakdown Voltage Variation With Temperature**

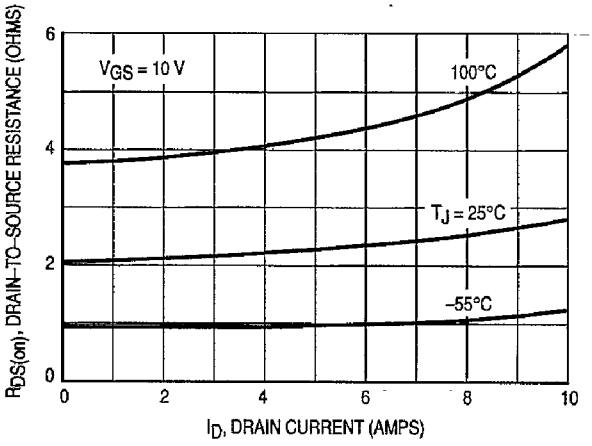



**Figure 5. On–Resistance versus Drain Current**

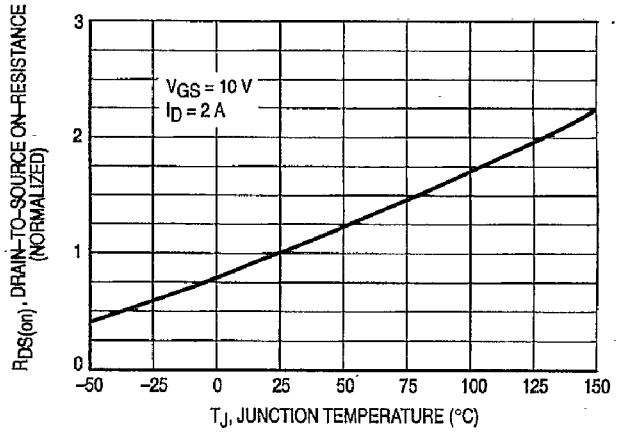



**Figure 6. On–Resistance Variation With Temperature**

## SAFE OPERATING AREA INFORMATION

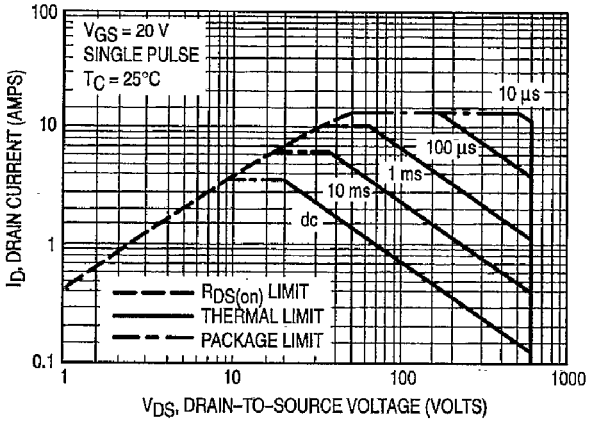



**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

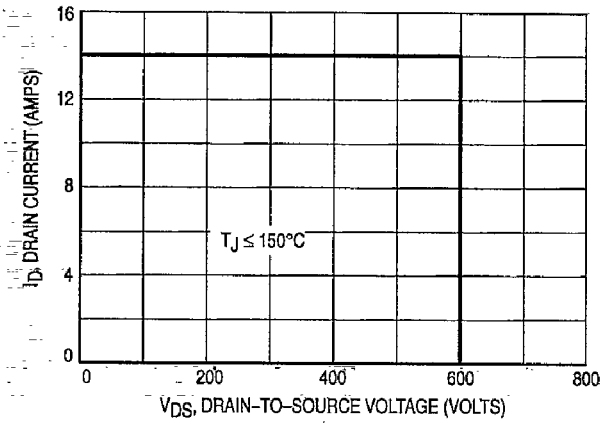



**Figure 8. Maximum Rated Switching Safe Operating Area**

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

### SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

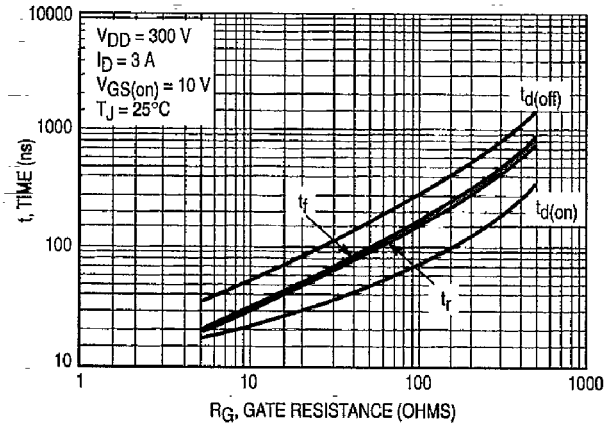



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

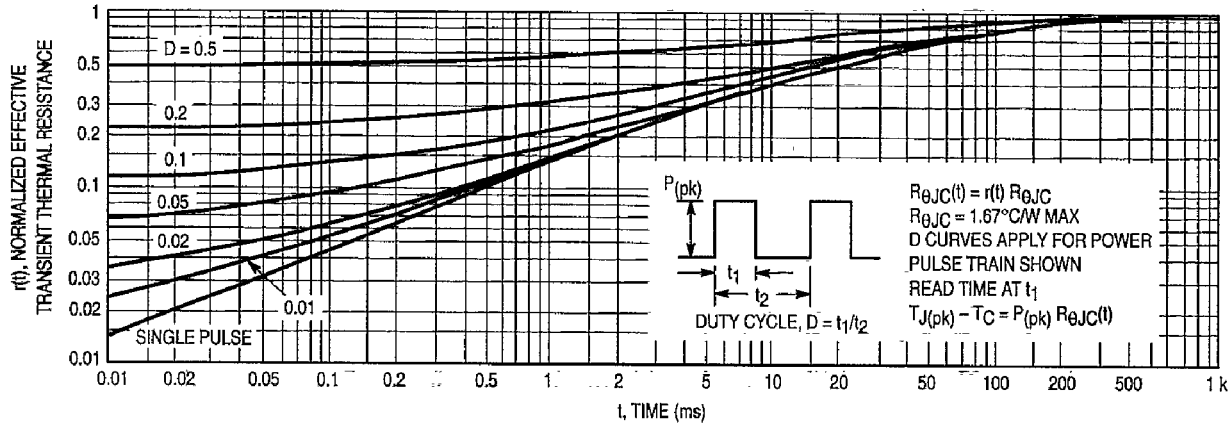



**Figure 10. Thermal Response**

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of $I_{FM}$ and peak $V_R$ for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval $t_{frr}$ is the speed of the commutation cycle. Device stresses increase with commutation speed, so $t_{frr}$ is specified with a minimum value. Faster commutation speeds require an appropriate derating of $I_{FM}$, peak $V_R$ or both. Ultimately, $t_{frr}$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{rr}$ as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; $I_{FM}$ is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$ is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as $I_S$ decays from $I_{RM}$ to zero.

$R_{GS}$ should be minimized during commutation. $T_J$ has only a second order effect on CSOA.

Stray inductances, $L_i$ in Motorola's test circuit are assumed to be practical minimums.

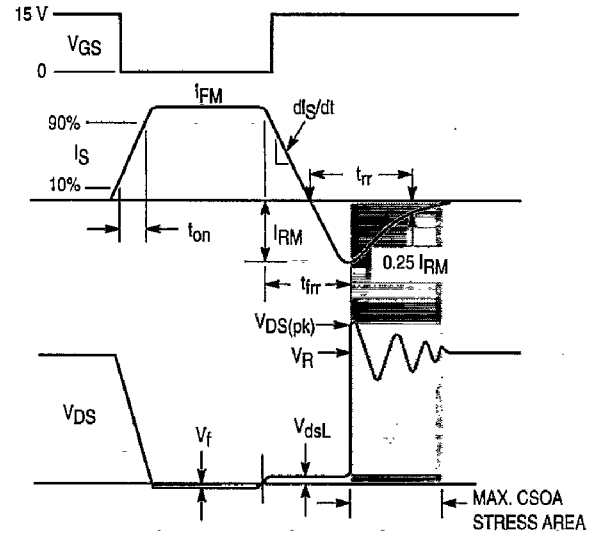



**Figure 11. Commutating Waveforms**

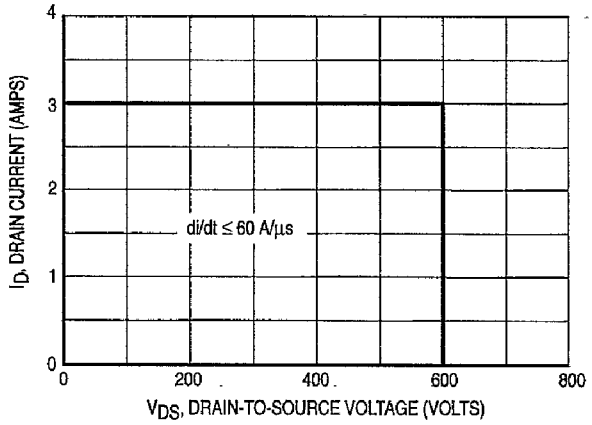



**Figure 12. Commutating Safe Operating Area (CSOA)**

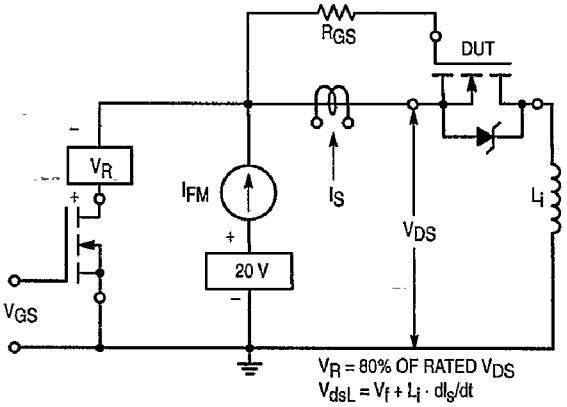



**Figure 13. Commutating Safe Operating Area Test Circuit**

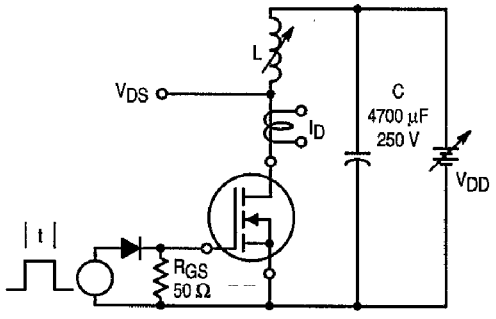



**Figure 14. Unclamped Inductive Switching Test Circuit**

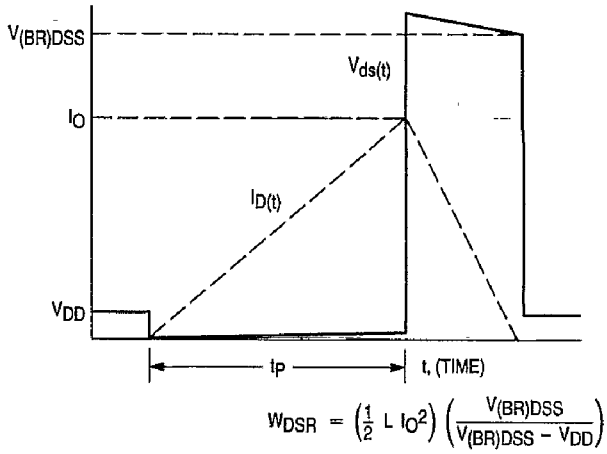



**Figure 15. Unclamped Inductive Switching Waveforms**

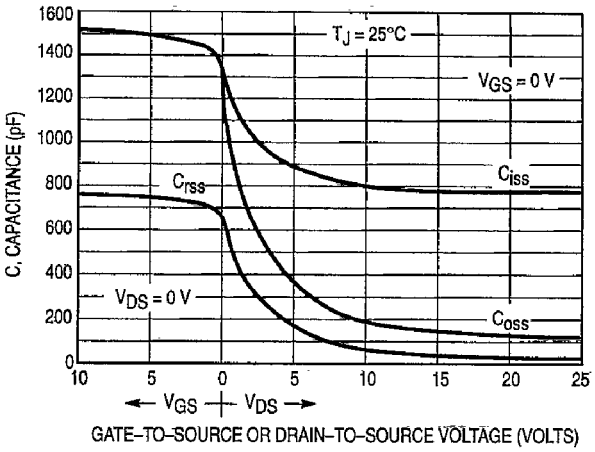



**Figure 16. Capacitance Variation**

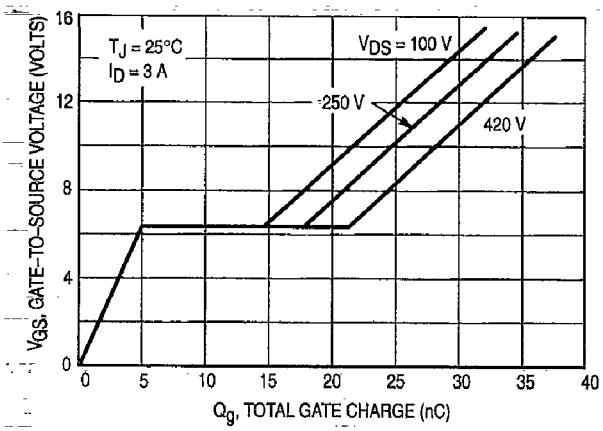
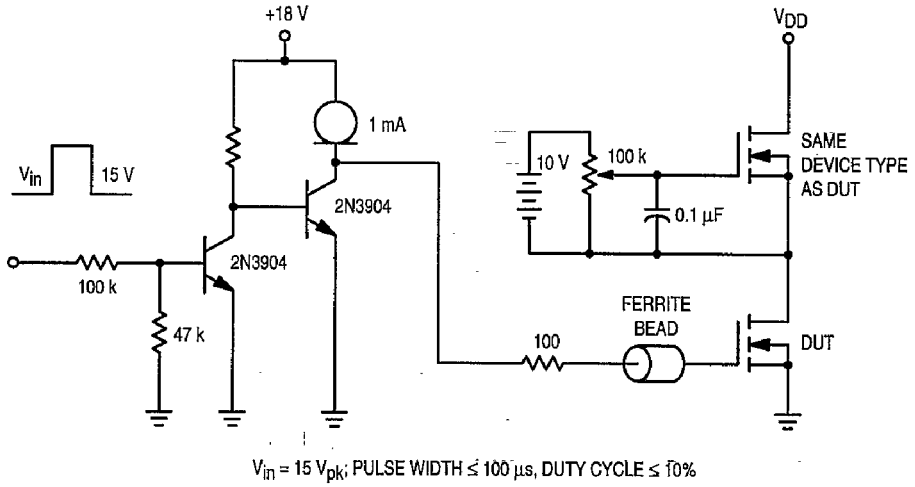



**Figure 17. Gate Charge versus Gate–To–Source Voltage**




$V_{in}$ = 15 $V_{pk}$; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

**Figure 18. Gate Charge Test Circuit**

*Designer's™ Data Sheet*

# TMOS E-FET ™

# Power Field Effect Transistor

## N–Channel Enhancement–Mode Silicon Gate

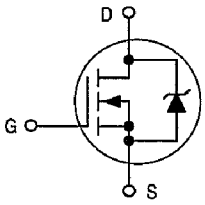
**MTP3N100E**

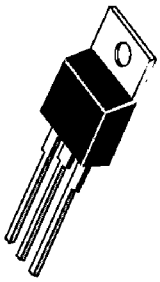
Motorola Preferred Device

**TMOS POWER FET**
**3.0 AMPERES**
**1000 VOLTS**
**$R_{DS(on)}$ = 4.0 OHM**

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature



**CASE 221A–06, Style 5**
**TO–220AB**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 1000 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 1000 | Vdc |
| Gate–Source Voltage — Continuous<br>— Non–Repetitive ($t_p \leq 10$ ms) | $V_{GS}$<br>$V_{GSM}$ | ± 20<br>± 40 | Vdc<br>Vpk |
| Drain Current — Continuous<br>— Continuous @ 100°C<br>— Single Pulse ($t_p \leq 10$ µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.0<br>2.4<br>9.0 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 125<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy — Starting $T_J$ = 25°C<br>($V_{DD}$ = 150 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 7.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 245 | mJ |
| Thermal Resistance — Junction to Case<br>— Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.00<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

REV 3

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc) | $V_{(BR)DSS}$ | 1000 | — | — | Vdc |
| Temperature Coefficient (Positive) | | — | 1.23 | — | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 1000 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | — | — | 10 | µAdc |
| ($V_{DS}$ = 1000 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | — | — | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS (1)** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc) | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | — | 6.0 | — | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc) | $R_{DS(on)}$ | — | 2.96 | 4.0 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 3.0 Adc) | $V_{DS(on)}$ | — | 4.97 | 12 | Vdc |
| ($I_D$ = 1.5 Adc, $T_J$ = 125°C) | | — | — | 10 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 1.5 Adc) | $g_{FS}$ | 2.0 | 3.56 | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | $C_{iss}$ | — | 1316 | 1800 | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{oss}$ | — | 117 | 260 | |
| Reverse Transfer Capacitance | $C_{rss}$ | — | 26 | 75 | |
| **SWITCHING CHARACTERISTICS (2)** | | | | | |
| Turn–On Delay Time | $t_{d(on)}$ | — | 13 | 25 | ns |
| Rise Time ($V_{DD}$ = 400 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_r$ | — | 19 | 40 | |
| Turn–Off Delay Time | $t_{d(off)}$ | — | 42 | 90 | |
| Fall Time | $t_f$ | — | 33 | 55 | |
| Gate Charge (See Figure 8) | $Q_T$ | — | 32.5 | 45 | nC |
| ($V_{DS}$ = 400 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_1$ | — | 6.0 | — | |
| | $Q_2$ | — | 14.6 | — | |
| | $Q_3$ | — | 13.5 | — | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage (1) ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | — | 0.794 | 1.1 | Vdc |
| ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | — | 0.63 | — | |
| Reverse Recovery Time (See Figure 14) | $t_{rr}$ | — | 615 | — | ns |
| ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_a$ | — | 104 | — | |
| | $t_b$ | — | 511 | — | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | — | 2.92 | — | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) | $L_D$ | — | 3.5 | — | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | 4.5 | | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | — | 7.5 | — | nH |

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

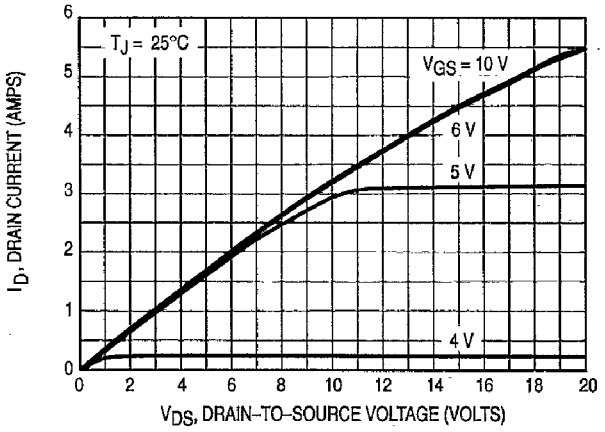



**Figure 1. On–Region Characteristics**

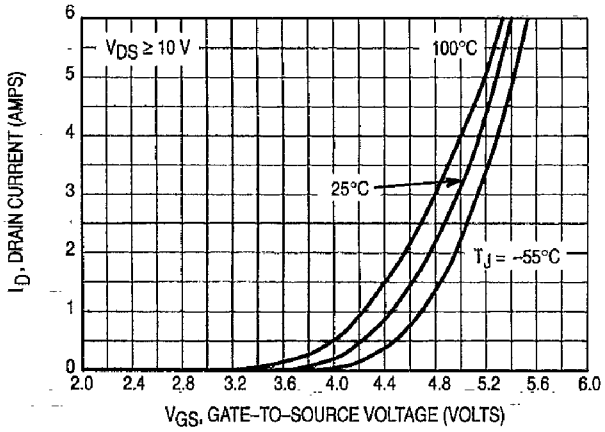



**Figure 2. Transfer Characteristics**

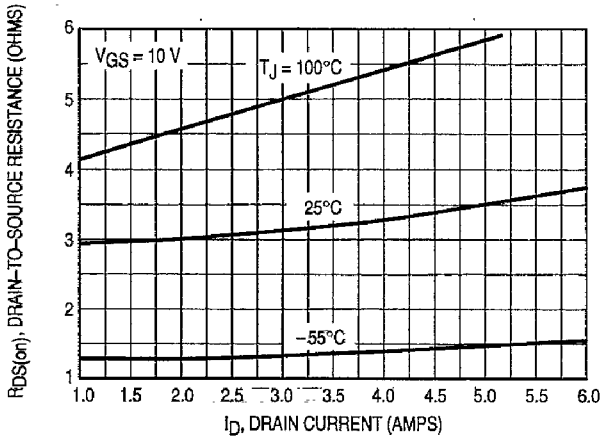



**Figure 3. On–Resistance versus Drain Current and Temperature**

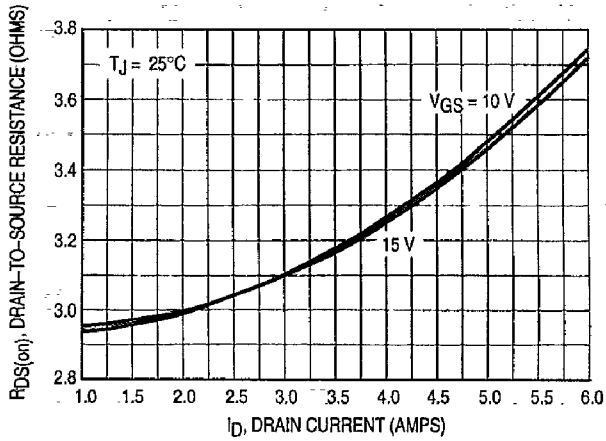



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

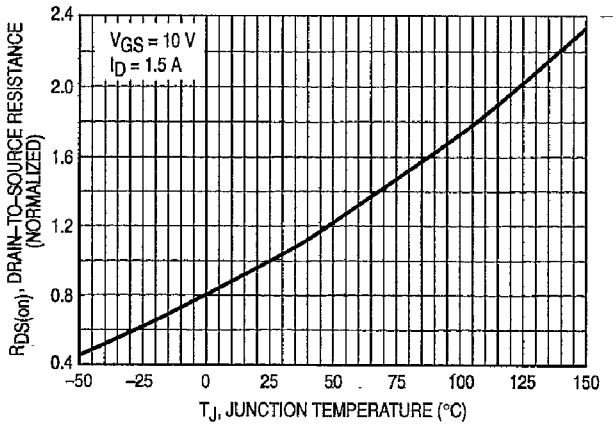



**Figure 5. On–Resistance Variation with Temperature**

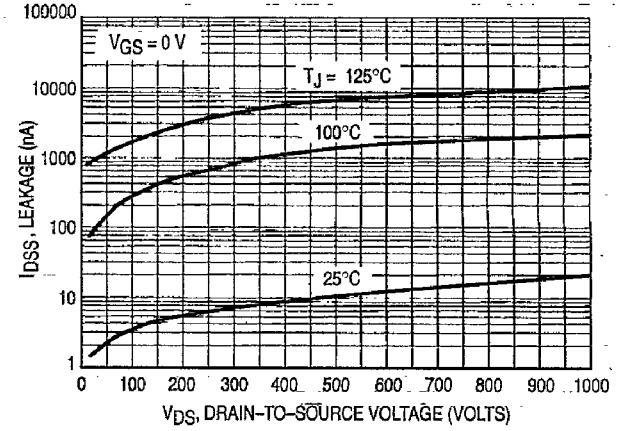



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

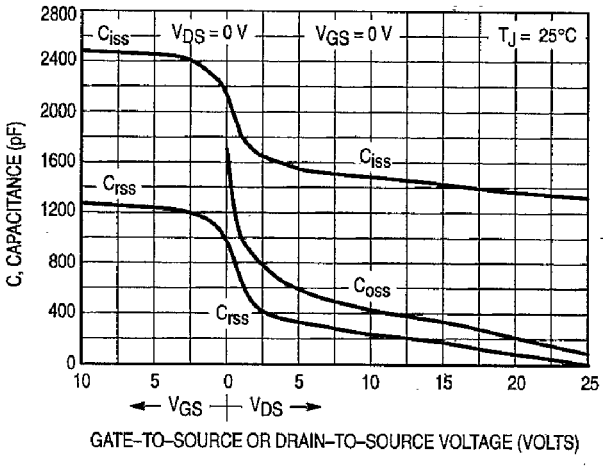



**Figure 7a. Capacitance Variation**

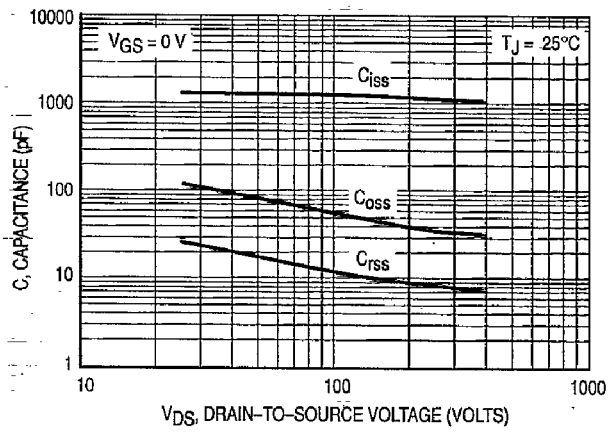



**Figure 7b. High Voltage Capacitance Variation**

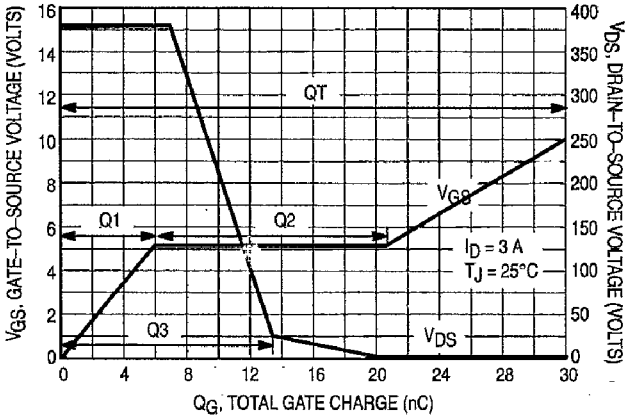



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

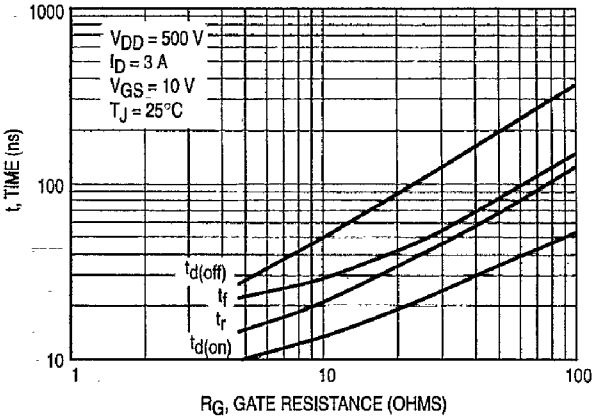



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

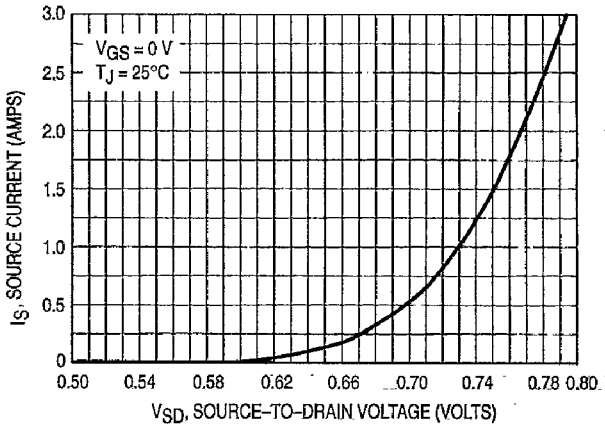



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

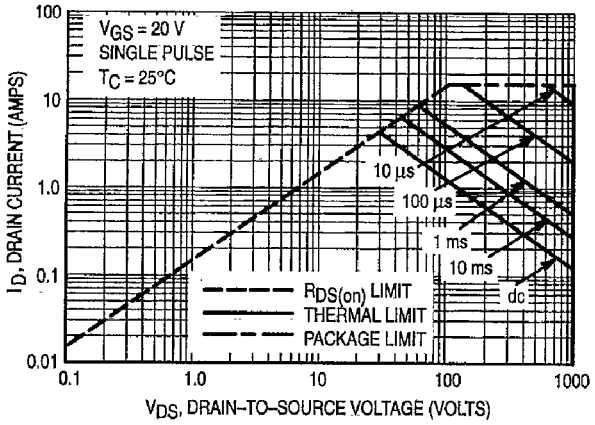



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

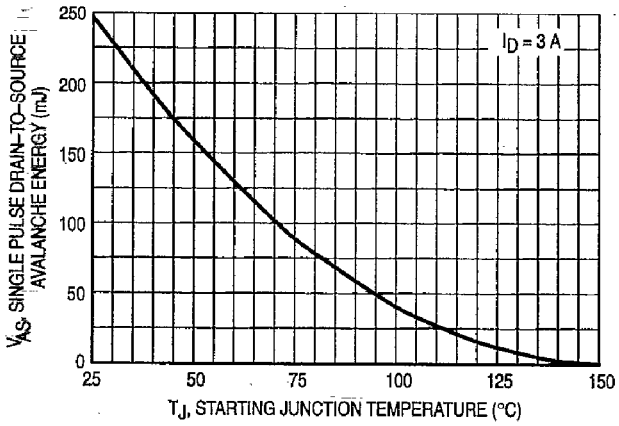



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

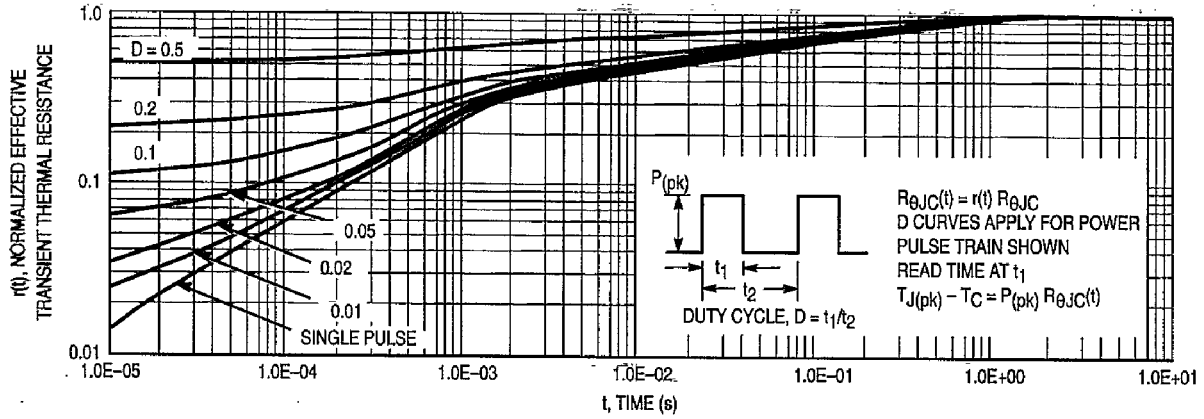



**Figure 13. Thermal Response**

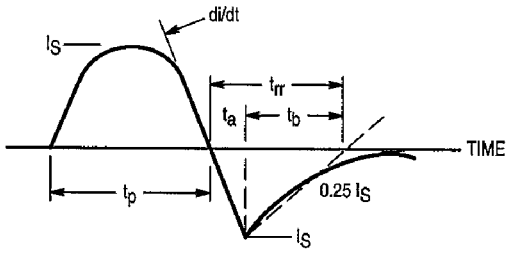



**Figure 14. Diode Reverse Recovery Waveform**