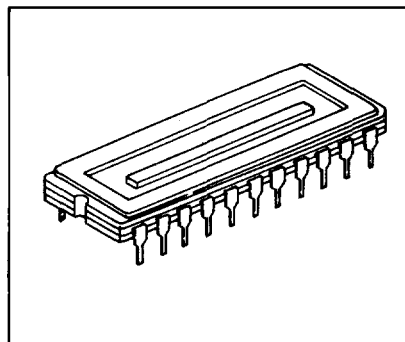


TCD142D

(TENTATIVE)

The TCD142D is a high sensitive and low dark current 2048-element image sensor. The sensor can be used for facsimile, imagescanner and OCR. The device contains a row of 2048 photodiodes, which provide a 8 lines/mm (200 DPI) across a A4 size paper.

The device is operated by only 12V power supply, and mounted in 22-pin cerdip package with hermetic sealed optical glass window.



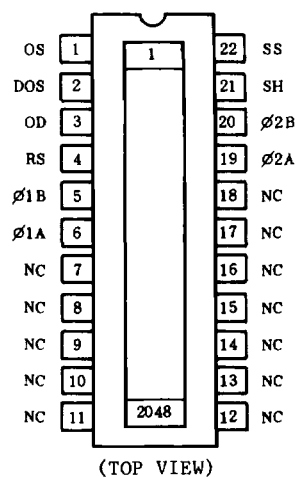
- Number of Image Sensing Elements : 2048
- Image Sensing Elements Size : 14 μ m by 14 μ m on 14 μ m centers
- Photo Sensing Region : High sensitive and low voltage dark signal pn photodiode.
- Clock : 2 phase
- Package : 22 pin Cerdip

MAXIMUM RATINGS (Note 1)

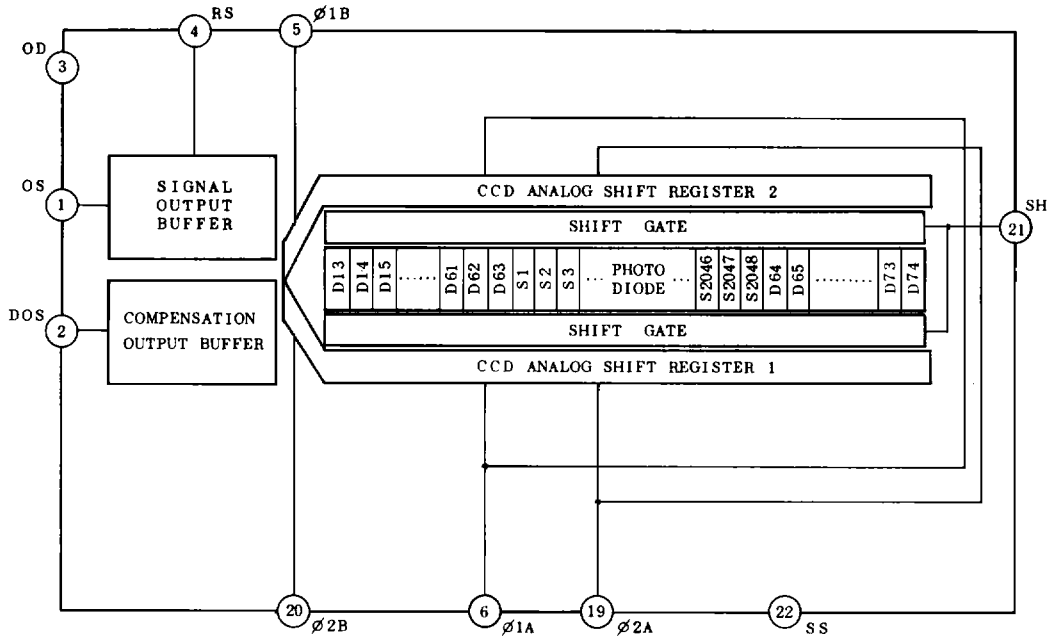
CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V ϕ	-0.3~15	V
Shift Pulse Voltage	VSH		
Reset Pulse Voltage	VRS		
Power Supply Voltage	VOD		
Operating Temperature	Topr	-25~60	°C
Storage Temperature	Tstg	-40~100	°C

(Note 1) All voltage are with respect to SS terminals (Ground).

PIN CONNECTIONS



CIRCUIT DIAGRAM



PIN NAMES

$\phi 1A$	Clock (Phase 1)
$\phi 2A$	Clock (Phase 2)
$\phi 1B$	Final Stage Clock (Phase 1)
$\phi 2B$	Final Stage Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
OS	Signal Output
DOS	Compensation Output
OD	Power
SS	Ground
NC	Non Connection

OPTICAL/ELECTRICAL CHARACTERISTICS

(Ta=25°C, VOD=12V, V_φ=V_{SH}=V_{RS}=12V (PULSE), f_φ=0.5MHz, f_{RS}=1MHz, LOAD RESISTANCE=100kΩ)
(t_{INT}(INTEGRATION TIME)=10ms, LIGHT SOURCE=DAYLIGHT FLUORESCENT LAMP)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Responsivity	R	4.8	6.0	7.2	V/lx·sec	(Note 2)
Photo Response Non Uniformity	PRNU	-	-	10	%	(Note 3)
Register Imbalance	RI	-	-	3	%	(Note 4)
Saturation Output Voltage	V _{SAT}	1.2	1.5	-	V	(Note 5)
Saturation Exposure	SE	0.17	0.25	-	lx·sec	(Note 6)
Dark Signal Voltage	V _{DRK}	-	0.2	1	mV	(Note 7)
Dark Signal Non Uniformity	DSNU	-	0.2	2	mV	(Note 7)
DC Power Dissipation	P _D	-	45	150	mW	
Total Transfer Efficiency	TTE	92	-	-	%	
Output Impedance	Z _o	-	-	1	kΩ	
Dynamic Range	DR	-	1500	-	-	(Note 8)
DC Signal Output Voltage	V _{OS}	3.5	4.5	6.0	V	(Note 9)
DC Compensation Output Voltage	V _{DOS}	3.5	4.5	6.0	V	(Note 9)
DC Mismatch Voltage	V _{OS} -V _{DOS}	-	-	100	mV	

(Note 2) Responsivity for 2854K W-Lamp is 18V/lx·sec (Typ.)

(Note 3) Measured at 50% of SE (Typ.)

Definition of PRNU: $PRNU = \frac{\Delta x}{\bar{x}} \times 100 (\%)$

Where $\bar{x}$ is average of total signal outputs and Δx is the maximum deviation from $\bar{x}$ under uniform illumination.

(Note 4) Measured at 50% of SE (Typ.)

RI is defined as follows:

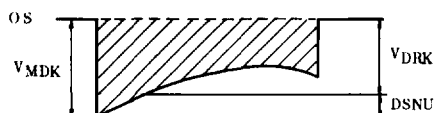
$$RI = \frac{\sum_{n=1}^{2047} |x_n - x_{n+1}|}{2047 \times \bar{x}} \times 100 (\%)$$

Where x_n and x_{n+1} are signal outputs of each pixel. $\bar{x}$ is average of total signal outputs.

(Note 5) V_{SAT} is defined as minimum Saturation Output Voltage of all effective pixels.

(Note 6) Definition of SE: $SE = \frac{V_{SAT}}{R}$

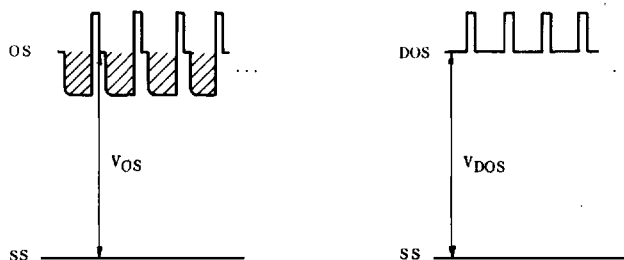
(Note 7) V_{DRK} is defined as average dark signal voltage of all effective pixels.
 $DSNU$ is defined as different voltage between V_{DRK} and V_{MDK} , when V_{MDK} is maximum dark voltage.



(Note 8) Definition of DR: $DR = \frac{V_{SAT}}{V_{DRK}}$

V_{DRK} is proportional to t_{INT} (Integration time). So the shorter t_{INT} is, the wider DR is.

(Note 9) DC Signal Output Voltage and DC Compensation Output Voltage are defined as follows:



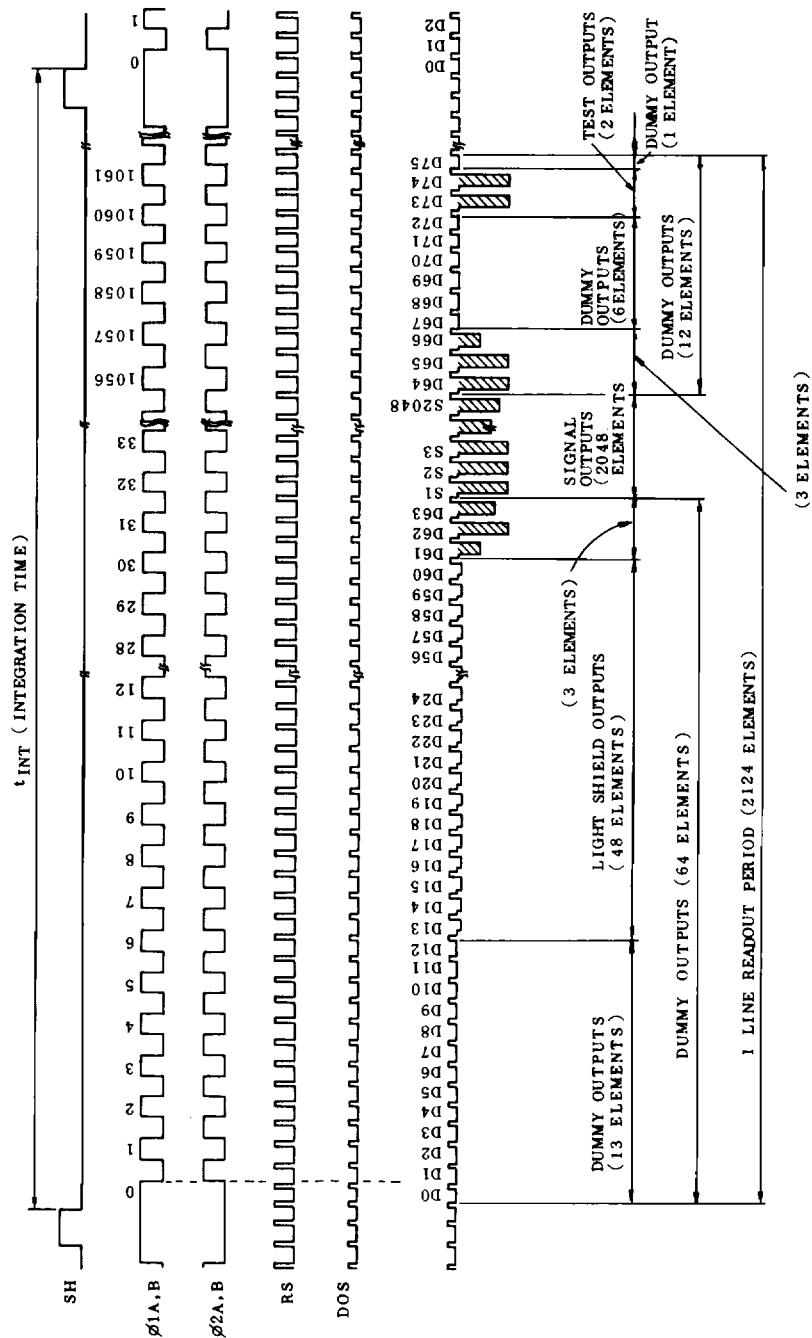
OPERATING CONDITION

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	H-Level	V_{ϕ}	$V_{OD}-1$	V_{OD}	V_{OD}	V
	L-Level		0	0.5	0.8	
Shift Pulse Voltage	H-Level	V_{SH}	$V_{OD}-1$	V_{OD}	V_{OD}	V
	L-Level		0	0.5	0.8	
Reset Pulse Voltage	H-Level	V_{RS}	$V_{OD}-1$	V_{OD}	V_{OD}	V
	L-Level		0	0.5	0.8	
Power Supply Voltage		V_{OD}	11.4	12	13	V

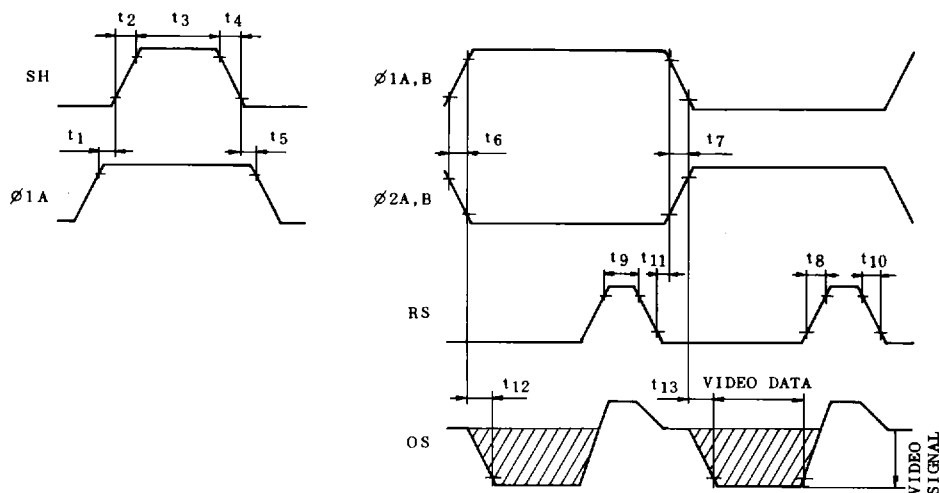
CLOCK CHARACTERISTICS ($T_a=25^{\circ}\text{C}$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	-	0.5	5	MHz
Reset Pulse Frequency	f_{RS}	-	1.0	10	MHz
Clock Capacitance	$C_{\phi A}$	-	400	500	pF
Final Stage Clock Capacitance	$C_{\phi B}$	-	10	25	pF
Shift Gate Capacitance	C_{SH}	-	150	250	pF
Reset Gate Capacitance	C_{RS}	-	10	25	pF

TIMING CHART



TIMING REQUIREMENTS

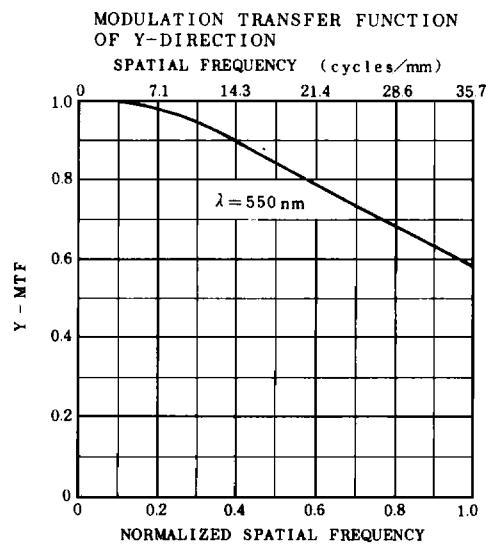
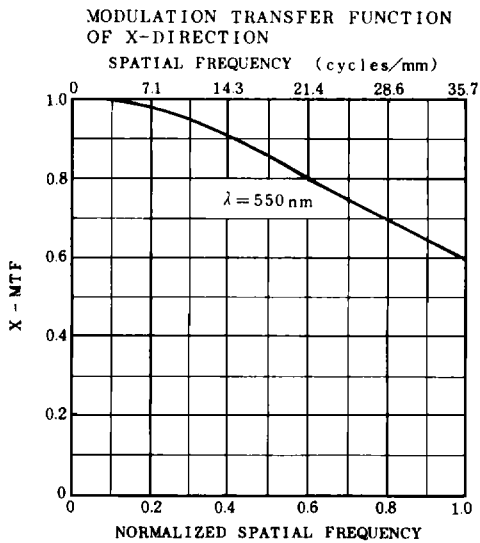
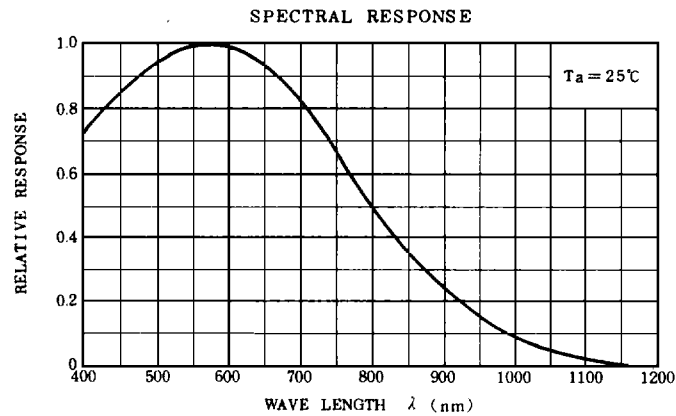


CHARACTERISTIC	SYMBOL	MIN.	TYP. (Note 10)	MAX.	UNIT
Pulse Timing of SH and φ1A	t_1, t_5	0	100	-	ns
SH Pulse Rise Time, Fall Time	t_2, t_4	0	50	-	ns
SH Pulse Width	t_3	200	1000	-	ns
φ1A,B, φ2A,B Pulse Rise Time, Fall Time	t_6, t_7	0	100	-	ns
RS Pulse Rise Time, Fall Time	t_8, t_{10}	0	20	-	ns
RS Pulse Width	t_9	40	250	-	ns
Pulse Timing of φ1B, φ2B and RS	t_{11}	10	250	-	ns
Video Data Delay Time (Note 11)	t_{12}, t_{13}	-	50	-	ns

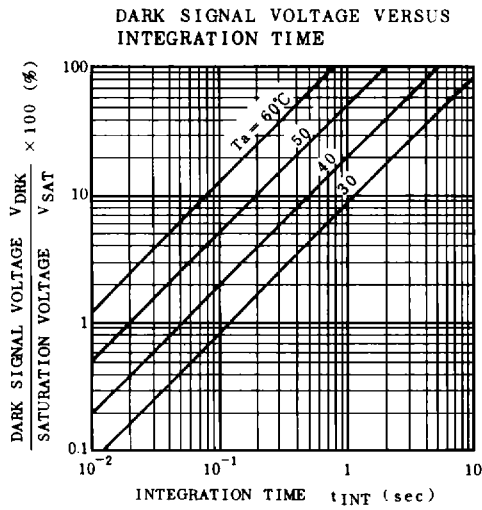
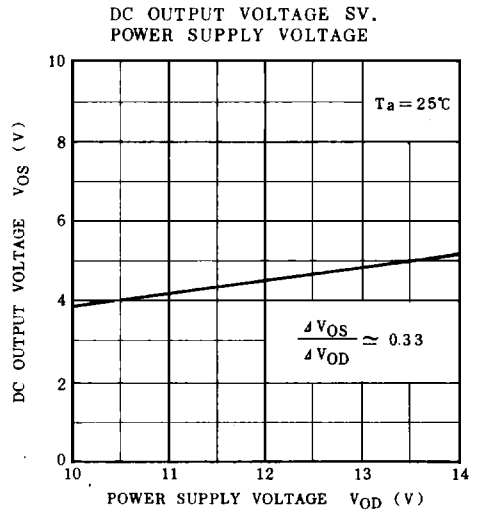
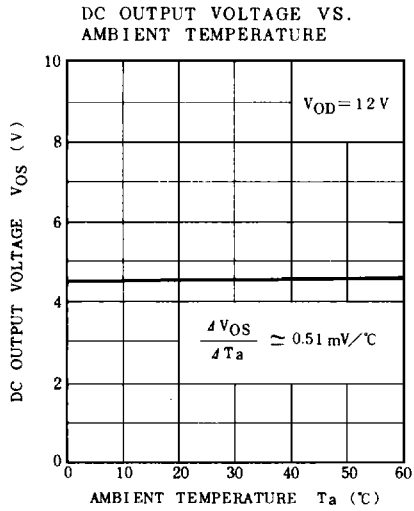
(Note 10) TYP. is the case of $f_{RS}=1\text{MHz}$.

(Note 11) Load Resistance is $100\text{k}\Omega$.

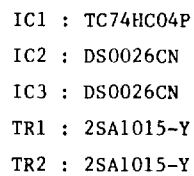
TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES(Cont'd)



TYPICAL DRIVE CIRCUIT



CAUTION**1. Window Glass**

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

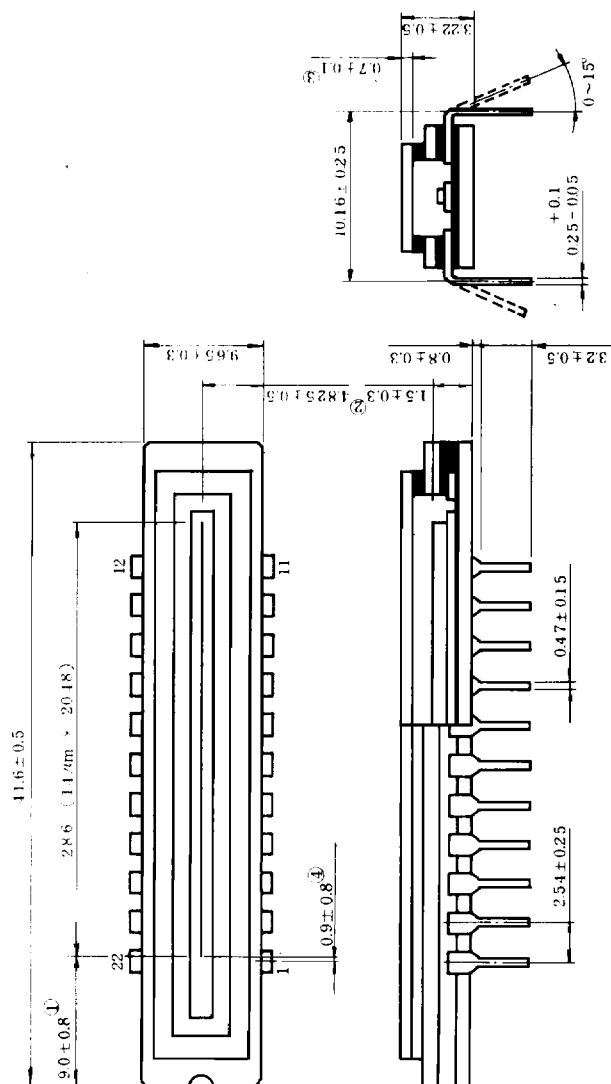
4. Lead Frame Forming

Since this package is not stout against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to a PCB.

PACKAGE OUTLINE

Unit in mm



- ① No.1 SENSOR ELEMENT (S1) TO EDGE OF PACKAGE
- ② TOP OF CHIP TO BOTTOM OF PACKAGE
- ③ GLASS THICKNESS ($n=1.5$)
- ④ No.1 SENSOR ELEMENT(S1) TO CENTER OF No.1 pin.