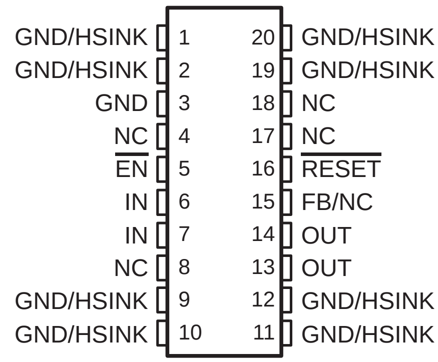
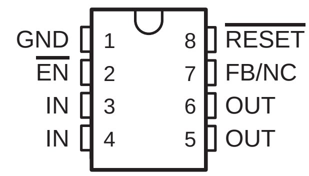
- **1 A Low-Dropout Voltage Regulator**
- **Available in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V, 5.0-V Fixed Output and Adjustable Versions**
- **Dropout Voltage Down to 230 mV at 1 A (TPS76750)**
- **Ultra Low 85 μA Typical Quiescent Current**
- **Fast Transient Response**
- **2% Tolerance Over Specified Conditions for Fixed-Output Versions**
- **Open Drain Power-On Reset With 200-ms Delay (See TPS768xx for PG Option)**
- **8-Pin SOIC and 20-Pin TSSOP PowerPAD™ (PWP) Package**
- **Thermal Shutdown Protection**

PWP PACKAGE
(TOP VIEW)



NC – No internal connection

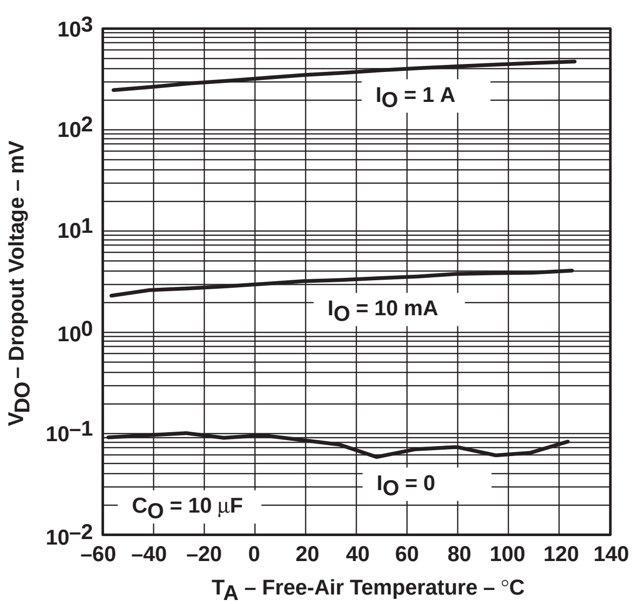
D PACKAGE
(TOP VIEW)



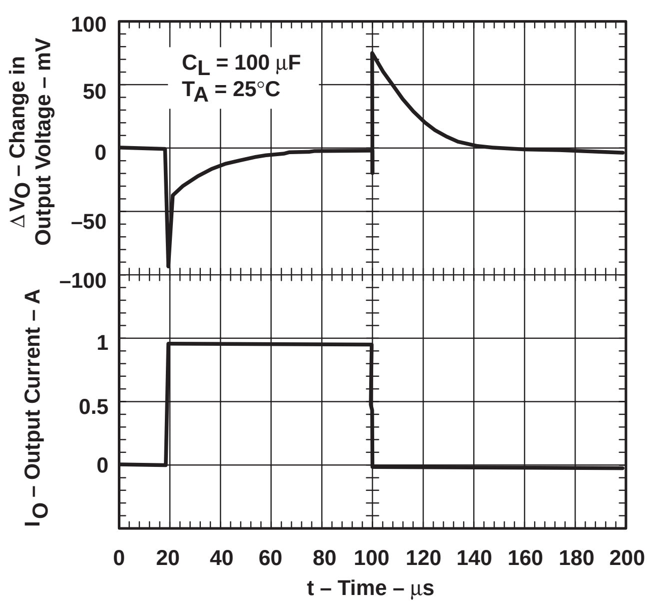
description

This device is designed to have a fast transient response and be stable with 10-μF low ESR capacitors. This combination provides high performance at a reasonable cost.

TPS76733
DROPOUT VOLTAGE
vs
FREE-AIR TEMPERATURE



TPS76733
LOAD TRANSIENT RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

description (continued)

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 230 mV at an output current of 1 A for the TPS76750) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85 μA over the full range of output current, 0 mA to 1 A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to 1 μA at T_J = 25°C.

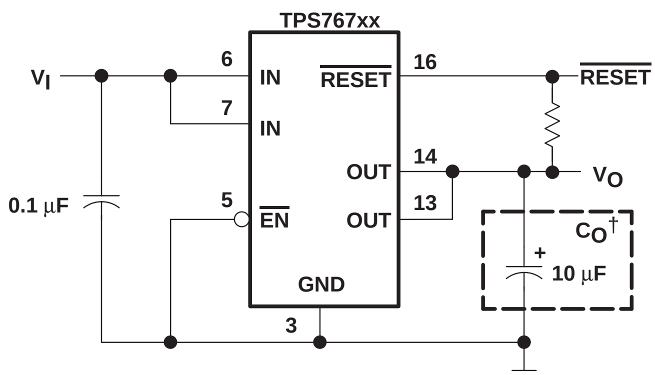
The $\overline{\text{RESET}}$ output of the TPS767xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767xx is offered in 1.5-V, 1.8-V, 2.5-V, 2.7-V, 2.8-V, 3.0-V, 3.3-V and 5.0-V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5 V to 5.5 V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767xx family is available in 8 pin SOIC and 20 pin PWP packages.

AVAILABLE OPTIONS

T_J	OUTPUT VOLTAGE (V)	PACKAGED DEVICES	
	TYP	TSSOP (PWP)	SOIC (D)
–40°C to 125°C	5.0	TPS76750Q	TPS76750Q
	3.3	TPS76733Q	TPS76733Q
	3.0	TPS76730Q	TPS76730Q
	2.8	TPS76728Q	TPS76728Q
	2.7	TPS76727Q	TPS76727Q
	2.5	TPS76725Q	TPS76725Q
	1.8	TPS76718Q	TPS76718Q
	1.5	TPS76715Q	TPS76715Q
	Adjustable 1.5 V to 5.5 V	TPS76701Q	TPS76701Q

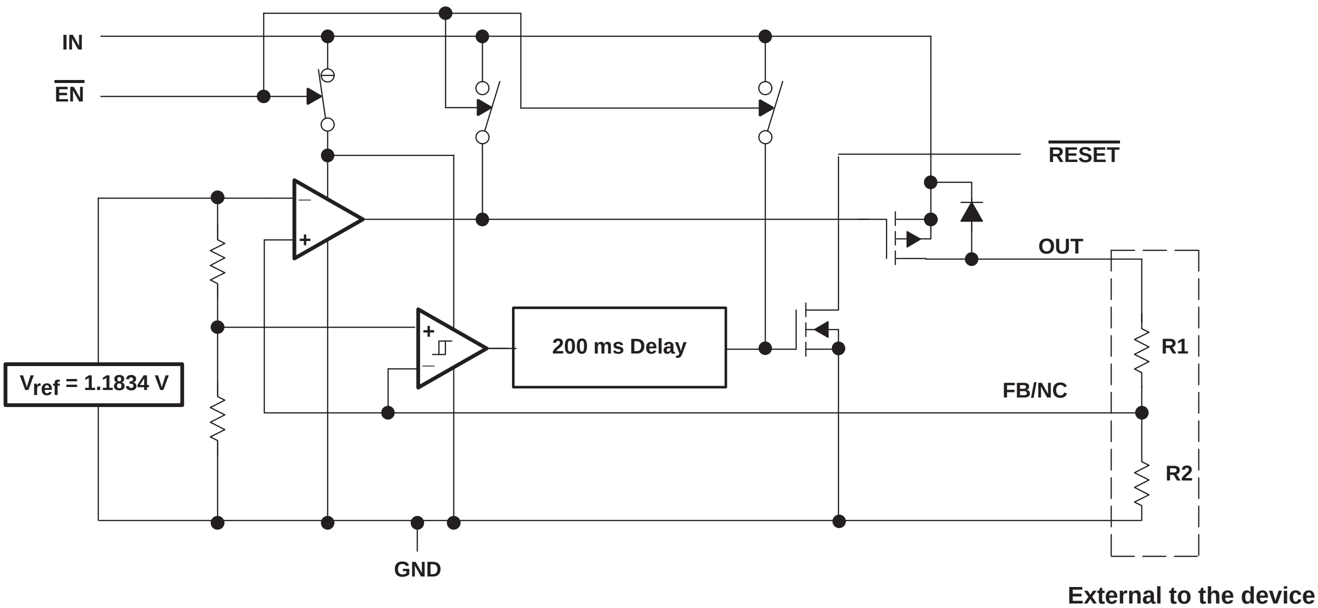
The TPS76701 is programmable using an external resistor divider (see application information). The D and PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., TPS76701QDR).



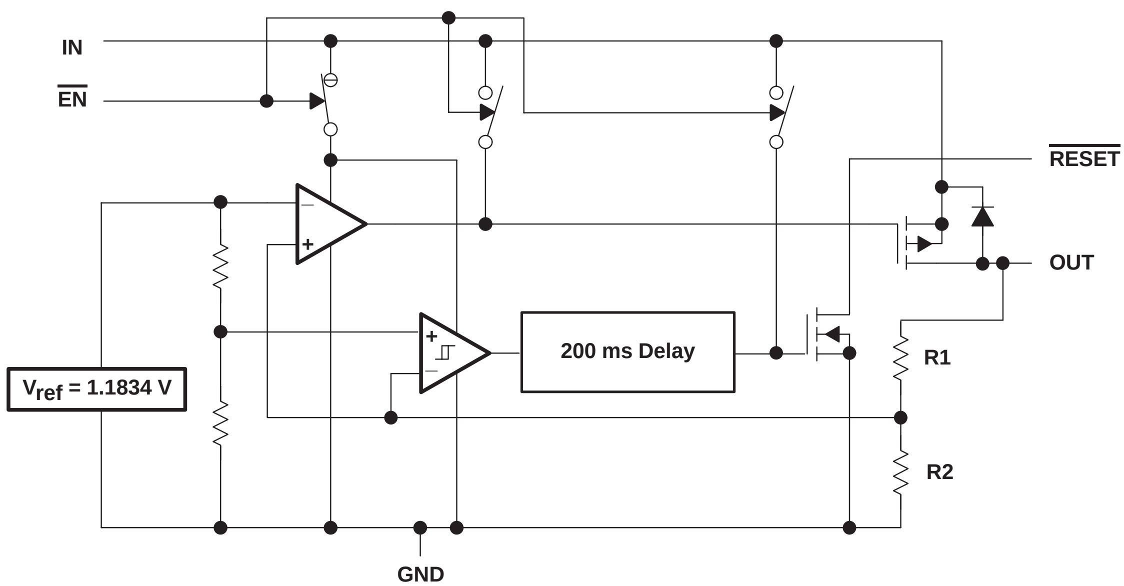
† See application information section for capacitor selection details.

Figure 1. Typical Application Configuration (For Fixed Output Options)

functional block diagram—adjustable version



functional block diagram—fixed-voltage version



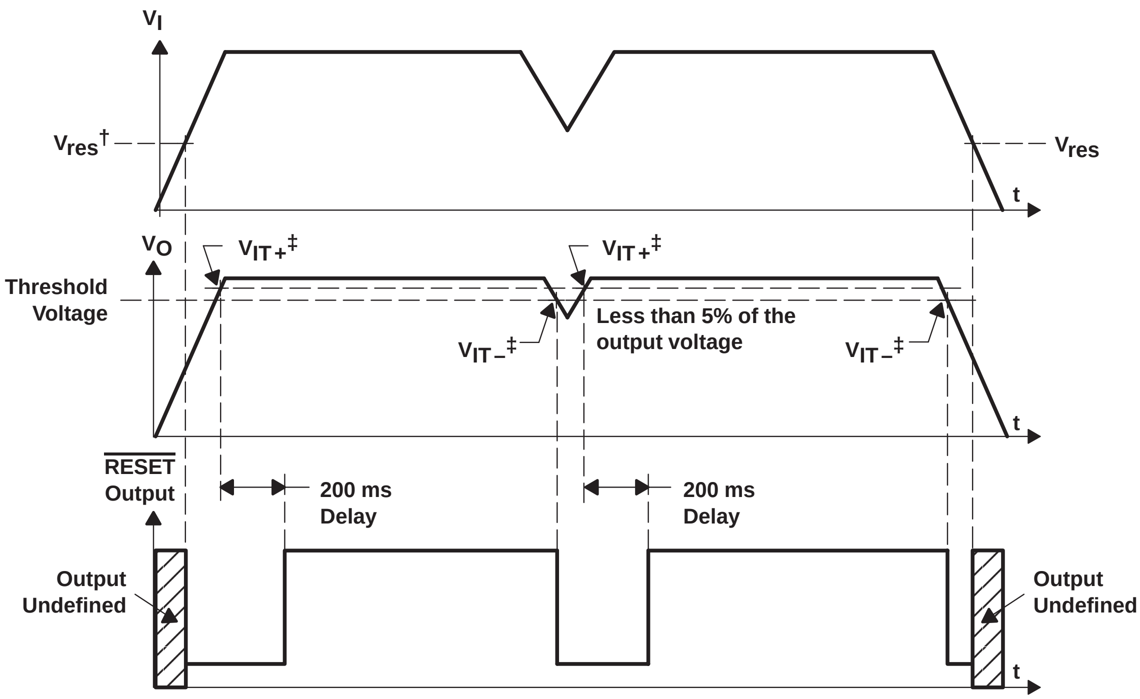
Terminal Functions – SOIC Package

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	2	I	Enable input
FB/NC	7	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	1		Regulator ground
IN	3, 4	I	Input voltage
OUT	5, 6	O	Regulated output voltage
$\overline{\text{RESET}}$	8	O	$\overline{\text{RESET}}$ output

Terminal Functions – PWP Package

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	5	I	Enable input
FB/NC	15	I	Feedback input voltage for adjustable device (no connect for fixed options)
GND	3		Regulator ground
GND/HSINK	1, 2, 9, 10, 11, 12, 19, 20		Ground/heatsink
IN	6, 7	I	Input voltage
NC	4, 8, 17, 18		No connect
OUT	13, 14	O	Regulated output voltage
$\overline{\text{RESET}}$	16	O	$\overline{\text{RESET}}$ output

timing diagram



† V_{res} is the minimum input voltage for a valid $\overline{\text{RESET}}$. The symbol V_{res} is not currently listed within EIA or JEDEC standards for semiconductor symbology.

‡ VIT –Trip voltage is typically 5% lower than the output voltage (95%V_O) V_{IT-} to V_{IT+} is the hysteresis voltage.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range‡, V_I .... –0.3 V to 13.5 V
Voltage range at $\overline{EN}$ .... –0.3 V to V_I + 0.3 V
Maximum $\overline{RESET}$ voltage .... 16.5 V
Peak output current .... Internally limited
Output voltage, V_O (OUT, FB) .... 7 V
Continuous total power dissipation .... See dissipation rating tables
Operating virtual junction temperature range, T_J .... –40°C to 125°C
Storage temperature range, T_{stg} .... –65°C to 150°C
ESD rating, HBM .... 2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

DISSIPATION RATING TABLE 2 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
PWP#	0	2.9 W	23.5 mW/°C	1.9 W	1.5 W
	300	4.3 W	34.6 mW/°C	2.8 W	2.2 W
PWP‖	0	3 W	23.8 mW/°C	1.9 W	1.5 W
	300	7.2 W	57.9 mW/°C	4.6 W	3.8 W

This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5-in × 5-in PCB, 1 oz. copper, 2-in × 2-in coverage (4 in^2).
‖ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5-in × 2-in PCB, 1 oz. copper with layers 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in^2) and layers 3 and 6 at 100% coverage (6 in^2). For more information, refer to TI technical brief SLMA002.

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I☆	2.7	10	V
Output voltage range, V_O	1.5	5.5	V
Output current, I_O (Note 1)	0	1.0	A
Operating virtual junction temperature, T_J (Note 1)	–40	125	°C

☆ To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$.
NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage (10 µA to 1 A load) (see Note 2)	TPS76701	1.5 V ≤ V_O ≤ 5.5 V,	T_J = 25°C		V_O		V
	TPS76701	1.5 V ≤ V_O ≤ 5.5 V,	T_J = –40°C to 125°C	0.98V_O		1.02V_O	
	TPS76715	T_J = 25°C,	2.7 V < V_{IN} < 10 V		1.5		
	TPS76715	T_J = –40°C to 125°C,	2.7 V < V_{IN} < 10 V	1.470		1.530	
	TPS76718	T_J = 25°C,	2.8 V < V_{IN} < 10 V		1.8		
	TPS76718	T_J = –40°C to 125°C,	2.8 V < V_{IN} < 10 V	1.764		1.836	
	TPS76725	T_J = 25°C,	3.5 V < V_{IN} < 10 V		2.5		
	TPS76725	T_J = –40°C to 125°C,	3.5 V < V_{IN} < 10 V	2.450		2.550	
	TPS76727	T_J = 25°C,	3.7 V < V_{IN} < 10 V		2.7		
	TPS76727	T_J = –40°C to 125°C,	3.7 V < V_{IN} < 10 V	2.646		2.754	
	TPS76728	T_J = 25°C,	3.8 V < V_{IN} < 10 V		2.8		
	TPS76728	T_J = –40°C to 125°C,	3.8 V < V_{IN} < 10 V	2.744		2.856	
	TPS76730	T_J = 25°C,	4.0 V < V_{IN} < 10 V		3.0		
	TPS76730	T_J = –40°C to 125°C,	4.0 V < V_{IN} < 10 V	2.940		3.060	
	TPS76733	T_J = 25°C,	4.3 V < V_{IN} < 10 V		3.3		
	TPS76733	T_J = –40°C to 125°C,	4.3 V < V_{IN} < 10 V	3.234		3.366	
	TPS76750	T_J = 25°C,	6.0 V < V_{IN} < 10 V		5.0		
	TPS76750	T_J = –40°C to 125°C,	6.0 V < V_{IN} < 10 V	4.900		5.100	
Quiescent current (GND current) $\overline{EN}$ = 0V, (see Note 2)		10 µA < I_O < 1 A,	T_J = 25°C		85		µA
		I_O = 1 A,	T_J = –40°C to 125°C			125	
Output voltage line regulation ($\Delta V_O/V_O$) (see Notes 2 and 3)		V_O + 1 V < V_I ≤ 10 V,	T_J = 25°C		0.01		%/V
Load regulation					3		mV
Output noise voltage		BW = 300 Hz to 50 kHz, C_O = 10 µF,	T_J = 25°C		190		µVrms
Output current Limit		V_O = 0 V			1.7	2	A
Thermal shutdown junction temperature					150		°C
Standby current		$\overline{EN}$ = V_I,	T_J = 25°C, 2.7 V < V_I < 10 V		1		µA
		$\overline{EN}$ = V_I,	T_J = –40°C to 125°C 2.7 V < V_I < 10 V			10	µA
FB input current	TPS76701	FB = 1.5 V			2		nA
High level enable input voltage				1.7			V
Low level enable input voltage						0.9	V
Power supply ripple rejection (see Note 2)		f = 1 KHz, T_J = 25°C	C_O = 10 µF,		60		dB
Reset	Minimum input voltage for valid $\overline{RESET}$	$I_{O(RESET)}$ = 300µA			1.1		V
	Trip threshold voltage	V_O decreasing		92		98	%V_O
	Hysteresis voltage	Measured at V_O			0.5		%V_O
	Output low voltage	V_I = 2.7 V,	$I_{O(RESET)}$ = 1mA		0.15	0.4	V
	Leakage current	$V_{(RESET)}$ = 5 V				1	µA
	RESET time-out delay				200		ms

NOTE 2: Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. Maximum IN voltage 10V.

electrical characteristics over recommended operating free-air temperature range, $V_i = V_{O(typ)} + 1$ V, $I_O = 1$ mA, $\overline{EN} = 0$ V, $C_O = 10$ µF (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input current (EN)		$\overline{EN} = 0$ V		–1	0	1	µA
		$\overline{EN} = V_I$		–1		1	
Dropout voltage (See Note 4)	TPS76728	$I_O = 1$ A,	$T_J = 25°C$		500		mV
		$I_O = 1$ A,	$T_J = –40°C$ to 125°C			825	
	TPS76730	$I_O = 1$ A,	$T_J = 25°C$		450		
		$I_O = 1$ A,	$T_J = –40°C$ to 125°C			675	
	TPS76733	$I_O = 1$ A,	$T_J = 25°C$		350		
		$I_O = 1$ A,	$T_J = –40°C$ to 125°C			575	
	TPS76750	$I_O = 1$ A,	$T_J = 25°C$		230		
		$I_O = 1$ A,	$T_J = –40°C$ to 125°C			380	

NOTES: 3. If $V_O \leq 1.8$ V then $V_{imax} = 10$ V, $V_{imin} = 2.7$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O \geq 2.5$ V then $V_{imax} = 10$ V, $V_{imin} = V_O + 1$ V:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O\left(V_{imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

4. IN voltage equals V_O(Typ) – 100 mV; TPS76701 output voltage set to 3.3 V nominal with external resistor divider. TPS76715, TPS76718, TPS76725, and TPS76727 dropout voltage limited by input voltage range limitations (i.e., TPS76730 input voltage needs to drop to 2.9 V for purpose of this test).

Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Free-air temperature	5, 6, 7
	Ground current	vs Free-air temperature	8, 9
	Power supply ripple rejection	vs Frequency	10
	Output noise	vs Frequency	11
Z_O	Output impedance	vs Frequency	12
V_{DO}	Dropout voltage	vs Free-air temperature	13
	Line transient response		14, 16
	Load transient response		15, 17
	Output voltage	vs Time	18
	Dropout voltage	vs Input voltage	19
	Equivalent series resistance (ESR)	vs Output current	21 – 24

TYPICAL CHARACTERISTICS

TPS76733
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

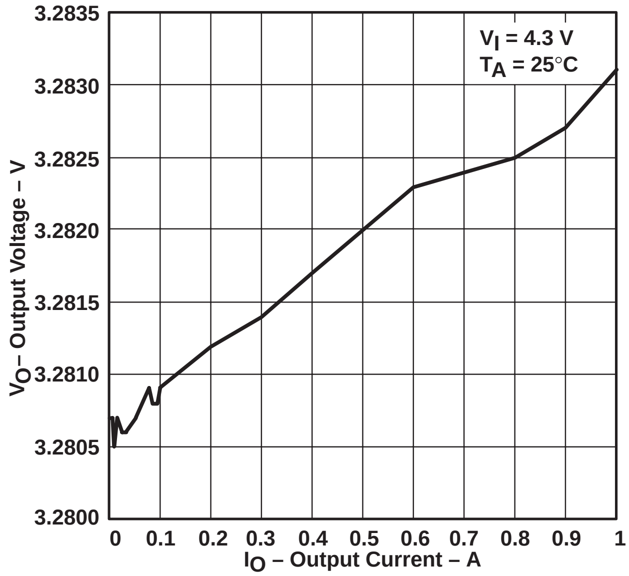


Figure 2

TPS76715
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

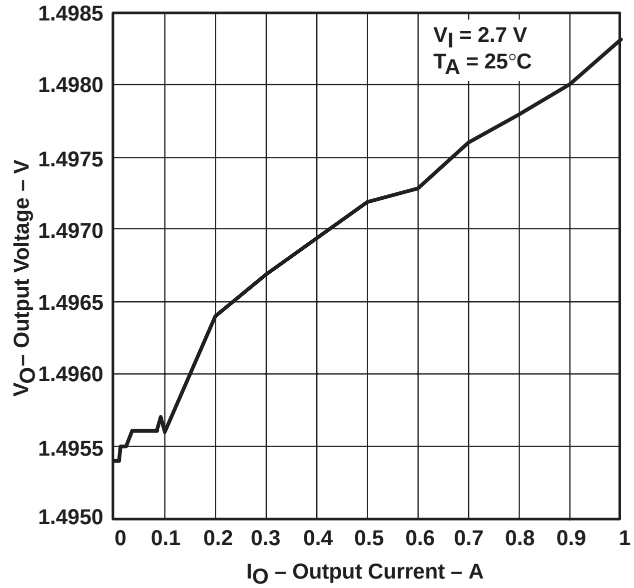


Figure 3

TPS76725
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

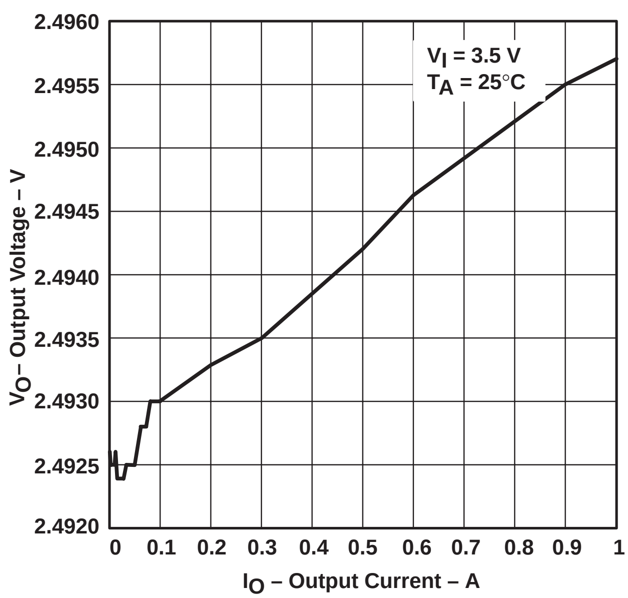


Figure 4

TPS76733
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

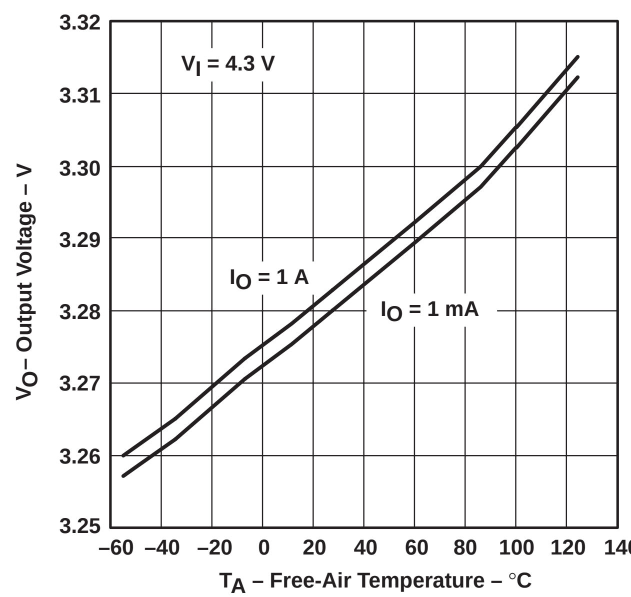


Figure 5

TYPICAL CHARACTERISTICS

TPS76715
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

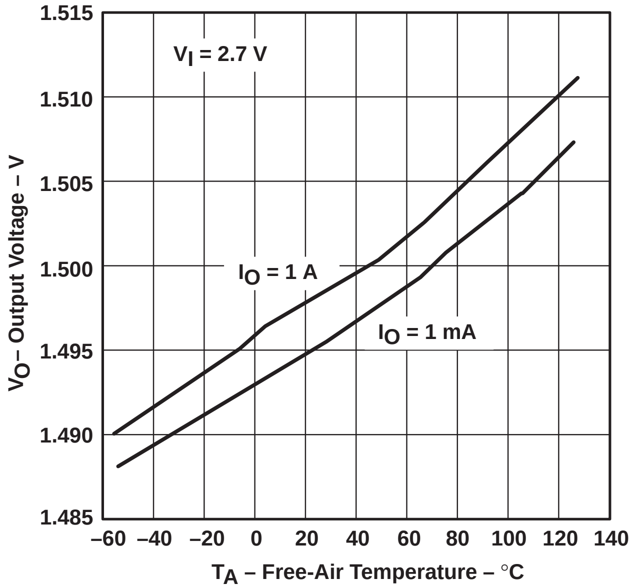


Figure 6

TPS76725
OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

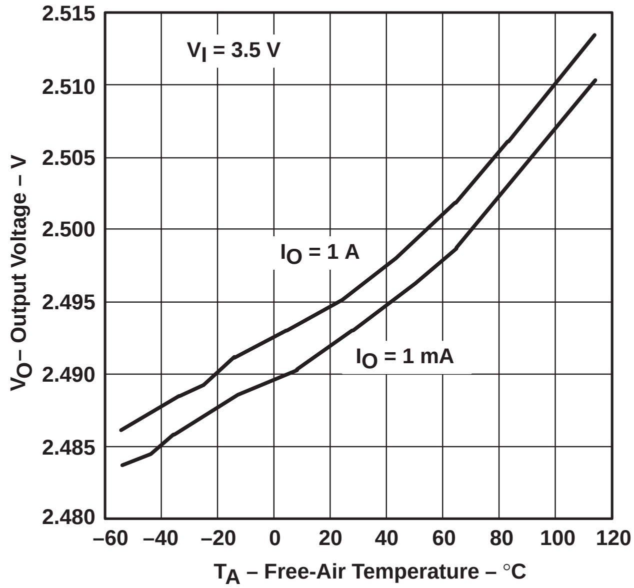


Figure 7

TPS76733
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

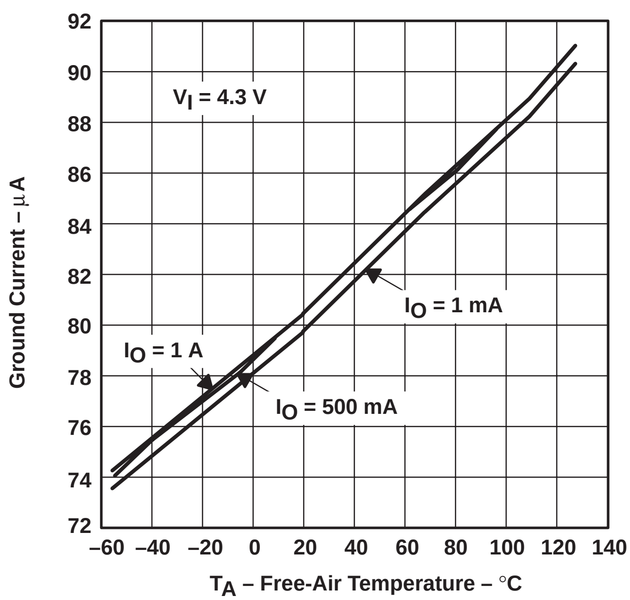


Figure 8

TPS76715
GROUND CURRENT
vs
FREE-AIR TEMPERATURE

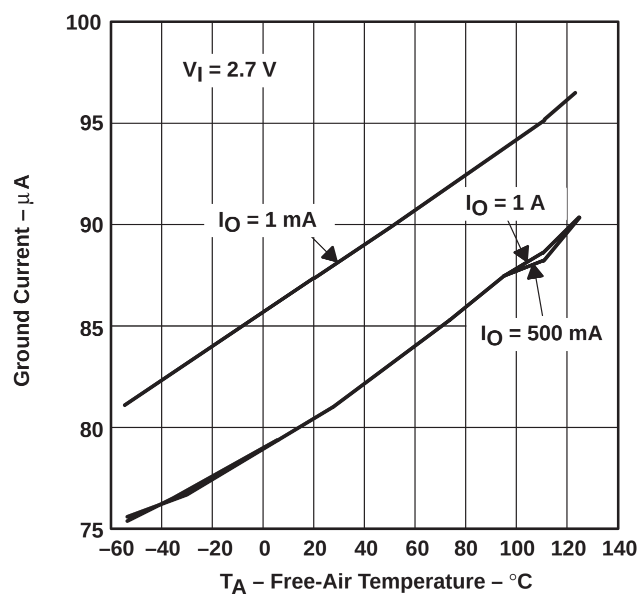


Figure 9

TYPICAL CHARACTERISTICS

TPS76733
POWER SUPPLY RIPPLE REJECTION vs FREQUENCY

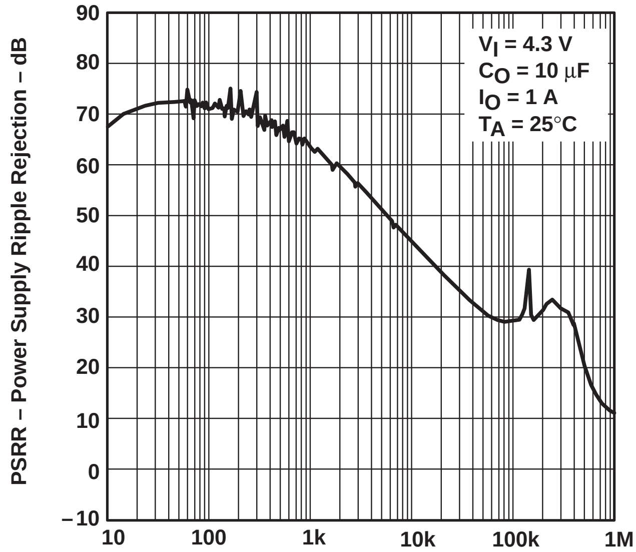


Figure 10

TPS76733
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

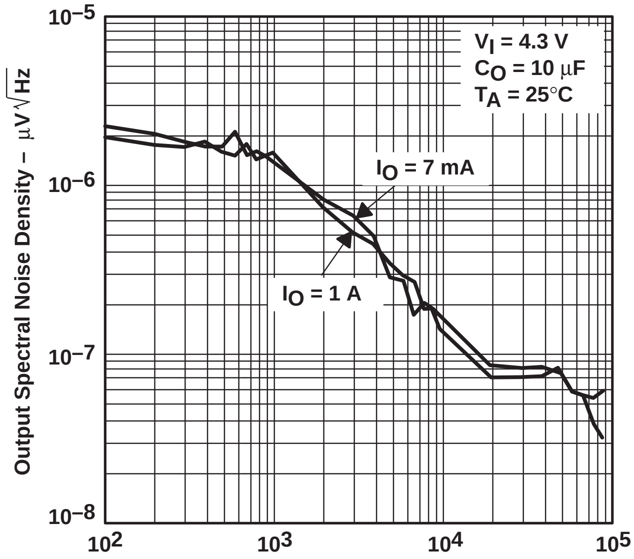


Figure 11

TPS76733
OUTPUT IMPEDANCE vs FREQUENCY

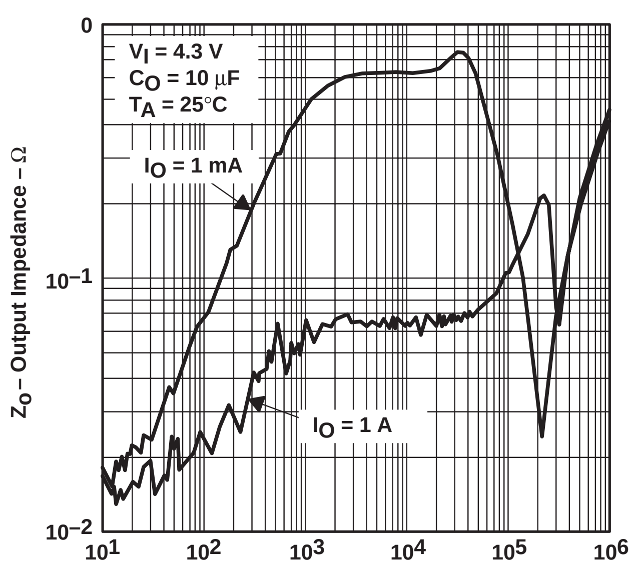


Figure 12

TPS76733
DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

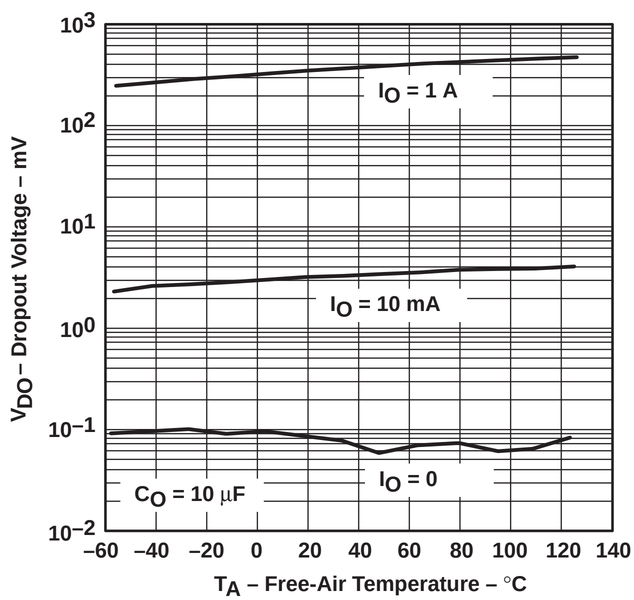


Figure 13

TYPICAL CHARACTERISTICS

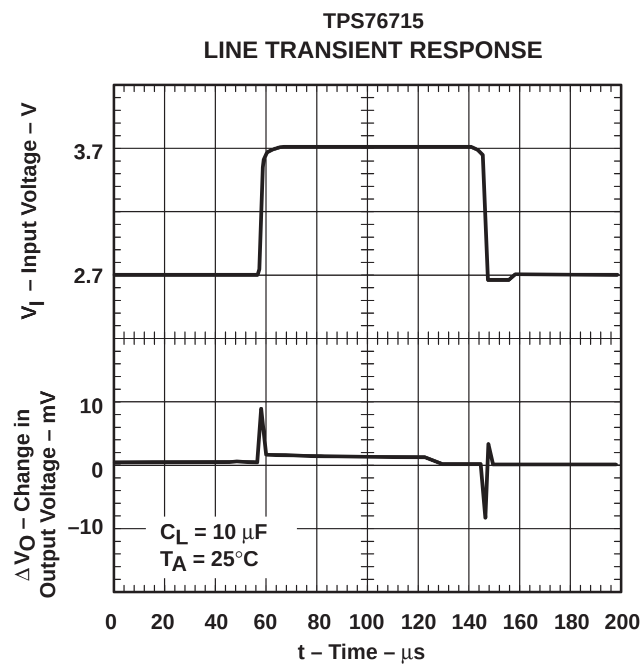


Figure 14

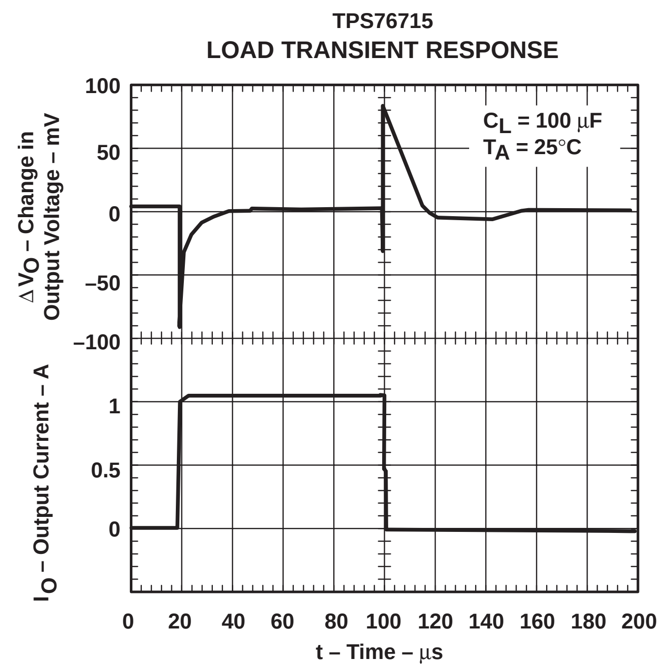


Figure 15

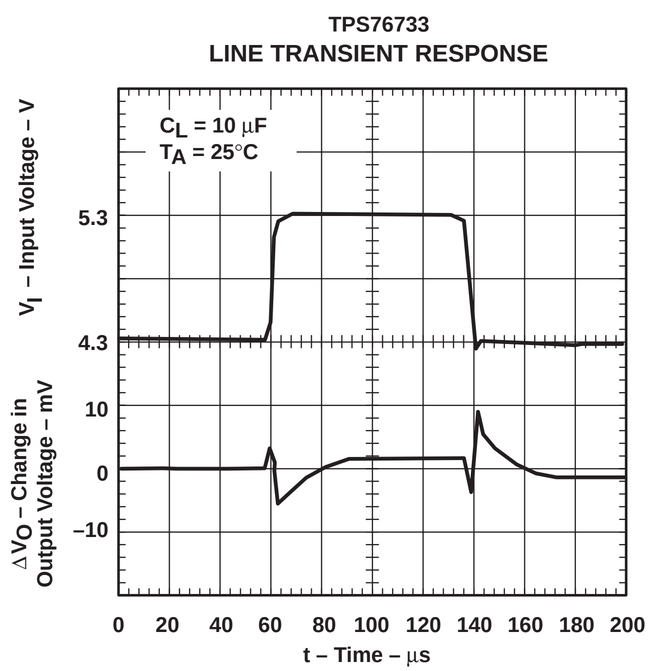


Figure 16

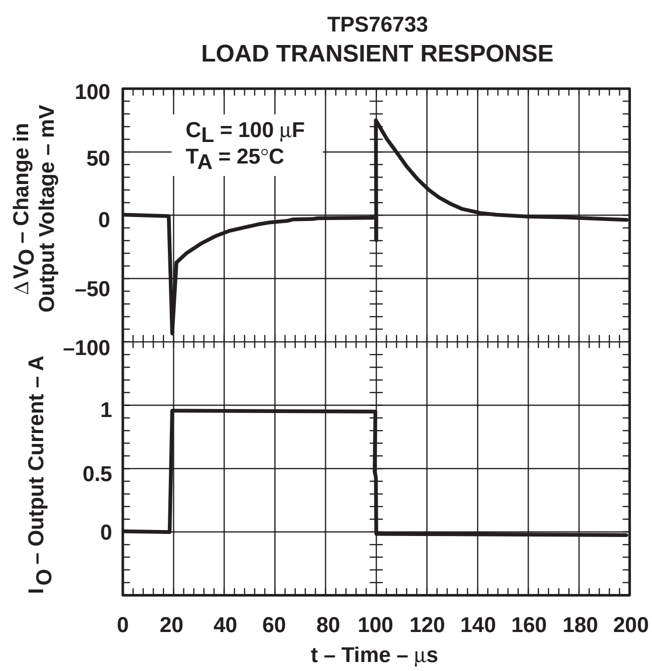


Figure 17

TYPICAL CHARACTERISTICS

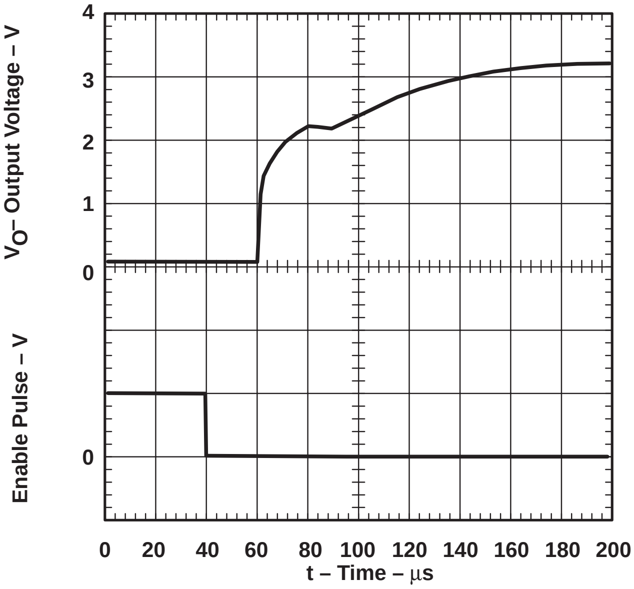


Figure 18

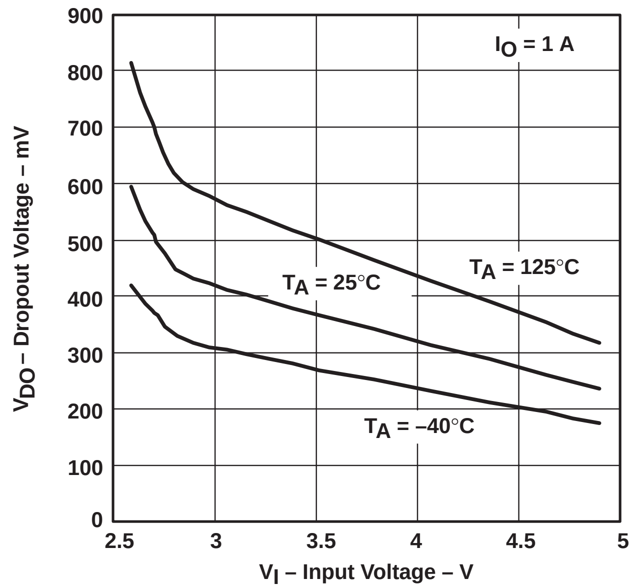


Figure 19

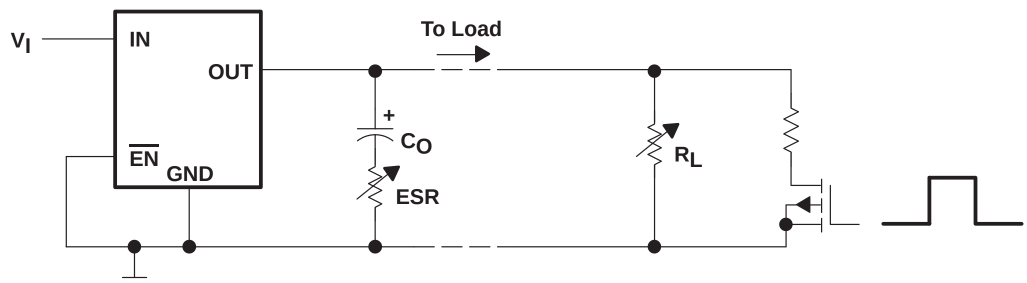


Figure 20. Test Circuit for Typical Regions of Stability (Figures 21 through 24) (Fixed Output Options)

TYPICAL CHARACTERISTICS

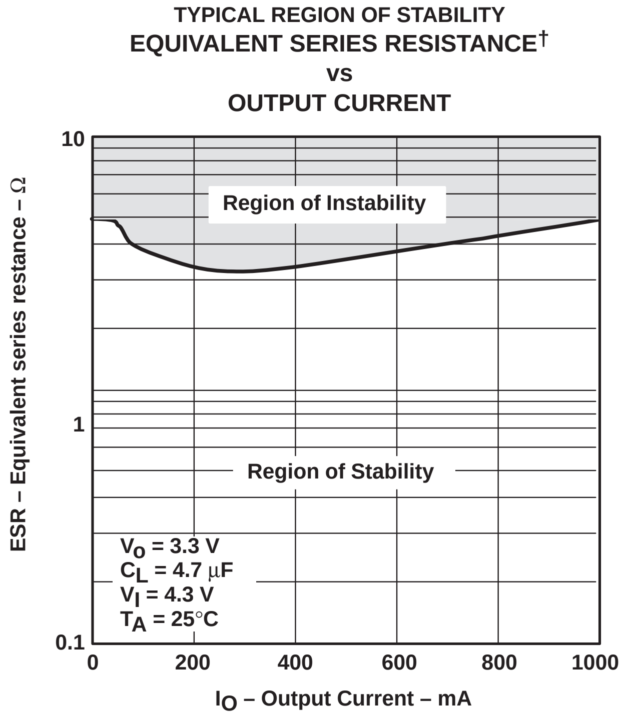


Figure 21

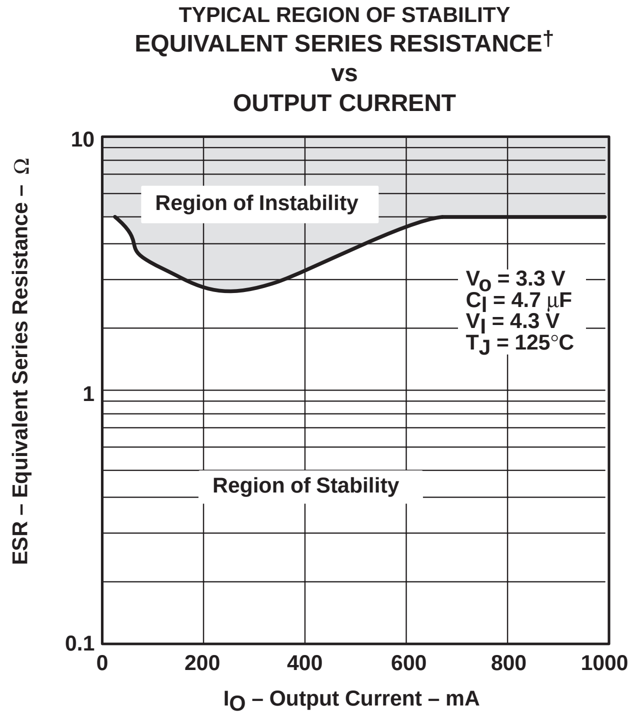


Figure 22

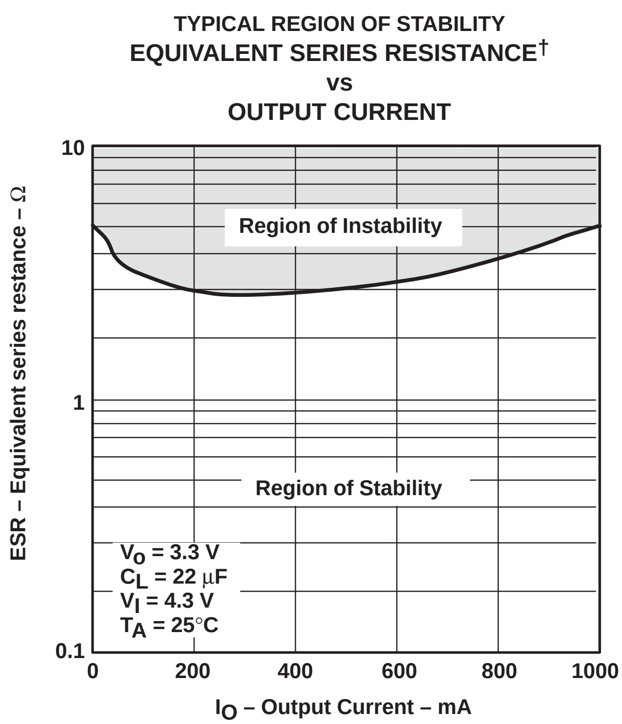


Figure 23

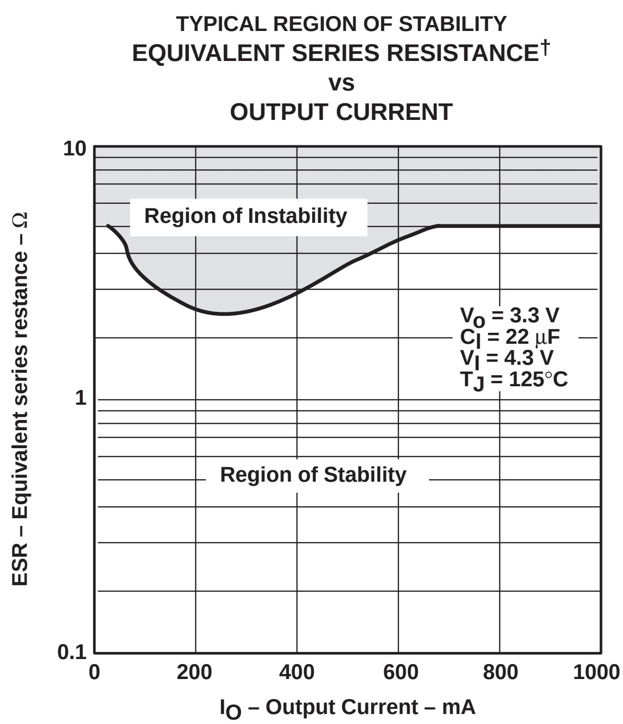


Figure 24

† Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O.

APPLICATION INFORMATION

The TPS767xx family includes eight fixed-output voltage regulators (1.5 V, 1.8 V, 2.5 V, 2.7 V, 2.8 V, 3.0 V, 3.3 V, and 5.0 V), and an adjustable regulator, the TPS76701 (adjustable from 1.5 V to 5.5 V).

device operation

The TPS767xx features very low quiescent current, which remains virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). The TPS767xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range.

Another pitfall associated with the pnp-pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 2 μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically reestablished in 120 μs.

minimum load requirements

The TPS767xx family is stable even at zero load; no minimum load is required for operation.

FB - pin connection (adjustable version only)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option . The output voltage is sensed through a resistor divider network to close the loop as it is shown in Figure 26. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (0.047 μF or larger) improves load transient response and noise rejection if the TPS767xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10 μF and the ESR (equivalent series resistance) must be between 50 mΩ and 1.5 Ω. Capacitor values 10 μF or larger are acceptable, provided the ESR is less than 1.5 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 10 μF surface-mount ceramic capacitors, including devices from Sprague and Kemet, meet the ESR requirements stated above.

APPLICATION INFORMATION

external capacitor requirements (continued)

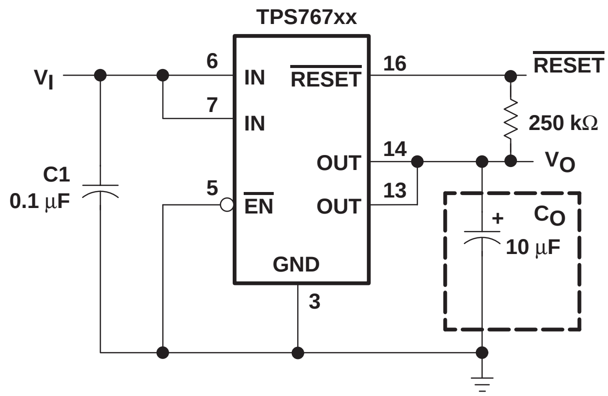


Figure 25. Typical Application Circuit (Fixed Versions)

programming the TPS76701 adjustable LDO regulator

The output voltage of the TPS76701 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

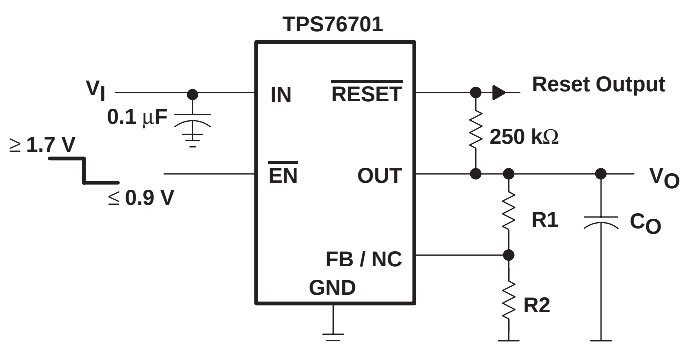
$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{1}$$

Where

V_{ref} = 1.1834 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \tag{2}$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	UNIT
2.5 V	33.2	30.1	kΩ
3.3 V	53.6	30.1	kΩ
3.6 V	61.9	30.1	kΩ
4.75 V	90.8	30.1	kΩ

Figure 26. TPS76701 Adjustable LDO Regulator Programming

APPLICATION INFORMATION

reset indicator

The TPS767xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator. $\overline{\text{RESET}}$ does not assert itself when the regulated output voltage falls outside the specified 2% tolerance, but instead reports an output voltage low relative to its nominal regulated value (refer to timing diagram for start-up sequence).

regulator protection

The TPS767xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767xx also features internal current limiting and thermal protection. During normal operation, the TPS767xx limits output current to approximately 1.7 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C(typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where

$T_J max$ is the maximum allowable junction temperature

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC and 32.6°C/W for the 20-terminal PWP with no airflow.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

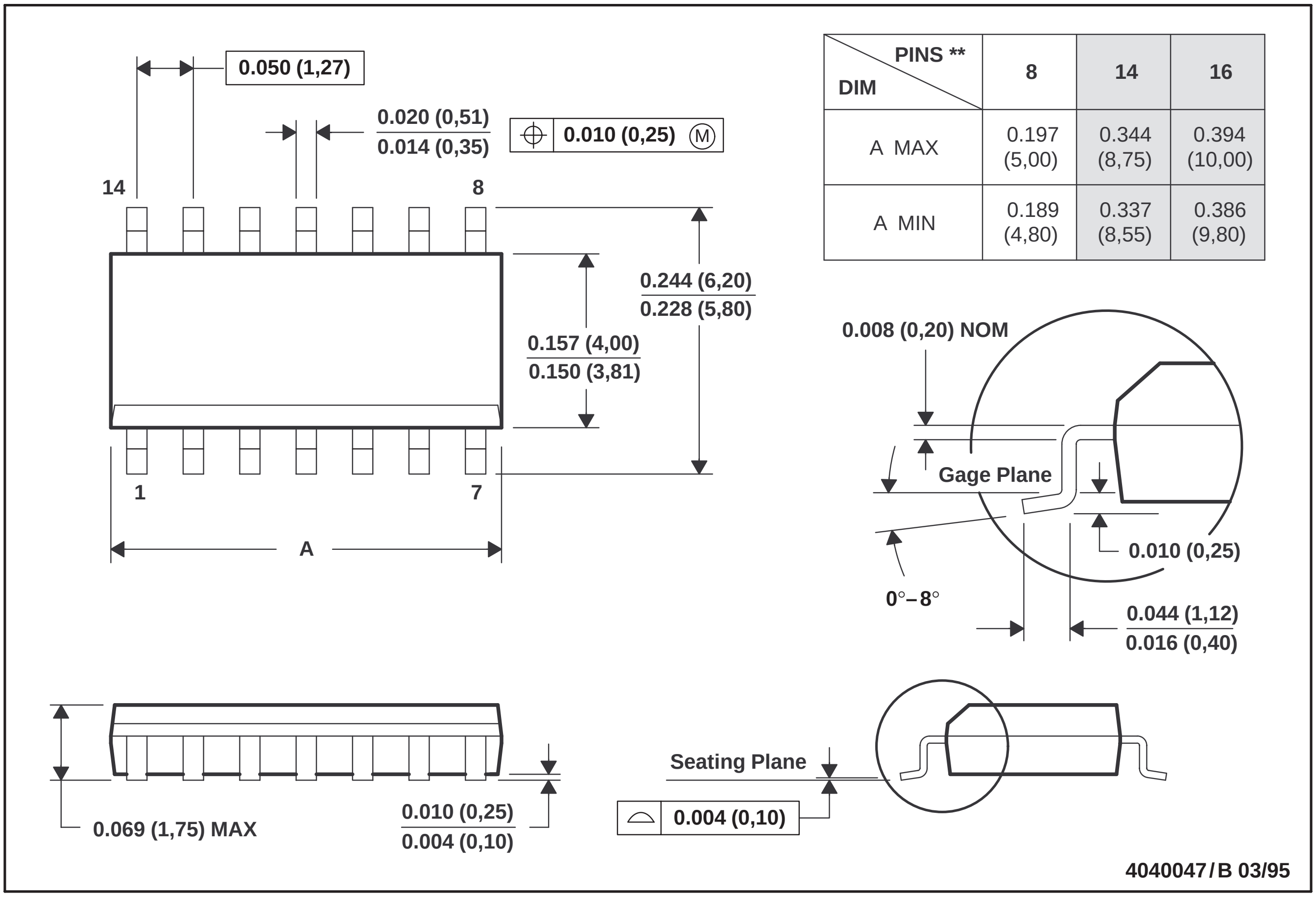
$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



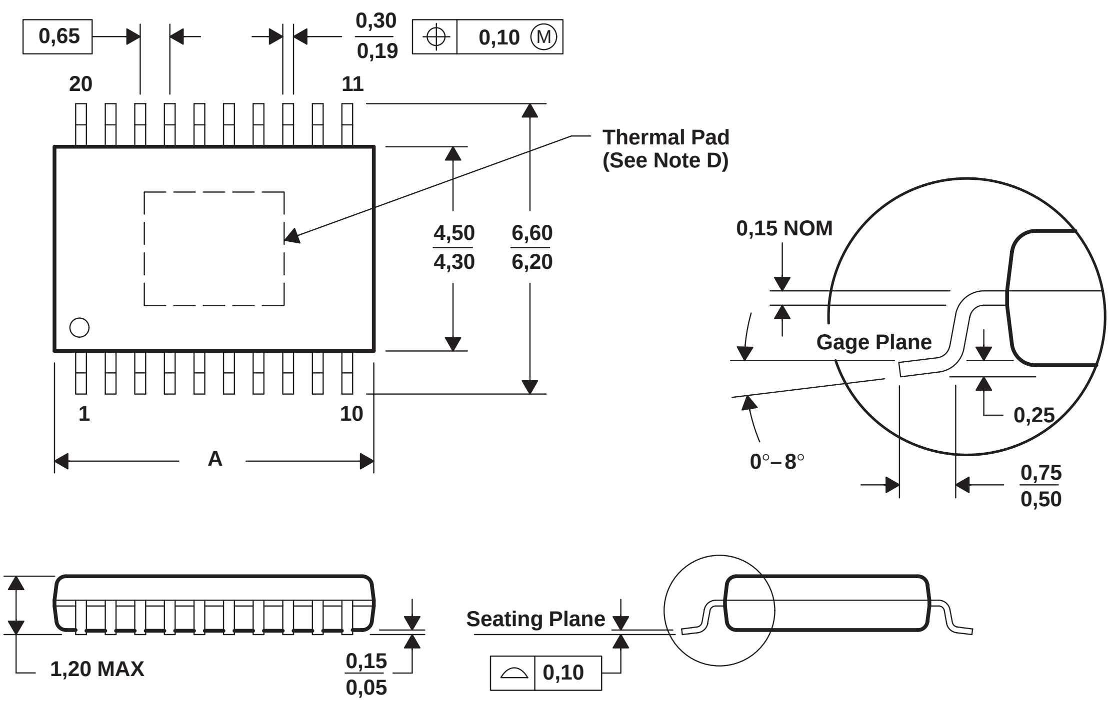
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad.
E. Falls within JEDEC MS-012

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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