

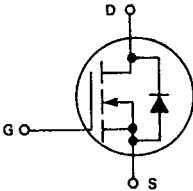
T-39-11

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Power Field Effect Transistor
N-Channel Enhancement-Mode
Silicon Gate TMOS

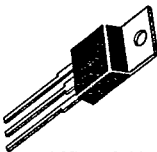
These TMOS Power FETs are designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads



IRF820
IRF821
IRF823

TMOS POWER FETs
2 and 2.5 AMPERES
 $r_{DS(on)} = 3 \text{ OHM}$
450 and 500 VOLTS
 $r_{DS(on)} = 4 \text{ OHM}$
450 VOLTS



CASE 221A-04
TO-220AB



MAXIMUM RATINGS

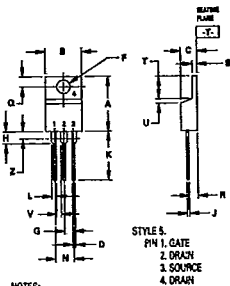
Rating	Symbol	IRF			Unit
		820	821	823	
Drain-Source Voltage	V_{DS}	500	450	450	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	500	450	450	Vdc
Gate-Source Voltage	V_{GS}	± 20			Vdc
Drain Current	I_D	2.5	2	8	Adc
	I_{DM}				
Continuous		10			
Pulsed					
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	40			Adc
		0.32			
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150			$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	3.12	$^\circ\text{C/W}$
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temp. for Soldering Purposes, 1/8" from Case for 5 Seconds	T_L	300	$^\circ\text{C}$

See the MTP3N45 Designer's Data Sheet for a complete set of design curves for the product on this data sheet.

OUTLINE DIMENSIONS



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	8.68	10.28	0.340	0.405
C	0.97	4.45	0.160	0.175
D	0.64	0.98	0.025	0.039
E	3.61	3.73	0.142	0.147
F	2.47	2.68	0.095	0.105
G	2.80	3.30	0.112	0.130
H	0.36	0.55	0.014	0.022
I	12.20	14.27	0.500	0.562
J	1.15	1.38	0.045	0.055
K	4.83	5.20	0.190	0.205
L	2.54	3.04	0.100	0.120
M	2.04	2.78	0.080	0.110
N	1.15	1.38	0.045	0.055
P	5.97	8.47	0.235	0.335
Q	0.91	1.27	0.035	0.050
R	1.15	—	0.045	—
S	—	2.04	—	0.080

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 0.25\text{ mA}$)	$V_{(BR)DSS}$	450 500	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}$, $V_{GS} = 0$, $T_J = 125^\circ\text{C}$)	I_{DSS}	—	0.25 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSF}	—	500	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\text{ Vdc}$, $V_{DS} = 0$)	I_{GSSR}	—	500	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 0.25\text{ mA}$)	$V_{GS(th)}$	2	4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$r_{DS(on)}$	—	3 4	Ohm
On-State Drain Current ($V_{GS} = 10\text{ V}$) ($V_{DS} \geq 7.5\text{ Vdc}$) ($V_{DS} \geq 8\text{ Vdc}$)	$I_{D(on)}$	2.5 2	—	Adc
Forward Transconductance ($V_{DS} \geq 7.5\text{ V}$, $I_D = 1\text{ A}$) ($V_{DS} \geq 8\text{ V}$, $I_D = 1\text{ A}$)	g_{FS}	1 1	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ V}$, $V_{GS} = 0$, $f = 1\text{ MHz})$	C_{iss}	—	400	pF
Output Capacitance		C_{oss}	—	150	
Reverse Transfer Capacitance		C_{rss}	—	40	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	$V_{DD} \approx 200\text{ V}$, $I_D = 1\text{ Apk}$, $R_{gen} = 50\text{ Ohms}$	$t_{d(on)}$	—	60	ns
Rise Time		t_r	—	50	
Turn-Off Delay Time		$t_{d(off)}$	—	60	
Fall Time		t_f	—	30	
Total Gate Charge	$(V_{GS} = 10\text{ V}$, $V_{DS} = 0.8 \times$ $\text{Rated } V_{DSS}$, $I_D = \text{Rated } I_D)$	Q_g	12 (Typ)	15	nC
Gate-Source Charge		Q_{gs}	6 (Typ)	—	
Gate-Drain Charge		Q_{gd}	6 (Typ)	—	

SOURCE-DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	$(I_S = \text{Rated } I_D$, $V_{GS} = 0)$	V_{SD}	—	1.5(1)	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	500 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_s	7.5 (Typ)	—	

*Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
(1) Add 0.1 V for IRF820 and IRF821.