MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range
  - 2.2 V to 3.6 V
    MSP430F543x, MSP430F541x
  - 1.8 V to 3.6 V
    MSP430F543xA, MSP430F541xA
- Ultralow Power Consumption
  - Active Mode (AM): 165 μA/MHz
  - Standby Mode (LPM3 RTC Mode): 2.6 μA
  - Off Mode (LPM4 RAM Retention): 1.6 μA
  - Shutdown Mode (LPM5): 0.1 μA
- Wake-Up From Standby Mode in Less Than 5 μs
- 16-Bit RISC Architecture
  - Extended Memory
  - Up to 18-MHz System Clock
    MSP430F543x, MSP430F541x
  - Up to 25-MHz System Clock
    MSP430F543xA, MSP430F541xA
- Flexible Power Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power/Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals
  - High-Frequency Crystals up to 25 MHz
- 16-Bit Timer0_A5 With Five Capture/Compare Registers
- 16-Bit Timer1_A3 With Three Capture/Compare Registers
- 16-Bit Timer_B7 With Seven Capture/Compare Shadow Registers
- Up to Four Universal Serial Communication Interfaces
  - Enhanced UART Supporting Auto-Baudrate Detection
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- 12-Bit Analog-to-Digital (A/D) Converter
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - 12 External Channels, 4 Internal Channels
- Hardware Multiplier Supporting 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three Channel Internal DMA
- Basic Timer With Real Time Clock Feature
- Family Members Include:
  - MSP430F5438, MSP430F5438A (1)
    - 256KB+512B Flash Memory
    - 16KB RAM
    - Four Universal Serial Communication Interfaces
  - MSP430F5436, MSP430F5436A (1)
    - 192KB+512B Flash Memory
    - 16KB RAM
    - Four Universal Serial Communication Interfaces
  - MSP430F5419 (1), MSP430F5419A (1)
    - 128KB+512B Flash Memory
    - 16KB RAM
    - Four Universal Serial Communication Interfaces
  - MSP430F5437 (1), MSP430F5437A (1)
    - 256KB+512B Flash Memory
    - 16KB RAM
    - Two Universal Serial Communication Interfaces

(1) Product Preview

PRODUCT PREVIEW

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- **MSP430F5435 (1), MSP430F5435A (1)**
  - **192KB+512B Flash Memory**
  - **16KB RAM**
  - **Two Universal Serial Communication Interfaces**
- **MSP430F5418 (1), MSP430F5418A (1)**
  - **128KB+512B Flash Memory**
  - **16KB RAM**
  - **Two Universal Serial Communication Interfaces**
- **For Complete Module Descriptions, See the *MSP430x5xx Family User's Guide* (SLAU208)**

DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 5 µs.

The MSP430F543x(A) and MSP430F541x(A) series are microcontroller configurations with three 16-bit timers, a high performance 12-bit analog-to-digital (A/D) converter, up to four universal serial communication interfaces (USCI), hardware multiplier, DMA, real time clock module with alarm capabilities, and up to 87 I/O pins.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

PRODUCT PREVIEW

ORDERING INFORMATION(1)

T_A	PACKAGED DEVICES(2)	
	PLASTIC 100-PIN TQFP (PZ)	PLASTIC 80-PIN TQFP (PN)
–40°C to 85°C	MSP430F5438IPZ	MSP430F5437IPN(3)
	MSP430F5436IPZ	MSP430F5435IPN(3)
	MSP430F5419IPZ(3)	MSP430F5418IPN(3)
	MSP430F5438AIPZ(3)	MSP430F5437AIPN(3)
	MSP430F5436AIPZ(3)	MSP430F5435AIPN(3)
	MSP430F5419AIPZ(3)	MSP430F5418AIPN(3)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/package.
(3) Product Preview

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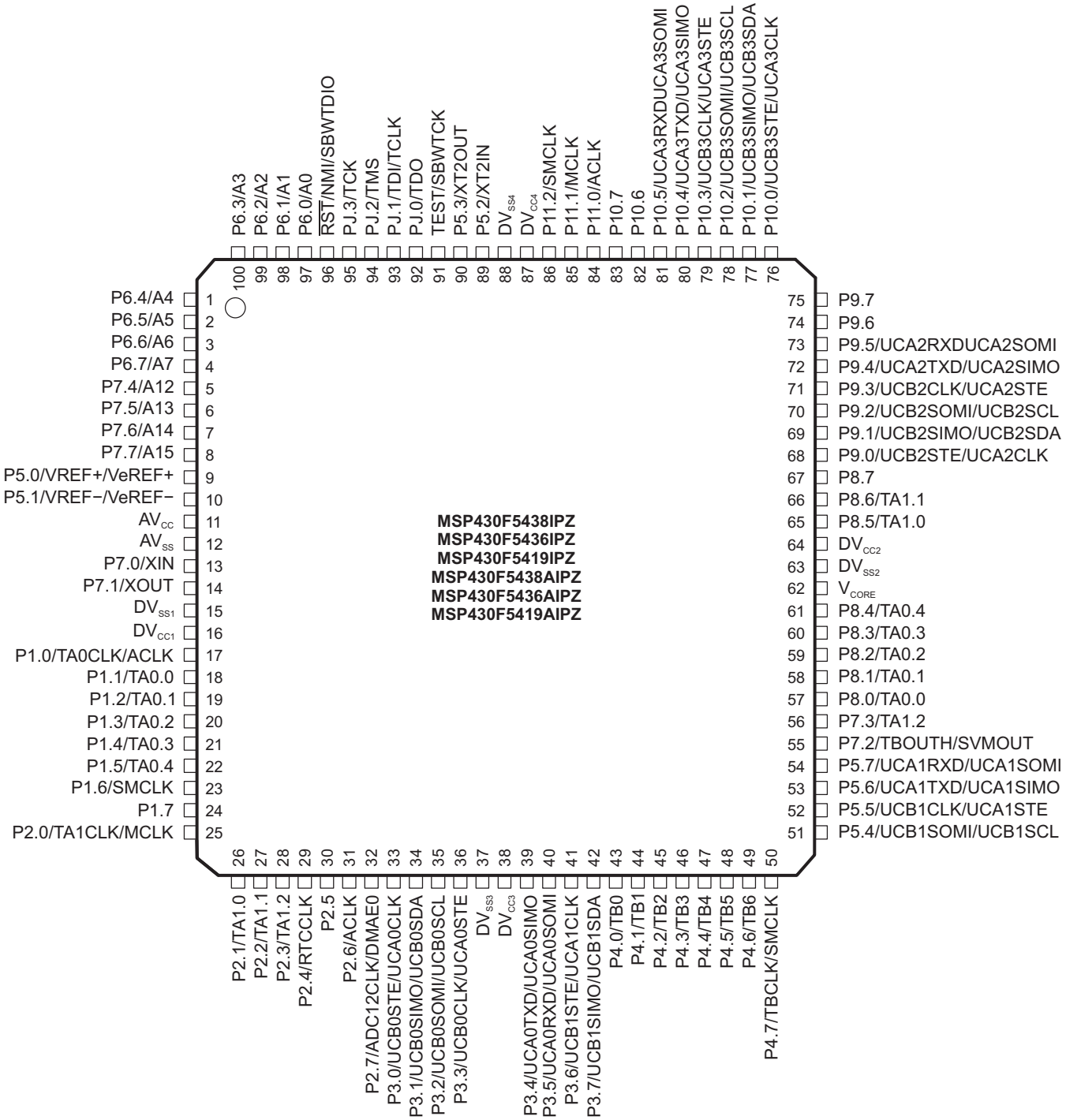
Pin Designation, MSP430F5438(A)IPZ, MSP430F5436(A)IPZ, MSP430F5419(A)IPZ

PZ PACKAGE
(TOP VIEW)



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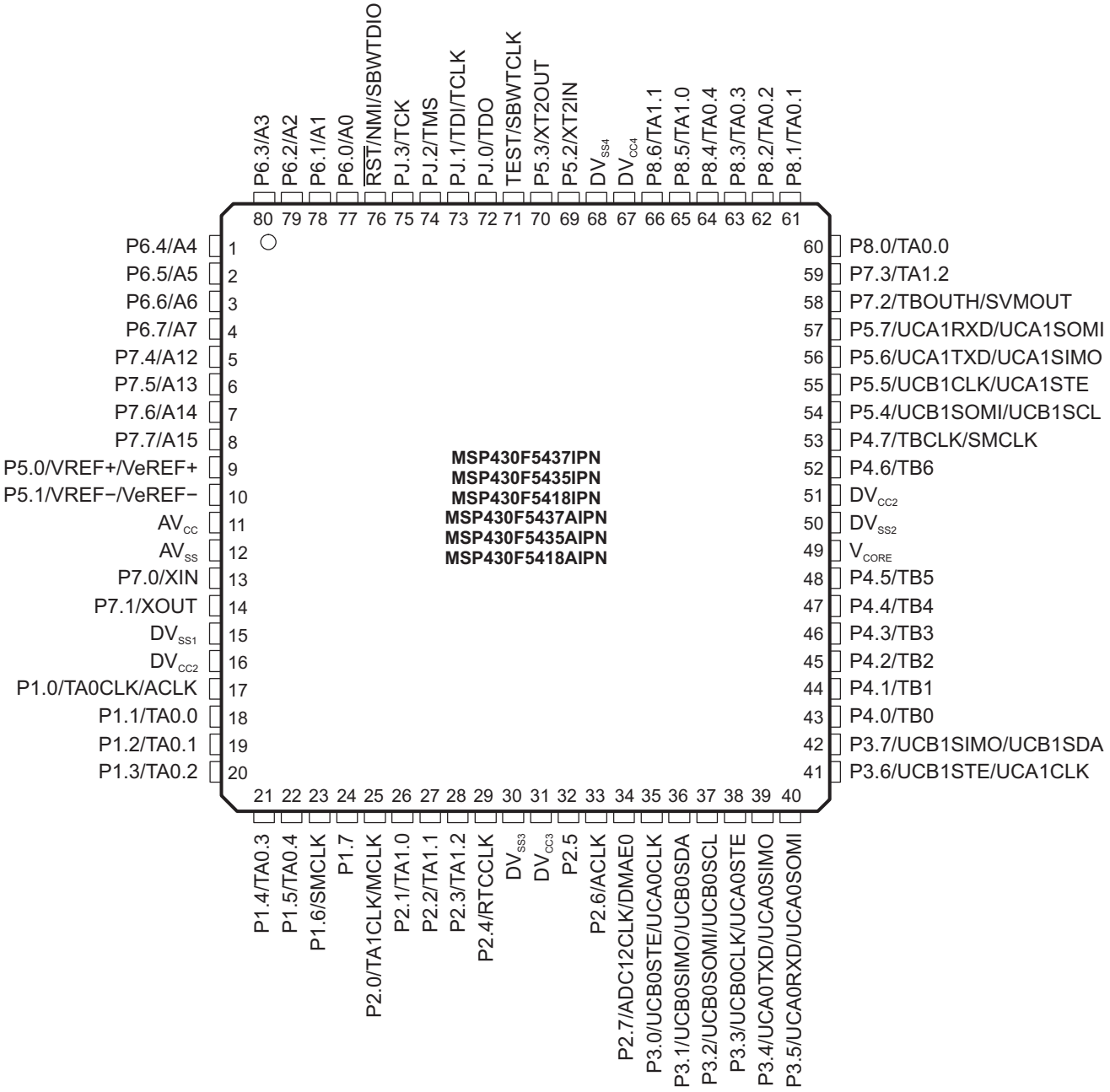
Pin Designation, MSP430F5437(A)IPN, MSP430F5435(A)IPN, MSP430F5418(A)IPN

PN PACKAGE
(TOP VIEW)



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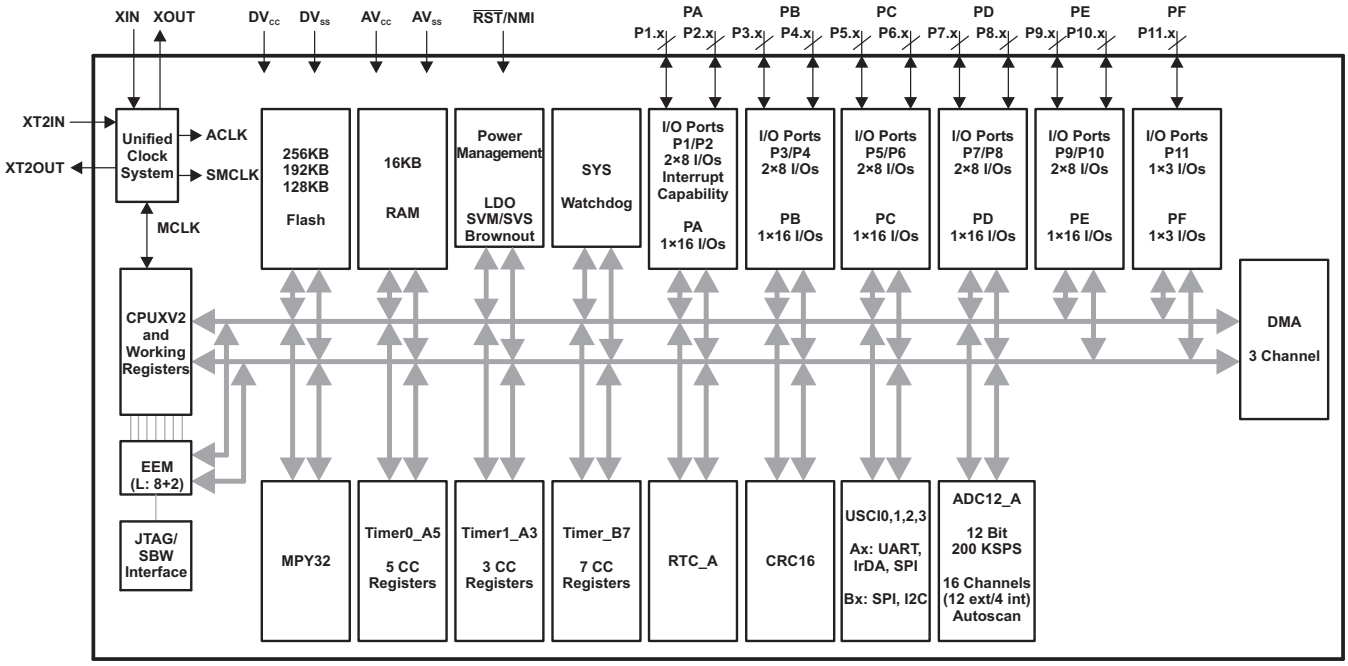
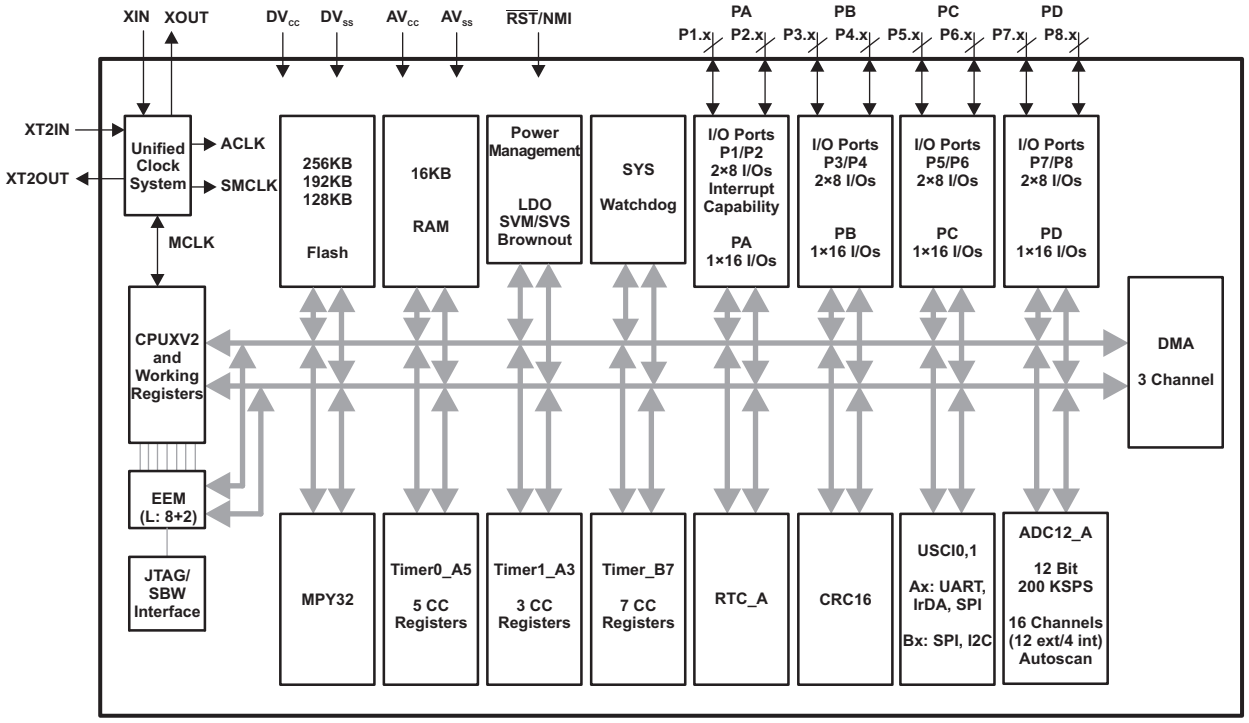
Functional Block Diagram, MSP430F5438(A)IPZ, MSP430F5436(A)IPZ, MSP430F5419(A)IPZ



Functional Block Diagram, MSP430F5437(A)IPN, MSP430F5435(A)IPN, MSP430F5418(A)IPN



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TERMINAL FUNCTIONS

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	PN		
P6.4/A4	1	1	I/O	General-purpose digital I/O Analog input A4 – ADC
P6.5/A5	2	2	I/O	General-purpose digital I/O Analog input A5 – ADC
P6.6/A6	3	3	I/O	General-purpose digital I/O Analog input A6 – ADC
P6.7/A7	4	4	I/O	General-purpose digital I/O Analog input A7 – ADC
P7.4/A12	5	5	I/O	General-purpose digital I/O Analog input A12 –ADC
P7.5/A13	6	6	I/O	General-purpose digital I/O Analog input A13 – ADC
P7.6/A14	7	7	I/O	General-purpose digital I/O Analog input A14 – ADC
P7.7/A15	8	8	I/O	General-purpose digital I/O Analog input A15 – ADC
P5.0/VREF+/VeREF+	9	9	I/O	General-purpose digital I/O Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P5.1/VREF-/VeREF-	10	10	I/O	General-purpose digital I/O Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
AV_{CC}	11	11		Analog power supply
AV_{SS}	12	12		Analog ground supply
P7.0/XIN	13	13	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P7.1/XOUT	14	14	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
DV_{SS1}	15	15		Digital ground supply
DV_{CC1}	16	16		Digital power supply
P1.0/TA0CLK/ACLK	17	17	I/O	General-purpose digital I/O with port interrupt Timer0_A5 clock signal TACLK input ACLK output (divided by 1, 2, 4, or 8)
P1.1/TA0.0	18	18	I/O	General-purpose digital I/O with port interrupt Timer0_A5 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	19	19	I/O	General-purpose digital I/O with port interrupt Timer0_A5 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	20	20	I/O	General-purpose digital I/O with port interrupt Timer0_A5 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	21	21	I/O	General-purpose digital I/O with port interrupt Timer0_A5 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	22	22	I/O	General-purpose digital I/O with port interrupt Timer0_A5 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/SMCLK	23	23	I/O	General-purpose digital I/O with port interrupt SMCLK output
P1.7	24	24	I/O	General-purpose digital I/O with port interrupt
P2.0/TA1CLK/MCLK	25	25	I/O	General-purpose digital I/O with port interrupt Timer1_A3 clock signal TA1CLK input MCLK output
P2.1/TA1.0	26	26	I/O	General-purpose digital I/O with port interrupt Timer1_A3 CCR0 capture: CCI0A input, compare: Out0 output

(1) I = input, O = output, N/A = not available on this package offering

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TERMINAL FUNCTIONS (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.			
	PZ	PN		
P2.2/TA1.1	27	27	I/O	General-purpose digital I/O with port interrupt Timer1_A3 CCR1 capture: CCI1A input, compare: Out1 output
P2.3/TA1.2	28	28	I/O	General-purpose digital I/O with port interrupt Timer1_A3 CCR2 capture: CCI2A input, compare: Out2 output
P2.4/RTCCLK	29	29	I/O	General-purpose digital I/O with port interrupt RTCCLK output
P2.5	30	32	I/O	General-purpose digital I/O with port interrupt
P2.6/ACLK	31	33	I/O	General-purpose digital I/O with port interrupt ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P2.7/ADC12CLK/DMAE0	32	34	I/O	General-purpose digital I/O with port interrupt Conversion clock input ADC DMA external trigger input
P3.0/UCB0STE/UCA0CLK	33	35	I/O	General-purpose digital I/O Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.1/UCB0SIMO/UCB0SDA	34	36	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode
P3.2/UCB0SOMI/UCB0SCL	35	37	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode
P3.3/UCB0CLK/UCA0STE	36	38	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
DV_{SS3}	37	30		Digital ground supply
DV_{CC3}	38	31		Digital power supply
P3.4/UCA0TXD/UCA0SIMO	39	39	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.5/UCA0RXD/UCA0SOMI	40	40	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P3.6/UCB1STE/UCA1CLK	41	41	I/O	General-purpose digital I/O Slave transmit enable – USCI_B1 SPI mode Clock signal input – USCI_A1 SPI slave mode Clock signal output – USCI_A1 SPI master mode
P3.7/UCB1SIMO/UCB1SDA	42	42	I/O	General-purpose digital I/O Slave in, master out – USCI_B1 SPI mode I2C data – USCI_B1 I2C mode
P4.0/TB0	43	43	I/O	General-purpose digital I/O Timer_B7 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P4.1/TB1	44	44	I/O	General-purpose digital I/O Timer_B7 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P4.2/TB2	45	45	I/O	General-purpose digital I/O Timer_B7 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P4.3/TB3	46	46	I/O	General-purpose digital I/O Timer_B7 capture CCR3: CCI3A/CCI3B input, compare: Out3 output
P4.4/TB4	47	47	I/O	General-purpose digital I/O Timer_B7 capture CCR4: CCI4A/CCI4B input, compare: Out4 output
P4.5/TB5	48	48	I/O	General-purpose digital I/O Timer_B7 capture CCR5: CCI5A/CCI5B input, compare: Out5 output
P4.6/TB6	49	52	I/O	General-purpose digital I/O Timer_B7 capture CCR6: CCI6A/CCI6B input, compare: Out6 output

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TERMINAL FUNCTIONS (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.			
	PZ	PN		
P4.7/TBCLK/SMCLK	50	53	I/O	General-purpose digital I/O Timer_B7 clock input SMCLK output
P5.4/UCB1SOMI/UCB1SCL	51	54	I/O	General-purpose digital I/O Slave out, master in – USCI_B1 SPI mode I2C clock – USCI_B1 I2C mode
P5.5/UCB1CLK/UCA1STE	52	55	I/O	General-purpose digital I/O Clock signal input – USCI_B1 SPI slave mode Clock signal output – USCI_B1 SPI master mode Slave transmit enable – USCI_A1 SPI mode
P5.6/UCA1TXD/UCA1SIMO	53	56	I/O	General-purpose digital I/O Transmit data – USCI_A1 UART mode Slave in, master out – USCI_A1 SPI mode
P5.7/UCA1RXD/UCA1SOMI	54	57	I/O	General-purpose digital I/O Receive data – USCI_A1 UART mode Slave out, master in – USCI_A1 SPI mode
P7.2/TBOUTH/SVMOUT	55	58	I/O	General-purpose digital I/O Switch all PWM outputs high impedance – Timer_B SVM output
P7.3/TA1.2	56	59	I/O	General-purpose digital I/O Timer1_A3 CCR2 capture: CCI2B input, compare: Out2 output
P8.0/TA0.0	57	60	I/O	General-purpose digital I/O Timer0_A5 CCR0 capture: CCI0B input, compare: Out0 output
P8.1/TA0.1	58	61	I/O	General-purpose digital I/O Timer0_A5 CCR1 capture: CCI1B input, compare: Out1 output
P8.2/TA0.2	59	62	I/O	General-purpose digital I/O Timer0_A5 CCR2 capture: CCI2B input, compare: Out2 output
P8.3/TA0.3	60	63	I/O	General-purpose digital I/O Timer0_A5 CCR3 capture: CCI3B input, compare: Out3 output
P8.4/TA0.4	61	64	I/O	General-purpose digital I/O Timer0_A5 CCR4 capture: CCI4B input, compare: Out4 output
V_{CORE}	62	49		Regulated core power supply
DV_{SS2}	63	50		Digital ground supply
DV_{CC2}	64	51		Digital power supply
P8.5/TA1.0	65	65	I/O	General-purpose digital I/O Timer1_A3 CCR0 capture: CCI0B input, compare: Out0 output
P8.6/TA1.1	66	66	I/O	General-purpose digital I/O Timer1_A3 CCR1 capture: CCI1B input, compare: Out1 output
P8.7	67	N/A	I/O	General-purpose digital I/O
P9.0/UCB2STE/UCA2CLK	68	N/A	I/O	General-purpose digital I/O Slave transmit enable – USCI_B2 SPI mode Clock signal input – USCI_A2 SPI slave mode Clock signal output – USCI_A2 SPI master mode
P9.1/UCB2SIMO/UCB2SDA	69	N/A	I/O	General-purpose digital I/O Slave in, master out – USCI_B2 SPI mode I2C data – USCI_B2 I2C mode
P9.2/UCB2SOMI/UCB2SCL	70	N/A	I/O	General-purpose digital I/O Slave out, master in – USCI_B2 SPI mode I2C clock – USCI_B2 I2C mode
P9.3/UCB2CLK/UCA2STE	71	N/A	I/O	General-purpose digital I/O Clock signal input – USCI_B2 SPI slave mode Clock signal output – USCI_B2 SPI master mode Slave transmit enable – USCI_A2 SPI mode

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TERMINAL FUNCTIONS (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	PN		
P9.4/UCA2TXD/UCA2SIMO	72	N/A	I/O	General-purpose digital I/O Transmit data – USCI_A2 UART mode Slave in, master out – USCI_A2 SPI mode
P9.5/UCA2RXD/UCA2SOMI	73	N/A	I/O	General-purpose digital I/O Receive data – USCI_A2 UART mode Slave out, master in – USCI_A2 SPI mode
P9.6	74	N/A	I/O	General-purpose digital I/O
P9.7	75	N/A	I/O	General-purpose digital I/O
P10.0/UCB3STE/UCA3CLK	76	N/A	I/O	General-purpose digital I/O Slave transmit enable – USCI_B3 SPI mode Clock signal input – USCI_A3 SPI slave mode Clock signal output – USCI_A3 SPI master mode
P10.1/UCB3SIMO/UCB3SDA	77	N/A	I/O	General-purpose digital I/O Slave in, master out – USCI_B3 SPI mode I2C data – USCI_B3 I2C mode
P10.2/UCB3SOMI/UCB3SCL	78	N/A	I/O	General-purpose digital I/O Slave out, master in – USCI_B3 SPI mode I2C clock – USCI_B3 I2C mode
P10.3/UCB3CLK/UCA3STE	79	N/A	I/O	General-purpose digital I/O Clock signal input – USCI_B3 SPI slave mode Clock signal output – USCI_B3 SPI master mode Slave transmit enable – USCI_A3 SPI mode
P10.4/UCA3TXD/UCA3SIMO	80	N/A	I/O	General-purpose digital I/O Transmit data – USCI_A3 UART mode Slave in, master out – USCI_A3 SPI mode
P10.5/UCA3RXD/UCA3SOMI	81	N/A	I/O	General-purpose digital I/O Receive data – USCI_A3 UART mode Slave out, master in – USCI_A3 SPI mode
P10.6	82	N/A	I/O	General-purpose digital I/O
P10.7	83	N/A	I/O	General-purpose digital I/O
P11.0/ACLK	84	N/A	I/O	General-purpose digital I/O ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P11.1/MCLK	85	N/A	I/O	General-purpose digital I/O MCLK output
P11.2/SMCLK	86	N/A	I/O	General-purpose digital I/O SMCLK output
DV_{CC4}	87	67		Digital power supply
DV_{SS4}	88	68		Digital ground supply
P5.2/XT2IN	89	69	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	90	70	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK	91	71	I	Test mode pin – select digital I/O on JTAG pins Spy-bi-wire input clock
PJ.0/TDO	92	72	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	93	73	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/TMS	94	74	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	95	75	I/O	General-purpose digital I/O Test clock
$\overline{RST}$/NMI/SBWTDIO	96	76	I/O	Reset input active low Non-maskable interrupt input Spy-bi-wire data input/output

PRODUCT PREVIEW

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TERMINAL FUNCTIONS (continued)

TERMINAL			I/O[1]	DESCRIPTION
NAME	NO.			
	PZ	PN		
P6.0/A0	97	77	I/O	General-purpose digital I/O Analog input A0 – ADC
P6.1/A1	98	78	I/O	General-purpose digital I/O Analog input A1 – ADC
P6.2/A2	99	79	I/O	General-purpose digital I/O Analog input A2 – ADC
P6.3/A3	100	80	I/O	General-purpose digital I/O Analog input A3 – ADC

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SHORT-FORM DESCRIPTION

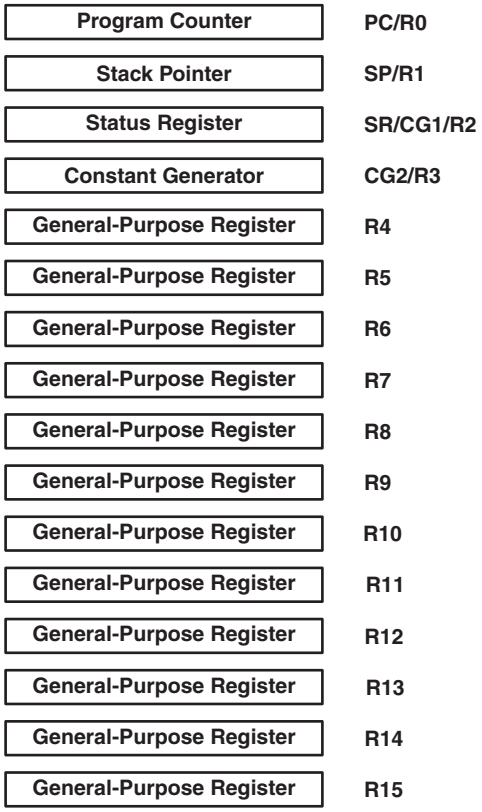
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 → R5
Single operands, destination only	e.g., CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	+	+	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	+	+	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	+	+	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	+	+	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	+		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	+		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	+		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

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Operating Modes

The MSP430 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 5 (LPM5)
  - Internal regulator disabled
  - No data retention
  - Wakeup from $\overline{\text{RST}}$/NMI

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Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG (SYSUNIV)(1)(2)	(Non)maskable	0FFFAh	61
Timer_B7	TBCCR0 CCIFG0 (3)	Maskable	0FFF8h	60
Timer_B7	TBCCR1 CCIFG1 ... TBCCR6 CCIFG6, TBIFG (TBIV)(1)(3)	Maskable	0FFF6h	59
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF4h	58
USCI_A0 Receive/Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(3)	Maskable	0FFF2h	57
USCI_B0 Receive/Transmit	UCB0RXIFG, UCB0TXIFG (UCAB0IV)(1)(3)	Maskable	0FFF0h	56
ADC12_A	ADC12IFG0 ... ADC12IFG15 (ADC12IV)(1)(3)	Maskable	0FFEEh	55
Timer0_A5	TA0CCR0 CCIFG0(3)	Maskable	0FFECh	54
Timer0_A5	TA0CCR1 CCIFG1 ... TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1)(3)	Maskable	0FFEAh	53
USCI_A2 Receive/Transmit	UCA2RXIFG, UCA2TXIFG (UCA2IV)(1)(3)	Maskable	0FFE8h	52
USCI_B2 Receive/Transmit	UCB2RXIFG, UCB2TXIFG (UCB2IV)(1)(3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)(3)	Maskable	0FFE4h	50
Timer1_A3	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
Timer1_A3	TA1CCR1 CCIFG1 ... TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1)(3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)(3)	Maskable	0FFDEh	47
USCI_A1 Receive/Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(3)	Maskable	0FFDCh	46
USCI_B1 Receive/Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1)(3)	Maskable	0FFDAh	45
USCI_A3 Receive/Transmit	UCA3RXIFG, UCA3TXIFG (UCA3IV)(1)(3)	Maskable	0FFD8h	44
USCI_B3 Receive/Transmit	UCB3RXIFG, UCB3TXIFG (UCB3IV)(1)(3)	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)(3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)(3)	Maskable	0FFD2h	41
Reserved	Reserved(4)		0FFD2h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

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Special Function Registers (SFRs)

The MSP430 SFRs are located in the lowest address space and can be accessed via word or byte formats.

Legend	**rw:**	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
	rw-[0,1]:	Bit can be read and written. It is reset or set by BOR.
	–	SFR bit is not present in device.

Interrupt Enable 1

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
JMBOUTIE	**JMBINIE**	**ACCVIE**	**NMIIE**	**VMAIE**	–	**OFIE**	**WDTIE**
rw-0	rw-0	rw-0	rw-0	rw-0		rw-0	rw-0

WDTIE	Watchdog-timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as a general-purpose timer.
OFIE	Oscillator-fault-interrupt enable
VMAIE	Vacant memory access interrupt enable
NMIIE	Nonmaskable-interrupt enable
ACCVIE	Flash access violation interrupt enable
JMBINIE	JTAG mailbox input interrupt enable
JMBOUTIE	JTAG mailbox output interrupt enable

Interrupt Flag 1

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
JMBOUTIFG	**JMBINIFG**	–	**NMIIFG**	**VMAIFG**	–	**OFIFG**	**WDTIFG**
rw-[0]	rw-[0]		rw-0	rw-0		rw-0	rw-0

WDTIFG	Set on watchdog timer overflow (in watchdog mode) or security key violation Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode
OFIFG	Flag set on oscillator fault
VMAIFG	Set on vacant memory access
NMIIFG	Set via $\overline{RST}$/NMI pin
JMBINIFG	Set on JTAG mailbox input message
JMBOUTIFG	Set on JTAG mailbox output register ready for next message

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Memory Organization

		MSP430F5419 MSP430F5419A	MSP430F5436 MSP430F5436A	MSP430F5438 MSP430F5438A
Memory Main: interrupt vector Main: code memory	Size Flash Flash	128KB 00FFFFh–00FF80h 025BFFh–005C00h	192KB 00FFFFh–00FF80h 035BFFh–005C00h	256KB 00FFFFh–00FF80h 045BFFh–005C00h
RAM	Size	16KB	16KB	16KB
	Sector 3	005BFFh–004C00h	005BFFh–004C00h	005BFFh–004C00h
	Sector 2	004BFFh–003C00h	004BFFh–003C00h	004BFFh–003C00h
	Sector 1	003BFFh–002C00h	003BFFh–002C00h	003BFFh–002C00h
	Sector 0	002BFFh–001C00h	002BFFh–001C00h	002BFFh–001C00h
Information memory	Size Flash	512 Byte 0019FFh–001800h	512 Byte 0019FFh–001800h	512 Byte 0019FFh–001800h
Bootstrap loader (BSL) memory	Size Flash	2KB 0017FFh–001000h	2KB 0017FFh–001000h	2KB 0017FFh–001000h
Peripherals	Size Flash	4KB 000FFFh–000000h	4KB 000FFFh–000000h	4KB 000FFFh–000000h

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. A bootstrap loader security key is provided at address TBD to disable the BSL completely or to disable the erasure of the flash if an invalid password is supplied. For complete description of the features of the BSL and its implementation, see the application report *Features of the MSP430 Bootstrap Loader*, TI literature number SLAA089.

BSL KEY	DESCRIPTION
00000h	Erasure of flash disabled if an invalid password is supplied
0AA55h	BSL disabled
any other value	BSL enabled

BSL FUNCTION	PZ PACKAGE PINS	PN PACKAGE PINS
Data transmit	18 – P1.1	18 – P1.1
Data receive	19 – P1.2	19 – P1.2

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0–n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sector of 4K bytes each.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

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Peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x5xx Family User's Guide*, literature number SLAU208.

Digital I/O

There are up to ten 8-bit I/O ports implemented: For 100 pin options, P1 through P10 are complete. P11 contains three individual I/O ports.For 80 pin options, P1 through P7 are complete. P8 contains seven individual I/O ports. P9 through P11 do not exist. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P11) or word-wise in pairs (PA through PF).

Oscillator and System Clock

The clock system in the MSP430x5xx family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32 kHz watch crystal oscillator (XT1 LF mode), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator (XT1 HF mode or XT2). The UCS module is designed to meet the requirements of both low system cost and low-power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in less than 5 μs. The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32 kHz watch crystal, a high-frequency crystal, the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

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Real-Time Clock (RTC_A)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

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Table 3. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV , System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	RST/NMI (POR)		04h	
	DoBOR (BOR)		06h	
	Reserved		08h	
	Reserved		0Ah	
	Security violation (BOR)		0Ch	
	SVSH (POR)		0Eh	
	SVML_OVP (POR)		10h	
	SVMH_OVP (POR)		12h	
	DoPOR (POR)		14h	
	WDT timeout (PUC)		16h	
	WDT key violation (PUC)		18h	
	KEYV flash key violation (PUC)		1Ah	
	FLL unlock (PUC)		1Ch	
	Peripheral area fetch (PUC)		1Eh	
	PMM key violation (PUC)		20h	
	Reserved		22h - 3Eh	Lowest
SYSSNIV , System NMI	No interrupt pending	019Ch	00h	
	SVMLIFG		02h	Highest
	SVMHIFG		04h	
	DLYLIFG		06h	
	DLYHIFG		08h	
	VMAIFG		0Ah	
	JMBINIFG		0Ch	
	JMBOUTIFG		0Eh	
	VLRLIFG		10h	
	VLRHIFG		12h	
	Reserved		14h - 1Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	ACCVIFG		06h	
	Reserved		06h - 1Eh	Lowest

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DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 4. DMA Trigger Assignments (1)

Trigger	Channel		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TBCCR0 CCIFG	TBCCR0 CCIFG	TBCCR0 CCIFG
6	TBCCR2 CCIFG	TBCCR2 CCIFG	TBCCR2 CCIFG
7	Reserved	Reserved	Reserved
8	Reserved	Reserved	Reserved
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx	ADC12IFGx	ADC12IFGx
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	Reserved	Reserved	Reserved
28	Reserved	Reserved	Reserved
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.

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Universal Serial Communication Interface (USCI)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART,or IrDA.

The USCI_Bn module provides support for SPI (3 or 4 pin) or I2C.

The MSP430F5438(A), MSP430F5436(A), and MSP430F5419(A) include four complete USCI modules (n = 0 to 3). The MSP430F5437(A), MSP430F5435(A), and MSP430F5418(A) include two complete USCI modules (n = 0 to 1).

Timer0_A5

Timer0_A5 is a 16-bit timer/counter with five capture/compare registers. Timer0_A5 can support multiple capture/compares, PWM outputs, and interval timing. Timer0_A5 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 5. Timer0_A5 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
17-P1.0	17-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
17-P1.0	17-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
18-P1.1	18-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	18-P1.1	18-P1.1
57-P8.0	60-P8.0	TA0.0	CCI0B				57-P8.0	60-P8.0
		DV_{SS}	GND				ADC12 (internal)	ADC12 (internal)
		DV_{CC}	V_{CC}					
19-P1.2	19-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	19-P1.2	19-P1.2
58-P8.1	59-P8.1	TA0.1	CCI1B				58-P8.1	59-P8.1
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
20-P1.3	20-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	20-P1.3	20-P1.3
59-P8.2	62-P8.2	TA0.2	CCI2B				59-P8.2	62-P8.2
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
21-P1.4	21-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	21-P1.4	21-P1.4
60-P8.3	63-P8.3	TA0.3	CCI3B				60-P8.3	63-P8.3
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
22-P1.5	22-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	22-P1.5	22-P1.5
61-P8.4	63-P8.4	TA0.4	CCI4B				61-P8.4	63-P8.4
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

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Timer1_A3

Timer1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer1_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer1_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6. Timer1_A3 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
25-P2.0	25-P2.0	TA1CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
25-P2.0	25-P2.0	TA1CLK	$\overline{\text{TACLK}}$					
26-P2.1	26-P2.1	TA1.0	CCI0A	CCR0	TA0	TA1.0	26-P2.1	26-P2.1
65-P8.5	65-P8.5	TA1.0	CCI0B				65-P8.5	65-P8.5
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
27-P2.2	27-P2.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	27-P2.2	27-P2.2
66-P8.6	66-P8.6	TA1.1	CCI1B				66-P8.6	66-P8.6
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
28-P2.3	28-P2.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	28-P2.3	28-P2.3
56-P7.3	59-P7.3	TA1.2	CCI2B				56-P7.3	59-P7.3
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

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Timer_B7

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 7. Timer_B7 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	PN						PZ	PN
50-P4.7	50-P4.7	TBCLK	TBCLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
50-P4.7	50-P4.7	TBCLK	$\overline{\text{TBCLK}}$					
43-P4.0	43-P4.0	TB0	CCI0A	CCR0	TB0	TB0	43-P4.0	43-P4.0
43-P4.0	43-P4.0	TB0	CCI0B				ADC12 (internal)	ADC12 (internal)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
44-P4.1	44-P4.1	TB1	CCI1A	CCR1	TB1	TB1	44-P4.1	44-P4.1
44-P4.1	44-P4.1	TB1	CCI1B				ADC12 (internal)	ADC12 (internal)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
45-P4.2	45-P4.2	TB2	CCI2A	CCR2	TB2	TB2	45-P4.2	45-P4.2
45-P4.2	45-P4.2	TB2	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
46-P4.3	46-P4.3	TB3	CCI3A	CCR3	TB3	TB3	46-P4.3	46-P4.3
46-P4.3	46-P4.3	TB3	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
47-P4.4	47-P4.4	TB4	CCI4A	CCR4	TB4	TB4	47-P4.4	47-P4.4
47-P4.4	47-P4.4	TB4	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
48-P4.5	48-P4.5	TB5	CCI5A	CCR5	TB5	TB5	48-P4.5	48-P4.5
48-P4.5	48-P4.5	TB5	CCI5B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
49-P4.6	52-P4.6	TB6	CCI6A	CCR6	TB6	TB6	49-P4.6	52-P4.6
		ACLK (internal)	CCI6B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

ADC12_A

The ADC12_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

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CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Peripheral File Map

Table 8. Peripherals

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Timer_B7	Timer_B7 interrupt vector	TBIV	03C0h	2Eh
	Timer_B7 expansion register 0	TBEX0		20h
	Capture/compare register 6	TBCCR6		1Eh
	Capture/compare register 5	TBCCR5		1Ch
	Capture/compare register 4	TBCCR4		1Ah
	Capture/compare register 3	TBCCR3		18h
	Capture/compare register 2	TBCCR2		16h
	Capture/compare register 1	TBCCR1		14h
	Capture/compare register 0	TBCCR0		12h
	Timer_B7 register	TBR		10h
	Capture/compare control 6	TBCCTL6		0Eh
	Capture/compare control 5	TBCCTL5		0Ch
	Capture/compare control 4	TBCCTL4		0Ah
	Capture/compare control 3	TBCCTL3		08h
	Capture/compare control 2	TBCCTL2		06h
	Capture/compare control 1	TBCCTL1		04h
	Capture/compare control 0	TBCCTL0		02h
	Timer_B7 control	TBCTL		00h
Timer0_A5	Timer0_A5 interrupt vector	TA0IV	0340h	2Eh
	Timer0_A5 expansion register 0	TA0EX0		20h
	Capture/compare register 4	TA0CCR4		1Ah
	Capture/compare register 3	TA0CCR3		18h
	Capture/compare register 2	TA0CCR2		16h
	Capture/compare register 1	TA0CCR1		14h
	Capture/compare register 0	TA0CCR0		12h
	Timer0_A5 register	TA0R		10h
	Capture/compare control 4	TA0CCTL4		0Ah
	Capture/compare control 3	TA0CCTL3		08h
	Capture/compare control 2	TA0CCTL2		06h
	Capture/compare control 1	TA0CCTL1		04h
	Capture/compare control 0	TA0CCTL0		02h
	Timer0_A5 control	TA0CTL		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Timer1_A3	Timer1_A3 interrupt vector	TA1IV	0380h	2Eh
	Timer1_A3 expansion register 0	TA1EX0		20h
	Capture/compare register 2	TA1CCR2		16h
	Capture/compare register 1	TA1CCR1		14h
	Capture/compare register 0	TA1CCR0		12h
	Timer1_A3 register	TA1R		10h
	Capture/compare control 2	TA1CCTL2		06h
	Capture/compare control 1	TA1CCTL1		04h
	Capture/compare control 0	TA1CCTL0		02h
	Timer1_A3 control	TA1CTL		00h
Hardware Multiplier	MPY32 control register 0	MPY32CTL0	04C0h	2Ch
	32 × 32 result 3 – most significant word	RES3		2Ah
	32 × 32 result 2	RES2		28h
	32 × 32 result 1	RES1		26h
	32 × 32 result 0 – least significant word	RES0		24h
	32-bit operand 2 – high word	OP2H		22h
	32-bit operand 2 – low word	OP2L		20h
	32-bit operand 1 – signed multiply accumulate high word	MACS32H		1Eh
	32-bit operand 1 – signed multiply accumulate low word	MACS32L		1Ch
	32-bit operand 1 – multiply accumulate high word	MAC32H		1Ah
	32-bit operand 1 – multiply accumulate low word	MAC32L		18h
	32-bit operand 1 – signed multiply high word	MPYS32H		16h
	32-bit operand 1 – signed multiply low word	MPYS32L		14h
	32-bit operand 1 – multiply high word	MPY32H		12h
	32-bit operand 1 – multiply low word	MPY32L		10h
	16 × 16 sum extension register	SUMEXT		0Eh
	16 × 16 result high word	RESHI		0Ch
	16 × 16 result low word	RESLO		0Ah
	16-bit operand 2	OP2		08h
	16-bit operand 1 – signed multiply accumulate	MACS		06h
	16-bit operand 1 – multiply accumulate	MAC		04h
	16-bit operand 1 – signed multiply	MPYS		02h
	16-bit operand 1 – multiply	MPY		00h
DMA Channel 2	DMA channel 2 transfer size	DMA2SZ	0530h	0Ah
	DMA channel 2 destination address high	DMA2DAH		08h
	DMA channel 2 destination address low	DMA2DAL		06h
	DMA channel 2 source address high	DMA2SAH		04h
	DMA channel 2 source address low	DMA2SAL		02h
	DMA channel 2 control	DMA2CTL		00h
DMA Channel 1	DMA channel 1 transfer size	DMA1SZ	0520h	0Ah
	DMA channel 1 destination address high	DMA1DAH		08h
	DMA channel 1 destination address low	DMA1DAL		06h
	DMA channel 1 source address high	DMA1SAH		04h
	DMA channel 1 source address low	DMA1SAL		02h
	DMA channel 1 control	DMA1CTL		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
DMA Channel 0	DMA channel 0 transfer size	DMA0SZ	0510h	0Ah
	DMA channel 0 destination address high	DMA0DAH		08h
	DMA channel 0 destination address low	DMA0DAL		06h
	DMA channel 0 source address high	DMA0SAH		04h
	DMA channel 0 source address low	DMA0SAL		02h
	DMA channel 0 control	DMA0CTL		00h
DMA	DMA interrupt vector	DMAIV	0500h	0Eh
	DMA module control 4	DMACTL4		08h
	DMA module control 3	DMACTL3		06h
	DMA module control 2	DMACTL2		04h
	DMA module control 1	DMACTL1		02h
	DMA module control 0	DMACTL0		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
ADC12_A	Conversion memory 15	ADC12MEM15	0700h	3Eh
	Conversion memory 14	ADC12MEM14		3Ch
	Conversion memory 13	ADC12MEM13		3Ah
	Conversion memory 12	ADC12MEM12		38h
	Conversion memory 11	ADC12MEM11		36h
	Conversion memory 10	ADC12MEM10		34h
	Conversion memory 9	ADC12MEM9		32h
	Conversion memory 8	ADC12MEM8		30h
	Conversion memory 7	ADC12MEM7		2Eh
	Conversion memory 6	ADC12MEM6		2Ch
	Conversion memory 5	ADC12MEM5		2Ah
	Conversion memory 4	ADC12MEM4		28h
	Conversion memory 3	ADC12MEM3		26h
	Conversion memory 2	ADC12MEM2		24h
	Conversion memory 1	ADC12MEM1		22h
	Conversion memory 0	ADC12MEM0		20h
	ADC memory-control register 15	ADC12MCTL15		1Fh
	ADC memory-control register 14	ADC12MCTL14		1Eh
	ADC memory-control register 13	ADC12MCTL13		1Dh
	ADC memory-control register 12	ADC12MCTL12		1Ch
	ADC memory-control register 11	ADC12MCTL11		1Bh
	ADC memory-control register 10	ADC12MCTL10		1Ah
	ADC memory-control register 9	ADC12MCTL9		19h
	ADC memory-control register 8	ADC12MCTL8		18h
	ADC memory-control register 7	ADC12MCTL7		17h
	ADC memory-control register 6	ADC12MCTL6		16h
	ADC memory-control register 5	ADC12MCTL5		15h
	ADC memory-control register 4	ADC12MCTL4		14h
	ADC memory-control register 3	ADC12MCTL3		13h
	ADC memory-control register 2	ADC12MCTL2		12h
	ADC memory-control register 1	ADC12MCTL1		11h
	ADC memory-control register 0	ADC12MCTL0		10h
	Interrupt-vector-word register	ADC12IV		0Eh
	Interrupt-enable register	ADC12IE		0Ch
	Interrupt-enable register	ADC12IFG		0Ah
	Control register 2	ADC12CTL2		04h
	Control register 1	ADC12CTL1		02h
	Control register 0	ADC12CTL0		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
USCI0	USCI interrupt vector word	UCB0IV	05C0h	3Eh
	USCI interrupt flags	UCB0IFG		3Dh
	USCI interrupt enable	UCB0IE		3Ch
	USCI I2C slave address	UCB0I2CSA		32h
	USCI I2C own address	UCB0I2COA		30h
	USCI synchronous transmit buffer	UCB0TXBUF		2Eh
	USCI synchronous receive buffer	UCB0RXBUF		2Ch
	USCI synchronous status	UCB0STAT		2Ah
	USCI I2C interrupt enable	UCB0I2CIE		28h
	USCI synchronous bit rate 1	UCB0BR1		27h
	USCI synchronous bit rate 0	UCB0BR0		26h
	USCI synchronous control 1	UCB0CTL1		21h
	USCI synchronous control 0	UCB0CTL0		20h
	USCI interrupt vector word	UCA0IV		1Eh
	USCI interrupt flags	UCA0IFG		1Dh
	USCI interrupt enable	UCA0IE		1Ch
	USCI IrDA receive control	UCA0IRRCTL		13h
	USCI IrDA transmit control	UCA0IRTCTL		12h
	USCI LIN control	UCA0ABCTL		10h
	USCI transmit buffer	UCA0TXBUF		0Eh
	USCI receive buffer	UCA0RXBUF		0Ch
	USCI status	UCA0STAT		0Ah
	USCI modulation control	UCA0MCTL		08h
	USCI baud rate 1	UCA0BR1		07h
	USCI baud rate 0	UCA0BR0		06h
	USCI control 1	UCA0CTL0		01h
	USCI control 0	UCA0CTL1		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
USCI1	USCI interrupt vector word	UCB1IV	0600h	3Eh
	USCI interrupt flags	UCB1IFG		3Dh
	USCI interrupt enable	UCB1IE		3Ch
	USCI I2C slave address	UCB1I2CSA		32h
	USCI I2C own address	UCB1I2COA		30h
	USCI synchronous transmit buffer	UCB1TXBUF		2Eh
	USCI synchronous receive buffer	UCB1RXBUF		2Ch
	USCI synchronous status	UCB1STAT		2Ah
	USCI I2C interrupt enable	UCB1I2CIE		28h
	USCI synchronous bit rate 1	UCB1BR1		27h
	USCI synchronous bit rate 0	UCB1BR0		26h
	USCI synchronous control 1	UCB1CTL1		21h
	USCI synchronous control 0	UCB1CTL0		20h
	USCI interrupt vector word	UCA1IV		1Eh
	USCI interrupt flags	UCA1IFG		1Dh
	USCI interrupt enable	UCA1IE		1Ch
	USCI IrDA receive control	UCA1IRRCTL		13h
	USCI IrDA transmit control	UCA1IRTCTL		12h
	USCI LIN control	UCA1ABCTL		10h
	USCI transmit buffer	UCA1TXBUF		0Eh
	USCI receive buffer	UCA1RXBUF		0Ch
	USCI status	UCA1STAT		0Ah
	USCI modulation control	UCA1MCTL		08h
	USCI baud rate 1	UCA1BR1		07h
	USCI baud rate 0	UCA1BR0		06h
	USCI control 1	UCA1CTL0		01h
	USCI control 0	UCA1CTL1		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
USCI2	USCI interrupt vector word	UCB2IV	0640h	3Eh
	USCI interrupt flags	UCB3IFG		3Dh
	USCI interrupt enable	UCB2IE		3Ch
	USCI I2C slave address	UCB2I2CSA		32h
	USCI I2C own address	UCB2I2COA		30h
	USCI synchronous transmit buffer	UCB2TXBUF		2Eh
	USCI synchronous receive buffer	UCB2RXBUF		2Ch
	USCI synchronous status	UCB2STAT		2Ah
	USCI I2C interrupt enable	UCB2I2CIE		28h
	USCI synchronous bit rate 1	UCB2BR1		27h
	USCI synchronous bit rate 0	UCB2BR0		26h
	USCI synchronous control 1	UCB2CTL1		21h
	USCI synchronous control 0	UCB2CTL0		20h
	USCI interrupt vector word	UCA2IV		1Eh
	USCI interrupt flags	UCA2IFG		1Dh
	USCI interrupt enable	UCA2IE		1Ch
	USCI IrDA receive control	UCA2IRRCTL		13h
	USCI IrDA transmit control	UCA2IRTCTL		12h
	USCI LIN control	UCA2ABCTL		10h
	USCI transmit buffer	UCA2TXBUF		0Eh
	USCI receive buffer	UCA2RXBUF		0Ch
	USCI status	UCA2STAT		0Ah
	USCI modulation control	UCA2MCTL		08h
	USCI baud rate 1	UCA2BR1		07h
	USCI baud rate 0	UCA2BR0		06h
	USCI control 1	UCA2CTL0		01h
	USCI control 0	UCA2CTL1		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
USCI3	USCI interrupt vector word	UCB3IV	0680h	3Eh
	USCI interrupt flags	UCB3IFG		3Dh
	USCI interrupt enable	UCB3IE		3Ch
	USCI I2C slave address	UCB3I2CSA		32h
	USCI I2C own address	UCB3I2COA		30h
	USCI synchronous transmit buffer	UCB3TXBUF		2Eh
	USCI synchronous receive buffer	UCB3RXBUF		2Ch
	USCI synchronous status	UCB3STAT		2Ah
	USCI I2C interrupt enable	UCB3I2CIE		28h
	USCI synchronous bit rate 1	UCB3BR1		27h
	USCI synchronous bit rate 0	UCB3BR0		26h
	USCI synchronous control 1	UCB3CTL1		21h
	USCI synchronous control 0	UCB3CTL0		20h
	USCI interrupt vector word	UCA3IV		1Eh
	USCI interrupt flags	UCA3IFG		1Dh
	USCI interrupt enable	UCA3IE		1Ch
	USCI IrDA receive control	UCA3IRRCTL		13h
	USCI IrDA transmit control	UCA3IRTCTL		12h
	USCI LIN control	UCA3ABCTL		10h
	USCI transmit buffer	UCA3TXBUF		0Eh
	USCI receive buffer	UCA3RXBUF		0Ch
	USCI status	UCA3STAT		0Ah
	USCI modulation control	UCA3MCTL		08h
	USCI baud rate 1	UCA3BR1		07h
	USCI baud rate 0	UCA3BR0		06h
	USCI control 1	UCA3CTL0		01h
	USCI control 0	UCA3CTL1		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
RTC_A	RTC alarm days	RTCADAY	04A0h	1Bh
	RTC alarm day of week	RTCADOW		1Ah
	RTC alarm hours	RTCAHOUR		19h
	RTC alarm minutes	RTCAMIN		18h
	RTC year high	RTCYEARH		17h
	RTC year low	RTCYEARL		16h
	RTC month	RTCMON		15h
	RTC days	RTCDAY		14h
	RTC day of week/counter register 4	RTCDOW/RTCNT4		13h
	RTC hours/counter register 3	RTCHOUR/RTCNT3		12h
	RTC minutes/counter register 2	RTCMIN/RTCNT2		11h
	RTC seconds/counter register 1	RTCSEC/RTCNT1		10h
	RTC interrupt vector word	RTCIV		0Eh
	RTC prescaler 1	RTCPS1		0Dh
	RTC prescaler 0	RTCPS0		0Ch
	RTC prescaler 1 control	RTCPS1CTL		0Ah
	RTC prescaler 0 control	RTCPS0CTL		08h
	RTC control 3	RTCCTL3		03h
	RTC control 2	RTCCTL2		02h
	RTC control 1	RTCCTL1		01h
	RTC control 0	RTCCTL0		00h
Port P11	Port P11 selection	P11SEL	02A0h	0Ah
	Port P11 drive strength	P11DS		08h
	Port P11 pullup/pulldown enable	P11REN		06h
	Port P11 direction	P11DIR		04h
	Port P11 output	P11OUT		02h
	Port P11 input	P11IN		00h
Port P10	Port P10 selection	P10SEL	0280h	0Bh
	Port P10 drive strength	P10DS		09h
	Port P10 pullup/pulldown enable	P10REN		07h
	Port P10 direction	P10DIR		05h
	Port P10 output	P10OUT		03h
	Port P10 input	P10IN		01h
Port P9	Port P9 selection	P9SEL	0280h	0Ah
	Port P9 drive strength	P9DS		08h
	Port P9 pullup/pulldown enable	P9REN		06h
	Port P9 direction	P9DIR		04h
	Port P9 output	P9OUT		02h
	Port P9 input	P9IN		00h
Port P8	Port P8 selection	P8SEL	0260h	0Bh
	Port P8 drive strength	P8DS		09h
	Port P8 pullup/pulldown enable	P8REN		07h
	Port P8 direction	P8DIR		05h
	Port P8 output	P8OUT		03h
	Port P8 input	P8IN		01h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Port P7	Port P7 selection	P7SEL	0260h	0Ah
	Port P7 drive strength	P7DS		08h
	Port P7 pullup/pulldown enable	P7REN		06h
	Port P7 direction	P7DIR		04h
	Port P7 output	P7OUT		02h
	Port P7 input	P7IN		00h
Port P6	Port P6 selection	P6SEL	0240h	0Bh
	Port P6 drive strength	P6DS		09h
	Port P6 pullup/pulldown enable	P6REN		07h
	Port P6 direction	P6DIR		05h
	Port P6 output	P6OUT		03h
	Port P6 input	P6IN		01h
Port P5	Port P5 selection	P5SEL	0240h	0Ah
	Port P5 drive strength	P5DS		08h
	Port P5 pullup/pulldown enable	P5REN		06h
	Port P5 direction	P5DIR		04h
	Port P5 output	P5OUT		02h
	Port P5 input	P5IN		00h
Port P4	Port P4 selection	P4SEL	0220h	0Bh
	Port P4 drive strength	P4DS		09h
	Port P4 pullup/pulldown enable	P4REN		07h
	Port P4 direction	P4DIR		05h
	Port P4 output	P4OUT		03h
	Port P4 input	P4IN		01h
Port P3	Port P3 selection	P3SEL	0220h	0Ah
	Port P3 drive strength	P3DS		08h
	Port P3 pullup/pulldown enable	P3REN		06h
	Port P3 direction	P3DIR		04h
	Port P3 output	P3OUT		02h
	Port P3 input	P3IN		00h
Port P2	Port P2 interrupt flag	P2IFG	0200h	1Dh
	Port P2 interrupt enable	P2IE		1Bh
	Port P2 interrupt edge select	P2IES		19h
	Port P2 interrupt vector word	P2IV		1Eh
	Port P2 selection	P2SEL		0Bh
	Port P2 drive strength	P2DS		09h
	Port P2 pullup/pulldown enable	P2REN		07h
	Port P2 direction	P2DIR		05h
	Port P2 output	P2OUT		03h
	Port P2 input	P2IN		01h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
Port P1	Port P1 interrupt flag	P1IFG	0200h	1Ch
	Port P1 interrupt enable	P1IE		1Ah
	Port P1 interrupt edge select	P1IES		18h
	Port P1 interrupt vector word	P1IV		0Eh
	Port P1 selection	P1SEL		0Ah
	Port P1 drive strength	P1DS		08h
	Port P1 pullup/pulldown enable	P1REN		06h
	Port P1 direction	P1DIR		04h
	Port P1 output	P1OUT		02h
	Port P1 input	P1IN		00h
Port PJ	Port PJ drive strength	PJDS	0320h	08h
	Port PJ pullup/pulldown enable	PJREN		06h
	Port PJ direction	PJDIR		04h
	Port PJ output	PJOUT		02h
	Port PJ input	PJIN		00h
SYS	Reset vector generator	SYSRSTIV	0180h	1Eh
	System NMI vector generator	SYSSNIV		1Ch
	User NMI vector generator	SYSUNIV		1Ah
	JTAG mailbox output 1	SYSJMBO1		0Eh
	JTAG mailbox output 0	SYSJMBO0		0Ch
	JTAG mailbox input 1	SYSJMBI1		0Ah
	JTAG mailbox input 0	SYSJMBI0		08h
	JTAG mailbox control	SYSJMBC		06h
	Bootstrap configuration area	SYSBSLC		02h
	System control	SYSCTL		00h
UCS	UCS control 8	UCSCTL8	0160h	10h
	UCS control 7	UCSCTL7		0Eh
	UCS control 6	UCSCTL6		0Ch
	UCS control 5	UCSCTL5		0Ah
	UCS control 4	UCSCTL4		08h
	UCS control 3	UCSCTL3		06h
	UCS control 2	UCSCTL2		04h
	UCS control 1	UCSCTL1		02h
	UCS control 0	UCSCTL0		00h
WDT_A	Watchdog timer control	WDTCTL	0150h	0Ch
RAM Control	RAM control 0	RCCTL0	0150h	08h
CRC16	CRC result	CRC16INIRES	0150h	04h
	CRC data input	CRC16DI		00h
Flash Control	Flash control 4	FCTL4	0140h	06h
	Flash control 3	FCTL3		04h
	Flash control 1	FCTL1		00h

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Table 8. Peripherals (continued)

MODULE NAME	REGISTER DESCRIPTION	REGISTER	BASE ADDRESS	OFFSET
PMM	PMM interrupt enable	PMMIE	0120h	0Eh
	PMM interrupt flags	PMMIFG		0Ch
	SVS low side control	SVSMLCTL		06h
	SVS high side control	SVSMHCTL		04h
	PMM control 1	PMMCTL1		02h
	PMM control 0	PMMCTL0		00h
Special Functions	SFR reset pin control	SFRRPCR	0100h	04h
	SFR interrupt flag	SFRIFG1		02h
	SFR interrupt enable	SFRIE1		00h

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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin (excluding V_{CORE})(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg}	Unprogrammed device(3)	–55°C to 150°C
	Programmed device(3)	–40°C to 105°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. V_{CORE} is for internal device usage only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming(AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC})(1)	'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)		1.8		3.6	V
		'F5438, 'F5436, 'F5419 'F5437, 'F5435, 'F5418		2.2		3.6	V
V_{SS}	Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS})				0		V
T_A	Operating free-air temperature	I version		–40		85	°C
CV_{CORE}	Capacitor at V_{CORE}				470		nF
CDV_{CC}/CV_{CORE}	Capacitor ratio of DV_{CC} to V_{CORE}			10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(2)(3) (see Figure 1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V	'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)	0		12.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)	0		16.0	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	'F5438, 'F5436, 'F5419 'F5437, 'F5435, 'F5418	0		18.0	
			'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)	0		25.0	

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(3) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.

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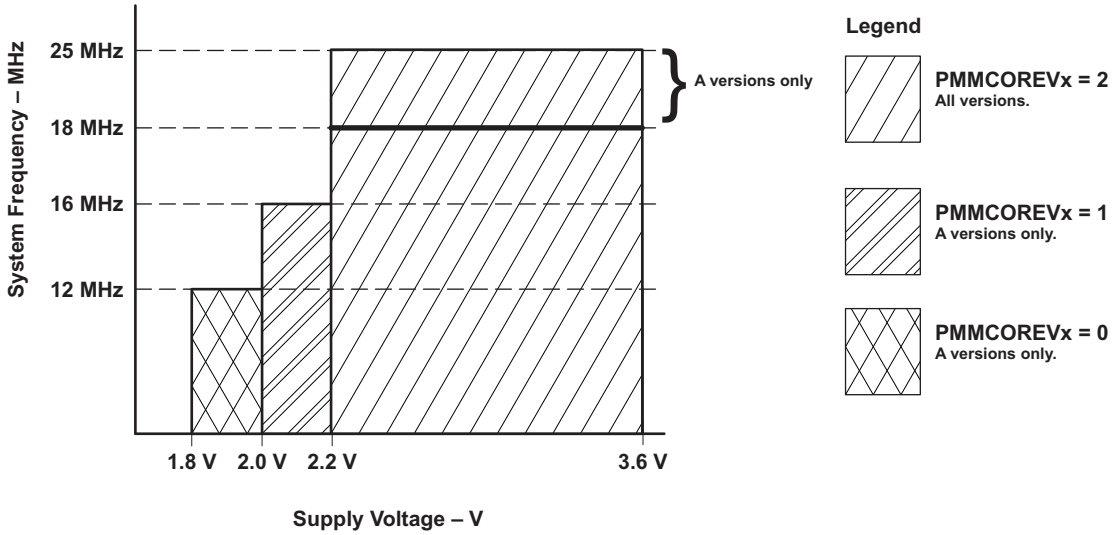

Figure 1. Frequency vs Supply Voltage

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Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)

PARAMETER	TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		0.22		mA
		PMMCOREVx = 1, V_{CC} = 3 V			0.25		
		PMMCOREVx = 2, V_{CC} = 3 V			0.28		
$I_{AM,\ 4MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 4$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		0.70		mA
		PMMCOREVx = 1, V_{CC} = 3 V			0.80		
		PMMCOREVx = 2, V_{CC} = 3 V			0.90		
$I_{AM,\ 8MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 8$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		1.32		mA
		PMMCOREVx = 1, V_{CC} = 3 V			1.55		
		PMMCOREVx = 2, V_{CC} = 3 V			1.75		
$I_{AM,\ 16MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 16$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 1, V_{CC} = 3 V	–40°C to 85°C		3.00		mA
		PMMCOREVx = 2, V_{CC} = 3 V			3.40		
$I_{AM,\ 18MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 18$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 1, V_{CC} = 3 V	–40°C to 85°C		3.40		mA
		PMMCOREVx = 2, V_{CC} = 3 V			3.85		
$I_{AM,\ 25MHz}$ A versions only	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 25$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in flash, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 2, V_{CC} = 3 V	–40°C to 85°C		5.65		mA
$I_{AM,\ 1MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in RAM, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		0.17		mA
		PMMCOREVx = 1, V_{CC} = 3 V			0.19		
		PMMCOREVx = 2, V_{CC} = 3 V			0.21		
$I_{AM,\ 4MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 4$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in RAM, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		0.49		mA
		PMMCOREVx = 1, V_{CC} = 3 V			0.56		
		PMMCOREVx = 2, V_{CC} = 3 V			0.63		
$I_{AM,\ 8MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK} = 8$ MHz, $f_{ACLK} = 32768$ Hz, Program executes in RAM, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 0, V_{CC} = 3 V	–40°C to 85°C		0.95		mA
		PMMCOREVx = 1, V_{CC} = 3 V			1.10		
		PMMCOREVx = 2, V_{CC} = 3 V			1.22		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Program executes typical data processing.

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Active Mode Supply Current Into V_{CC} Excluding External Current (continued)

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{AM,\ 16MHz}$	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 16 MHz, f_{ACLK} = 32768 Hz Program executes in RAM, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx = 1, V_{CC} = 3 V	–40°C to 85°C		2.10		mA
		PMMCOREVx = 2, V_{CC} = 3 V			2.40		
$I_{AM,\ 25MHz}$ A versions only	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 25 MHz, f_{ACLK} = 32768 Hz Program executes in RAM, XTS = 0, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0	PMMCOREVx =2, V_{CC} = 3 V	–40°C to 85°C		3.95		mA

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Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	V_{CC} = 2.2 V, PMMCOREVx = 0	–40°C to 85°C		75		µA
			V_{CC} = 3 V, PMMCOREVx = 2			78		
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0, XTS = 0	V_{CC} = 2.2 V, PMMCOREVx = 0	–40°C to 85°C		TBD		µA
			V_{CC} = 3 V, PMMCOREVx = 2			TBD		
$I_{LPM3,XT1LF}$	Low-power mode 3 (LPM3) current, XT1 LF mode(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, OSOCOFF = 0, CPUOFF = 1, SCG0 = 1, SCG1 = 1, XTS = 0, XT1DRIVEx = 0, SELAx = 0, SVM_H, SVS_H off, SVM_L, SVS_L off, RAM retention enabled	V_{CC} = 3 V, PMMCOREVx = 0	–40°C				µA
				25°C		2.6		
				60°C				
				85°C		7.1		
			V_{CC} = 3 V, PMMCOREVx = 1	–40°C				
				25°C		2.8		
				60°C				
				85°C		7.3		
			V_{CC} = 3 V, PMMCOREVx = 2	–40°C				
				25°C		2.9		
				60°C				
				85°C		7.6		
$I_{LPM3,VLO}$	Low-power mode 3 (LPM3) current, VLO mode(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = VLO, OSOCOFF = 0, CPUOFF = 1, SCG0 = 1, SCG1 = 1, SELAx = 1, SVM_H, SVS_H off, SVM_L, SVS_L off, RAM retention enabled	V_{CC} = 3 V, PMMCOREVx = 0	–40°C				µA
				25°C		1.7		
				60°C				
				85°C		6.2		
			V_{CC} = 3 V, PMMCOREVx = 1	–40°C				
				25°C		1.9		
				60°C				
				85°C		6.4		
			V_{CC} = 3 V, PMMCOREVx = 2	–40°C				
				25°C		2.0		
				60°C				
				85°C		6.7		

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(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout, WDT and RTC clocked by ACLK included.
(5) Current for brownout, WDT and RTC clocked by ACLK included.

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Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_{LPM4}	Low-power mode 4 (LPM4) current(6)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, OSOCOFF = 1, CPUOFF = 1, SCG0 = 1, SCG1 = 1, SVM_H, SVS_H off, SVM_L, SVS_L off, RAM retention enabled	V_{CC} = 3 V, PMMCOREVx = 0	–40°C				µA
				25°C		1.6		
				60°C				
				85°C		5.8		
			V_{CC} = 3 V, PMMCOREVx = 1	–40°C				
				25°C		1.65		
				60°C				
				85°C		6.1		
			V_{CC} = 3 V, PMMCOREVx = 2	–40°C				
				25°C		1.7		
				60°C				
				85°C		6.3		
I_{LPM5}	Low-power mode 5 (LPM5) current(7)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0 MHz, f_{ACLK} = 0 Hz, PMMREGOFF = 1	V_{CC} = 2.2 V	–40°C				µA
				25°C		0.1		
				60°C				
				85°C		0.5		
			V_{CC} = 3 V	–40°C				
				25°C		0.1		
				60°C				
				85°C		0.5		

(6) Current for brownout included. For this condition, the VLO must be selected as the source for ACLK, MCLK, and SMCLK otherwise additional current will be drawn due to the REFO oscillator.
(7) Internal regulator disabled. No data retention.

Schmitt-Trigger Inputs – Ports P1 to P11, PJ

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

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Inputs – Ports P1 and P2[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[2]	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag	2.2 V/3 V	20		ns

(1) Some devices may contain additional ports with interrupts. Please refer to the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – Ports P1 to P11, PJ

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1) (2)	1.8 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs – Ports P1 to P11, PJ (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA[1]	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA[2]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA[1]	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA[2]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA[1]	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA[2]		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA[1]	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA[2]		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – Ports P1 to P11, PJ (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA[2]	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA[3]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA[2]	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA[3]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA[2]	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA[3]		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA[2]	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA[3]		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

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Output Frequency – Ports P1 and P2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P1.6 C_L = 20 pF, R_L = 1 kΩ(1)(2)	V_{CC} = 1.8 V PMMCOREVx = 0	'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)		16	MHz
			V_{CC} = 3 V PMMCOREVx = 2	All versions		25	
f_{Port_CLK}	Clock output frequency	P1.0/TA0CLK/ACLK P1.6/SMCLK P2.0/TA1CLK/MCLK C_L = 20 pF(2)	V_{CC} = 1.8 V PMMCOREVx = 0	'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)		16	MHz
			V_{CC} = 3 V PMMCOREVx = 2	'F5438, 'F5436, 'F5419 'F5437, 'F5435, 'F5418		18	
				'F5438A, 'F5436A, 'F5419A 'F5437A, 'F5435A, 'F5418A (A versions only)		25	

(1) A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

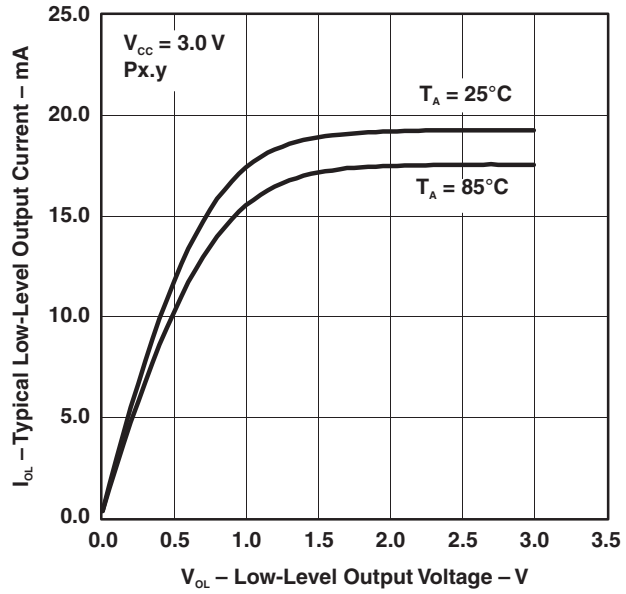

Figure 2.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

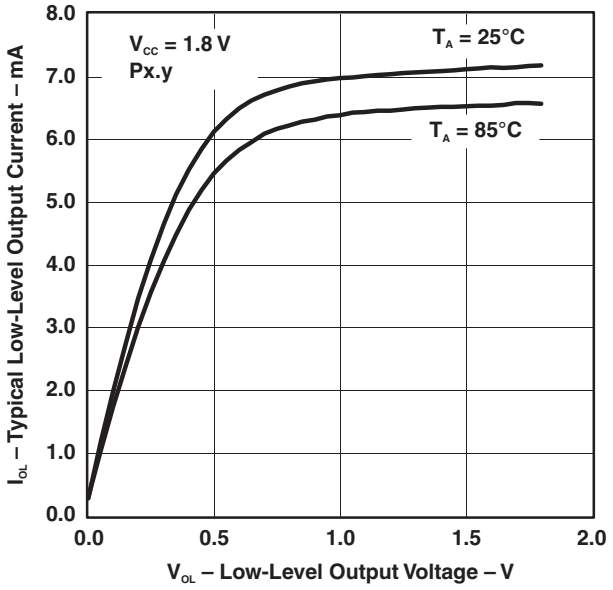

Figure 3.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

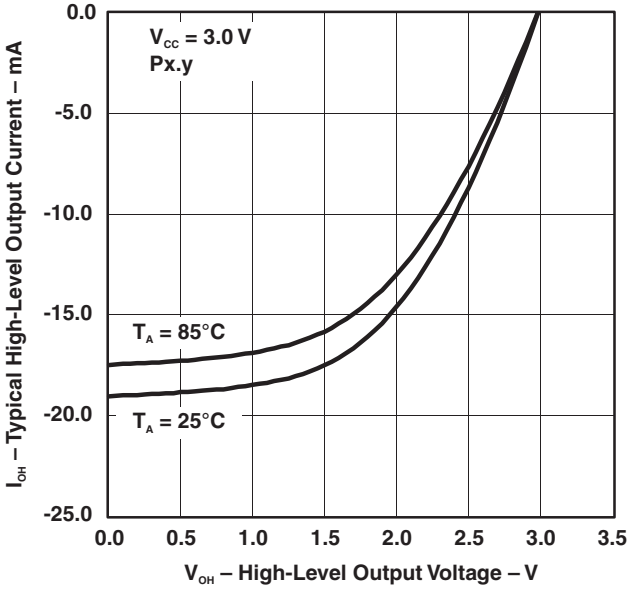

Figure 4.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

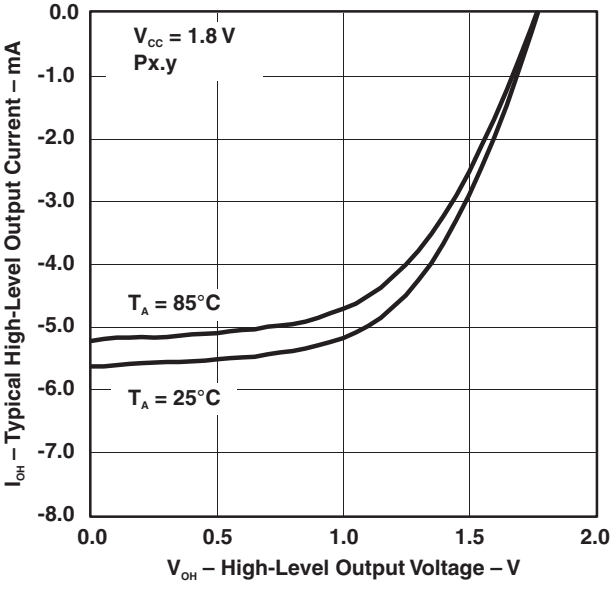

Figure 5.

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Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

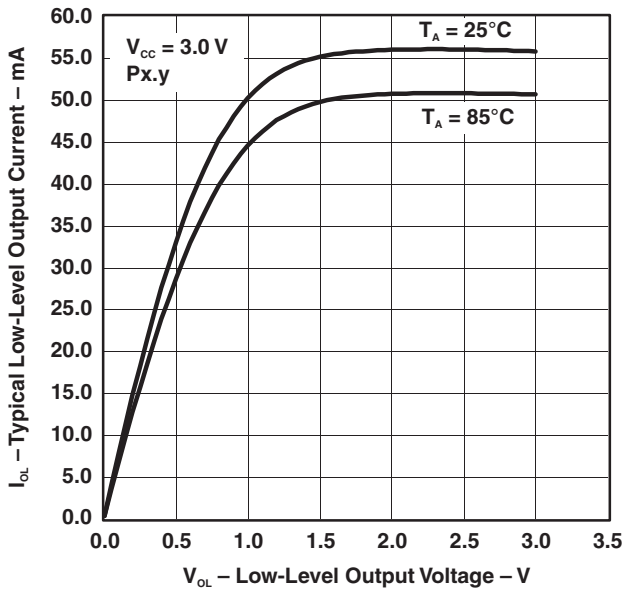

Figure 6.

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

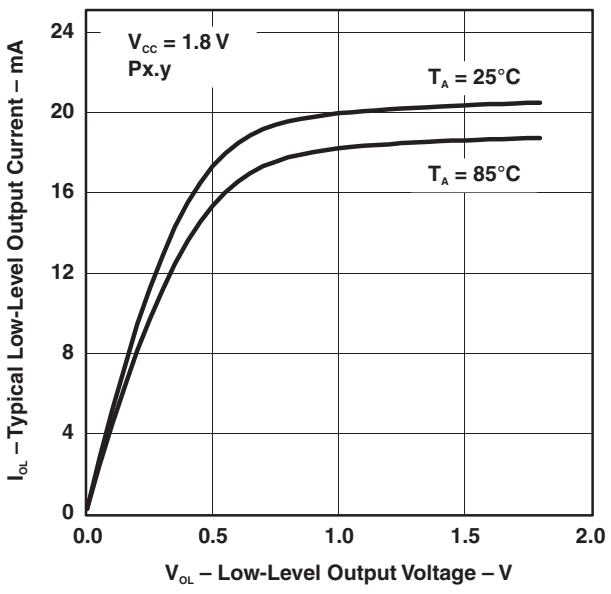

Figure 7.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

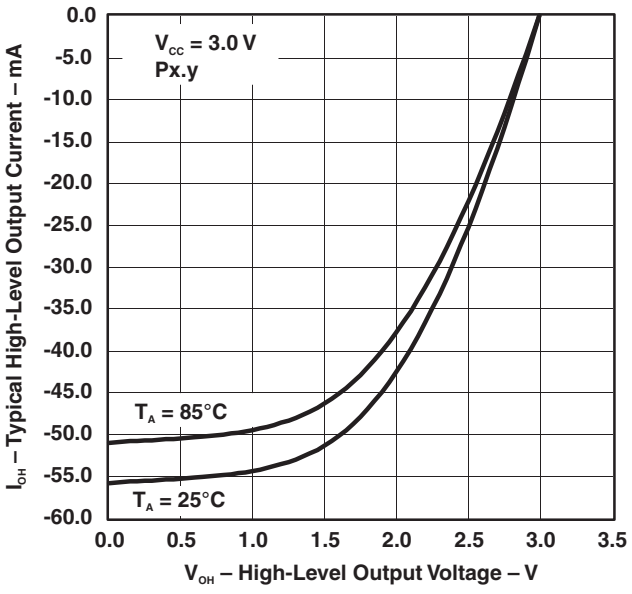

Figure 8.

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

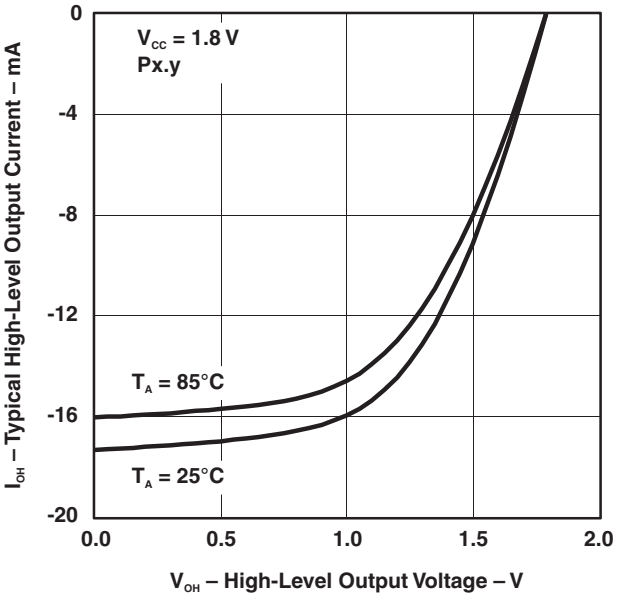

Figure 9.

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Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2)(3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
Duty cycle	LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0(8)		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 12 pF				1000	ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF				TBD	

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
a. Keep the trace between the device and the crystal as short as possible.
b. Design a good ground plane around the oscillator pins.
c. Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(2) When XT1BYPASS is set, the VLO, REFO, XT1 circuits are automatically powered down.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

PRODUCT PREVIEW

Crystal Oscillator, XT1, High-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.HF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, HF mode	f_{OSC} = 12 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C			60		µA
		f_{OSC} = 20 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			150		
		f_{OSC} = 32 MHz, XTS = 1, XOSCOFF = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			300		
$f_{XT1,HF0}$	XT1 oscillator crystal frequency, HF mode 0	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0[2]		4		8	MHz
$f_{XT1,HF1}$	XT1 oscillator crystal frequency, HF mode 1	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1[2]		8		16	MHz
$f_{XT1,HF2}$	XT1 oscillator crystal frequency, HF mode 2	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2[3]		16		24	MHz
$f_{XT1,HF3}$	XT1 oscillator crystal frequency, HF mode 3	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3[3]		24		32	MHz
$f_{XT1,HF,SW}$	XT1 oscillator logic-level square-wave input frequency, HF mode	XTS = 1, XT1BYPASS = 1[4][3]		4		32	MHz
OA_{HF}	Oscillation allowance for HF crystals[5]	XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,HF}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,HF}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 2, $f_{XT1,HF}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, $f_{XT1,HF}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time, HF mode	f_{OSC} = 6 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF				10	ms
		f_{OSC} = 20 MHz, XTS = 1, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 15 pF				TBD	
$C_{L,eff}$	Integrated effective load capacitance, HF mode[6][7]	XTS = 1			1		pF

(1) To improve EMI on the XT1 oscillator the following guidelines should be observed.
a. Keep the traces between the device and the crystal as short as possible.
b. Design a good ground plane around the oscillator pins.
c. Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
d. Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(2) Maximum frequency of operation of the entire device cannot be exceeded.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT1BYPASS is set, the VLO, REFO, XT1 circuits are automatically powered down.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

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Crystal Oscillator, XT1, High-Frequency Mode (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Duty cycle	HF mode	XTS = 1, Measured at ACLK, $f_{XT1,HF}$ = 32 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency, HF mode(8)	XTS = 1(9)		30		300	kHz

(8) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(9) Measured with logic-level input frequency but also applies to operation with crystals.

Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.XT2}$	Differential XT2 oscillator crystal current consumption from lowest drive setting	f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			60		µA
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			150		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			300		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency	XT2BYPASS = 1(4)(3)		4		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF				10	ms

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
a. Keep the traces between the device and the crystal as short as possible.
b. Design a good ground plane around the oscillator pins.
c. Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
d. Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
e. Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
f. If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

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Crystal Oscillator, XT2 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6)(1)				1		pF
Duty cycle		Measured at ACLK, $f_{XT2,HF3}$ = 32 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	4	12	20	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
Duty cycle		Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method: (MAX(-40...85°C) - MIN(-40...85°C))/MIN(85°C - (-40°C))
(2) Calculated using the box method: (MAX(1.8...3.6V) - MIN(1.8...3.6V))/MIN(1.8...3.6V)/(3.6V - 1.8V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated		1.8 V to 3.6 V			±3.5	%
		T_A = 25°C	3 V		±1.0		
Duty cycle		Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		0.4		ms

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)	DCORSELx = 0, DCOx = 0, MODx = 0	0.10		0.50	MHz
$f_{DCO(0,1)}$	DCO frequency (0, 1)	DCORSELx = 0, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(0,30)}$	DCO frequency (0, 30)	DCORSELx = 0, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(1,1)}$	DCO frequency (1, 1)	DCORSELx = 1, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(1,30)}$	DCO frequency (1, 30)	DCORSELx = 1, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(2,1)}$	DCO frequency (2, 1)	DCORSELx = 2, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(2,30)}$	DCO frequency (2, 30)	DCORSELx = 2, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(3,1)}$	DCO frequency (3, 1)	DCORSELx = 3, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(3,30)}$	DCO frequency (3, 30)	DCORSELx = 3, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(4,1)}$	DCO frequency (4, 1)	DCORSELx = 4, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(4,30)}$	DCO frequency (4, 30)	DCORSELx = 4, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(5,1)}$	DCO frequency (5, 1)	DCORSELx = 5, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(5,30)}$	DCO frequency (5, 30)	DCORSELx = 5, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(6,1)}$	DCO frequency (6, 1)	DCORSELx = 6, DCOx = 1, MODx = 0	TBD		TBD	MHz

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DCO Frequency (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(6,30)}$	DCO frequency (6, 30)	DCORSELx = 6, DCOx = 30, MODx = 0	TBD		TBD	MHz
$f_{DCO(7,1)}$	DCO frequency (7, 1)	DCORSELx = 7, DCOx = 1, MODx = 0	TBD		TBD	MHz
$f_{DCO(7,30)}$	DCO frequency (7, 30)	DCORSELx = 7, DCOx = 30, MODx = 0	32		95	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.5		2.1	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.04		1.10	ratio
Duty cycle		Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz, V_{CORE} = 1.2 V/2.0 V			±0.3	%/°C
df_{DCO}/dV_{CORE}	DCO frequency voltage drift	f_{DCO} = 1 MHz	0		TBD	%/V

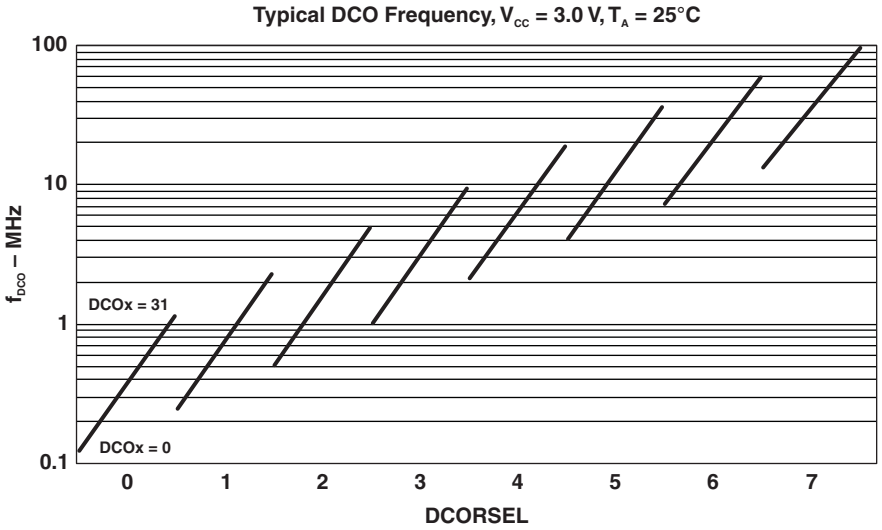

Figure 10. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}\_BOR\_IT-)$	BOR_H on voltage, DV_{CC} rising level	dDV_{CC}/d_t < 3 V/s			1.55	V
$V(DV_{CC}\_BOR\_IT+)$	BOR_H off voltage, DV_{CC} rising level	dDV_{CC}/d_t < 3 V/s	0.80	1.30	1.65	V
$V(DV_{CC}\_BOR\_hys)$	BOR_H hysteresis		100		250	mV
$V(V_{CORE}\_BOR\_IT-)$	BOR_L on voltage, V_{CORE} rising level		0.70		0.85	V
$V(V_{CORE}\_BOR\_IT+)$	BOR_L off voltage, V_{CORE} rising level		0.85		1.05	V
$V(V_{CORE}\_BOR\_hys)$	BOR_L hysteresis		70		200	mV
$V(DV_{CC}\_OK)$	DV_{CC} on/off voltage level		0.80		1.40	V
td_{BOR}	BOR_L reset release time				2000	µs
t_{RESET}	Pulse length required at $\overline{RST}$/NMI pin to accept a reset		2			µs

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PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		75		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		15		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level	SVSHE = 1, SVSHRVL = 0		1.64		V
		SVSHE = 1, SVSHRVL = 1		1.84		
		SVSHE = 1, SVSHRVL = 2		2.04		
		SVSHE = 1, SVSHRVL = 3		2.16		
$V_{(SVSH\_IT+)}$	SVS_H off voltage level	SVSHE = 1, SVSMHRRL = 0		1.74		V
		SVSHE = 1, SVSMHRRL = 1		1.94		
		SVSHE = 1, SVSMHRRL = 2		2.14		
		SVSHE = 1, SVSMHRRL = 3		2.26		
		SVSHE = 1, SVSMHRRL = 4		2.40		
		SVSHE = 1, SVSMHRRL = 5		2.70		
		SVSHE = 1, SVSMHRRL = 6		3.00		
		SVSHE = 1, SVSMHRRL = 7		3.00		
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, DV_{CC} = $V_{(SVMH\_IT+)}$ + 10 mV, SVSHFP = 0		1		µs
		SVSHE = 1, DV_{CC} = $V_{(SVMH\_IT-)}$ – 10 mV, SVSHFP = 0		1		
		SVSHE = 1, DV_{CC} = $V_{(SVMH\_IT+)}$ + 10 mV, SVSHFP = 1		150		
		SVSHE = 1, DV_{CC} = $V_{(SVMH\_IT-)}$ – 10 mV, SVSHFP = 1		150		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

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PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		75		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		15		µA
$V_{(SVMH)}$	SVM_H on/off voltage level	SVMHE = 1, SVSMHRRL = 0		1.74		V
		SVMHE = 1, SVSMHRRL = 1		1.94		
		SVMHE = 1, SVSMHRRL = 2		2.14		
		SVMHE = 1, SVSMHRRL = 3		2.26		
		SVMHE = 1, SVSMHRRL = 4		2.40		
		SVMHE = 1, SVSMHRRL = 5		2.70		
		SVMHE = 1, SVSMHRRL = 6		3.00		
		SVMHE = 1, SVSMHRRL = 7		3.00		
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, DV_{CC} = $V_{(SVMH\_IT)}$ ± 10 mV, SVMHFP = 0		1		µs
		SVMHE = 1, DV_{CC} = $V_{(SVMH\_IT)}$ ± 10 mV, SVMHFP = 1		150		µs

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, V_{CORE} = 1.8 V		0		nA
		SVSLE = 1, V_{CORE} = 1.8 V, SVSLFP = 0		75		nA
		SVSLE = 1, V_{CORE} = 1.8 V, SVSLFP = 1		15		µA
$V_{(SVSL\_IT-)}$	SVS_L on voltage level	SVSLE = 1, SVSLRVL = 0		1.27		V
		SVSLE = 1, SVSLRVL = 1		1.47		
		SVSLE = 1, SVSLRVL = 2		1.67		
		SVSLE = 1, SVSLRVL = 3		1.77		
$V_{(SVSL\_IT+)}$	SVS_L off voltage level	SVSLE = 1, SVSMLRRL = 0		1.34		V
		SVSLE = 1, SVSMLRRL = 1		1.54		
		SVSLE = 1, SVSMLRRL = 2		1.74		
		SVSLE = 1, SVSMLRRL = 3, 4, 5, 6, 7		1.84		
$V_{(SVSL\_HYS)}$	SVS_L hystersis	SVSLE = 1, SVSMLRRL = 0		70		mV
		SVSLE = 1, SVSMLRRL = 1		70		
		SVSLE = 1, SVSMLRRL = 2		70		
		SVSLE = 1, SVSMLRRL = 3		70		
$t_{(SVSL)}$	SVS_L on/off delay time	SVSLE = 1, DV_{CC} = $V_{(SVML\_IT+)}$ ± 10 mV, SVSLFP = 0		1		µs
		SVSLE = 1, DV_{CC} = $V_{(SVML\_IT+)}$ ± 10 mV, SVSLFP = 1		200		
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, DV_{CC} = $V_{(SVML\_IT+)}$ + 10 mV, SVSLFP = 0		1		µs
		SVSLE = 1, DV_{CC} = $V_{(SVML\_IT-)}$ – 10mV, SVSLFP = 0		1		
		SVSLE = 1, DV_{CC} = $V_{(SVML\_IT+)}$ + 10 mV, SVSLFP = 1		150		
		SVSLE = 1, DV_{CC} = $V_{(SVML\_IT-)}$ – 10 mV, SVSLFP = 1		150		

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PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, V_{CORE} = 1.8 V		0		nA
		SVMLE= 1, V_{CORE} = 1.8 V, SVMLFP = 0		75		nA
		SVMLE= 1, V_{CORE} = 1.8 V, SVMLFP = 1		15		µA
$V_{(SVML)}$	SVM_L on/off voltage level	SVMLE = 1, SVSMLRRL = 0		1.34		V
		SVMLE = 1, SVSMLRRL = 1		1.54		
		SVMLE = 1, SVSMLRRL = 2		1.74		
		SVMLE = 1, SVSMLRRL = 3, 4, 5, 6, 7		1.84		
		SVMLE = 1, SVSMLOVPL = 1		2.02		
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, DV_{CC} = $V_{(SVML\_IT)}$ 10 mV, SVMLFP = 0		1		µs
		SVMLE = 1, DV_{CC} = $V_{(SVML\_IT)}$ 10 mV, SVMLFP = 1		200		

PMM, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{FAST-WAKE-UP}$	PMM wake-up time from LPM2, LPM3, or LPM4 to active mode	DV_{CC} = 1.80 V, PMMCOREV = 0, SVSMLRRL = 0, SVSLFP = 0, I_{LOAD}(LPMx) = 30 µA, I_{LOAD}(AM) = 13 mA, V_{CORE} = $V_{(SVSL\_IT+, typ)}$			5	µs
		DV_{CC} = 2.00 V, PMMCOREV = 1, SVSMLRRL = 1, SVSLFP = 0, I_{LOAD}(LPMx) = 30 µA, I_{LOAD}(AM) = 17 mA, V_{CORE} = $V_{(SVSL\_IT+, typ)}$			5	
		DV_{CC} = 2.20 V, PMMCOREV = 2, SVSMLRRL = 2, SVSLFP = 0, I_{LOAD}(LPMx) = 30 µA, I_{LOAD}(AM) = 21 mA, V_{CORE} = $V_{(SVSL\_IT+, typ)}$			5	
		DV_{CC} = 2.40 V, PMMCOREV = 3, SVSMLRRL = 3, SVSLFP = 0, I_{LOAD}(LPMx) = 30 µA, I_{LOAD}(AM) = 25 mA, V_{CORE} = $V_{(SVSL\_IT+, typ)}$			5	
$t_{WAKE-UP\ LPM5}$	PMM wake-up time from LPM5 to active mode			2	3	ms

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USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz
t_{τ}	UART receive deglitch time(1)		2.2 V	50		600	ns
			3 V	50		600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 11 and Figure 12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		2.2 V	65			ns
			3 V	50			
$t_{HD,MI}$	SOMI input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	2.2 V			25	ns
			3 V			20	

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USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 13 and Figure 14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		2.2 V/3 V		40		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		2.2 V/3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		2.2 V/3 V		40		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		2.2 V/3 V		40		ns
$t_{SU,SI}$	SIMO input data setup time		2.2 V	20			ns
			3 V	15			
$t_{HD,SI}$	SIMO input data hold time		2.2 V	0			ns
			3 V	0			
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	2.2 V			62	ns
			3 V			50	

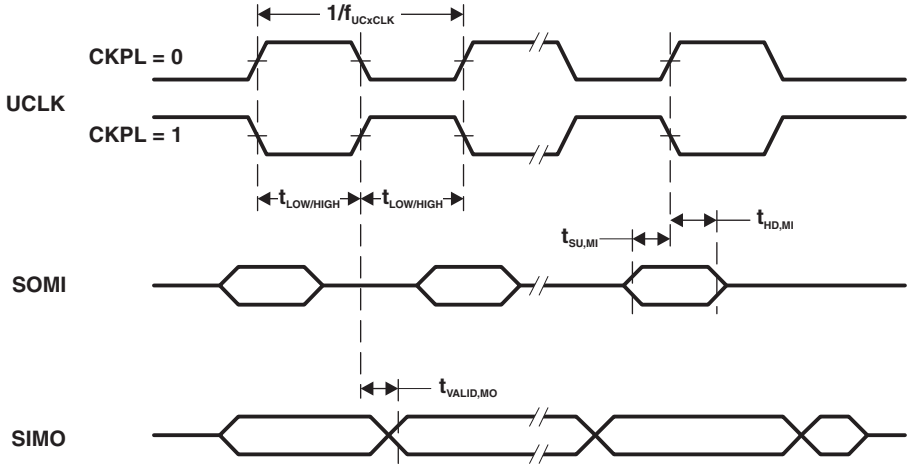

Figure 11. SPI Master Mode, CKPH = 0

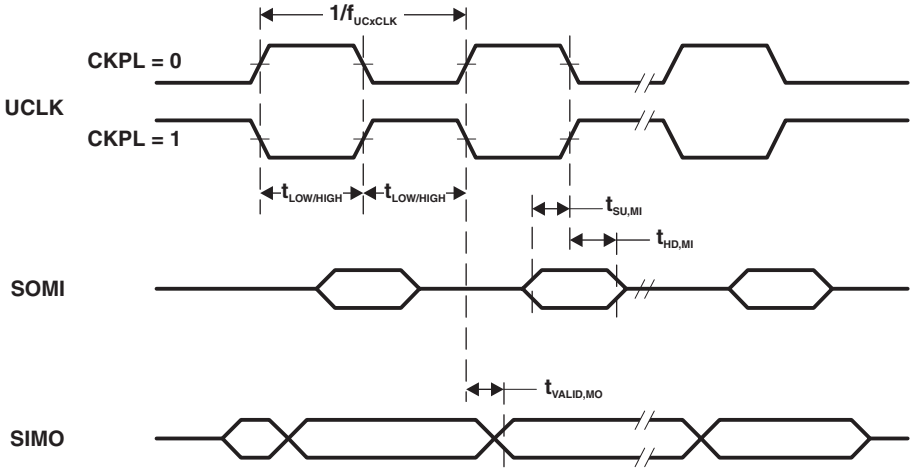

Figure 12. SPI Master Mode, CKPH = 1

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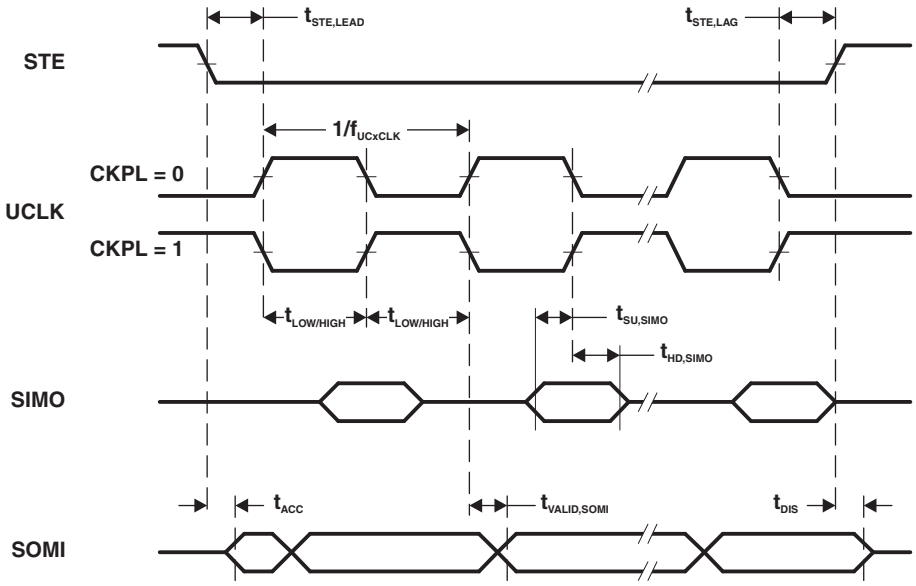

Figure 13. SPI Slave Mode, CKPH = 0

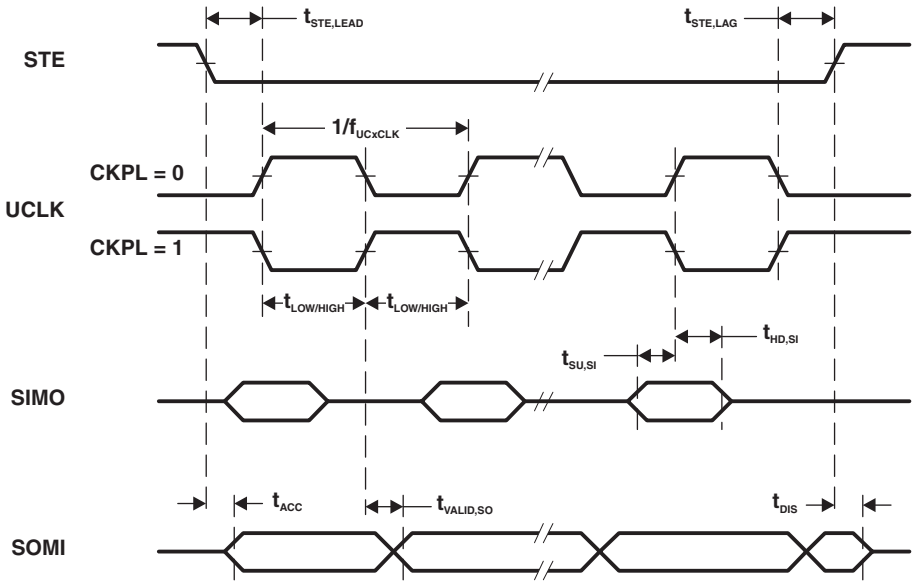

Figure 14. SPI Slave Mode, CKPH = 1

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USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V/3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V/3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V/3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		2.2 V/3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50		600	ns
			3 V	50		600	

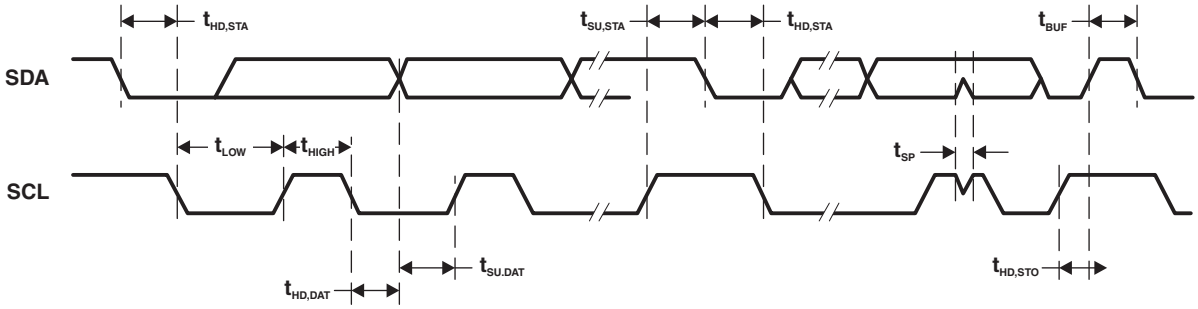

Figure 15. I2C Mode Timing

12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 pins: P6.0 to P6.7, P7.4 to P7.7, P5.0, and P5.1 terminals		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		125	155	µA
			3 V		150	220	
I_{REF+}	Operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		150	190	µA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V/3 V		150	180	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON resistance	$0 V \le V_{Ax} \le AV_{CC}$		10		2000	Ω

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion. No external load.

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12-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4		AV_{CC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0		1.2	V
($V_{eREF+} - V_{REF-}/V_{eREF-}$)	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4		AV_{CC}	V
I_{VeREF+}	Static input current	$0 V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0 V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

12-Bit ADC, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+}(max) \le I_{VREF+} \le I_{VREF+}(min)$	3 V	2.35	2.45	2.53	V
		REF2_5V = 0 for 1.5 V, $I_{VREF+}(max) \le I_{VREF+} \le I_{VREF+}(min)$	2.2 V/3 V	1.41	1.47	1.53	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0		2.2			V
		REF2_5V = 1		2.8			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V			–1	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal	I_{VREF+} = +10 µA/–1000 µA, Analog input voltage ~0.75 V, REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = +10 µA/–1000 µA, Analog input voltage ~1.25 V, REF2_5V = 1	3 V			±2	
C_{VREF+}	Capacitance at V_{REF+} terminal	REFON = REFOUT = 1, $0 mA \le I_{VREF+} \le I_{VREF+}(max)$	2.2 V/3 V	20		100	pF
T_{REF+}	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of $0 mA \le I_{VREF+} \le –1 mA$	2.2 V/3 V		±30		ppm/°C
t_{SETTLE}	Settling time of reference voltage(2)	V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V, REFOUT = 0, REFON = 0 → 1			20		µs
		V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V $C_{VREF} = C_{VREF}(max)$ REFOUT = 1, REFON = 0 → 1			35		
		V_{REF+} = 2.5 V, V_{AVCC} = 2.8 V $C_{VREF} = C_{VREF}(max)$ REFOUT = 1, REFON = 0 → 1			35		

(1) The leakage current is defined in the leakage current table with P6.x/Ax parameter.
(2) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

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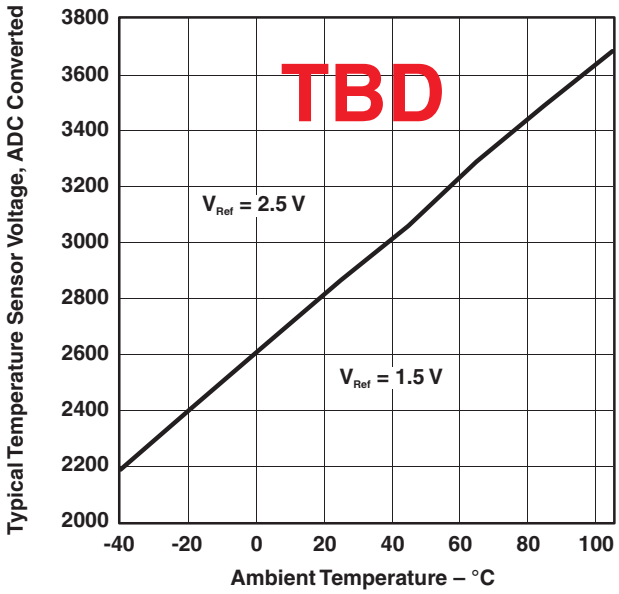

Figure 16. Typical Temperature Sensor Voltage

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12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2 V/3 V	0.45	5	5.5	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator (1)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V/3 V	4.5	5	5.5	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, $f_{ADC12OSC}$ = 4.5 MHz to 5.5 MHz	2.2 V/3 V	2.4		2.9	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			(2)		
$t_{ADC12ON}$	Turn on settling time of the ADC	See (3)				100	ns
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (4)	2.2 V/3 V	1000			ns

(1) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(2) $13 \times ADC12DIV \times 1/f_{ADC12CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

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12-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < (V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ V_{AVCC}				±1.7	
E_D	Differential linearity error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 20 pF	2.2 V/3 V			±1	LSB
E_O	Offset error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 20 pF	2.2 V/3 V		±1	±1.5	LSB
E_G	Gain error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 20 pF	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	(V_{eREF+} – V_{REF-}/V_{eREF-})min ≤ (V_{eREF+} – V_{REF-}/V_{eREF-}), C_{VREF+} = 20 pF	2.2 V/3 V		±2	±5	LSB

12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (1)	REFON = 0, INCH = 0Ah, ADC12ON = N A, T_A = 25°C	2.2 V		150		µA
			3 V		150		
V_{SENSOR}	See (2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		TBD		mV
			3 V		TBD		
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		TBD	±3%	mV/°C
			3 V		TBD	±3%	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (4)	ADC12ON = 1, INCH = 0Bh	2.2 V			TBD	µA
			3 V			TBD	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2.2 V		1.1		V
			3 V		1.5		
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V/3 V	1000			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1) or (ADC12ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
(2) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

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Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage	A versions only		1.8		3.6	V
		Non-A versions		2.2		3.6	
$t_{READMARGIN}$	Read access time during margin mode					200	ns
I_{PGM}	Supply current from DV_{CC} during program				3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase					2	mA
I_{MERASE}, I_{BANK}	Supply current from DV_{CC} during mass erase or bank erase					2	mA
t_{CPT}	Cumulative program time		See (1)			16	ms
$t_{CMErase}$	Cumulative mass erase time			10			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration		T_J = 25°C	100			years
t_{Word}	Word or byte program time		See (2)	64		85	µs
$t_{Block, 0}$	Block program time for first byte or word		See (2)	49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word		See (2)	37		49	µs
$t_{Block, N}$	Block program time for last byte or word		See (2)	55		73	µs
$t_{Mass\ Erase}$	Mass erase time		See (2)	23		32	ms
$t_{Seg\ Erase}$	Segment erase time		See (2)	23		32	ms

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V/3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length	2.2 V/3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V/3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency - 4-wire JTAG (2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pull-down resistance on TEST	2.2 V/3 V	20	35	50	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

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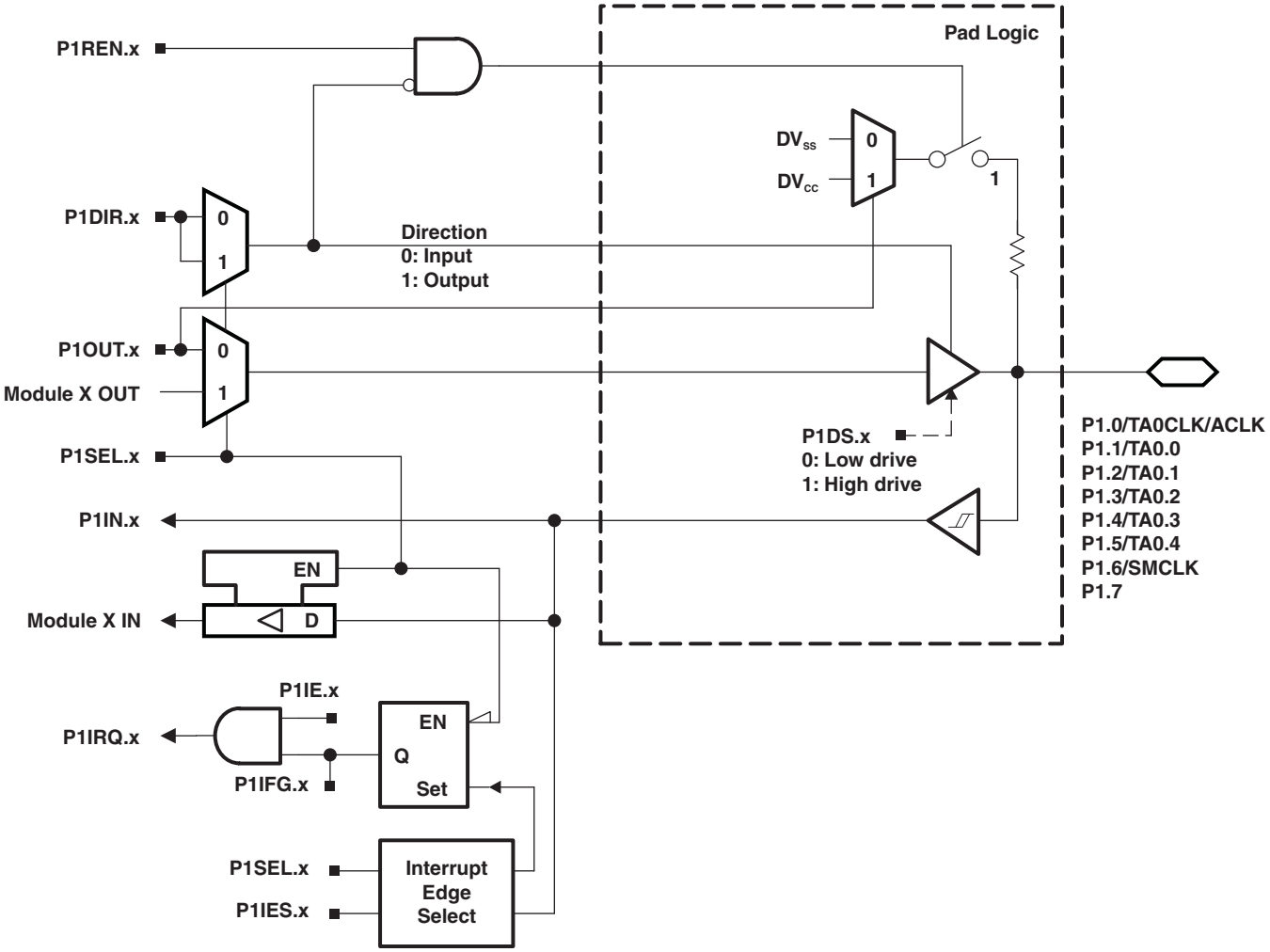
INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger



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Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer0_A5.TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI0A	0	1
		Timer0_A5.TA0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI1A	0	1
		Timer0_A5.TA1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI2A	0	1
		Timer0_A5.TA2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI3A	0	1
		Timer0_A5.TA3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI4A	0	1
		Timer0_A5.TA4	1	1
P1.6/SMCLK	6	P1.6 (I/O)	I: 0; O: 1	0
		SMCLK	1	1
P1.7	7	P1.7 (I/O)	I: 0; O: 1	0

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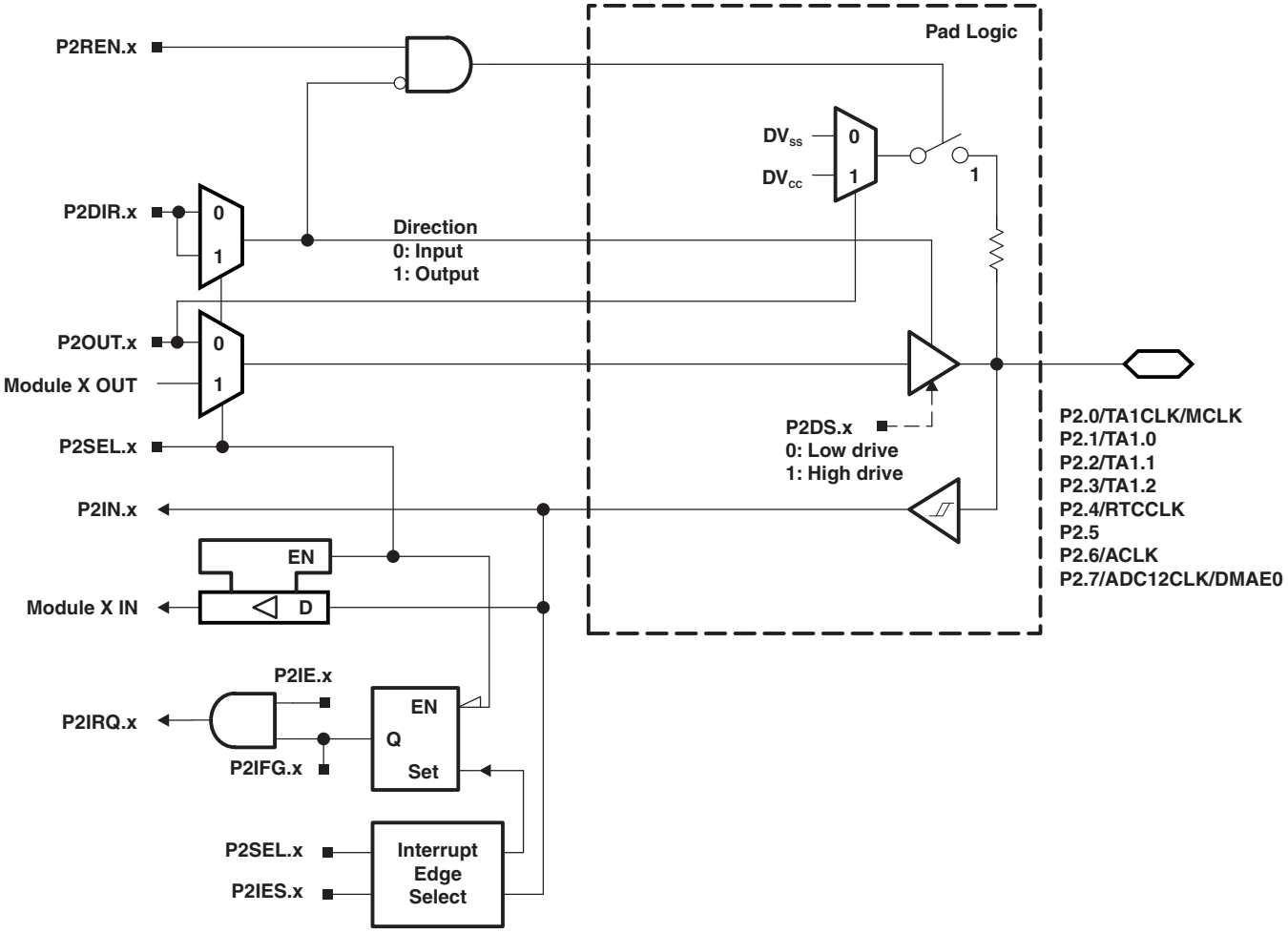
Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger



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Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P2DIR.x	P2SEL.x
P2.0/TA1CLK/MCLK	0	P2.0 (I/O)	I: 0; O: 1	0
		Timer1_A3.TA1CLK	0	1
		MCLK	1	1
P2.1/TA1.0	1	P2.1 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI0A	0	1
		Timer1_A3.TA0	1	1
P2.2/TA1.1	2	P2.2 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI1A	0	1
		Timer1_A3.TA1	1	1
P2.3/TA1.2	3	P2.3 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI2A	0	1
		Timer1_A3.TA2	1	1
P2.4/RTCCLK	4	P2.4 (I/O)	I: 0; O: 1	0
		RTCCLK	1	1
P2.5	5	P2.5 (I/O	I: 0; O: 1	0
P2.6/ACLK	6	P2.6 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P2.7/ADC12CLK/DMAE0	7	P2.7 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		ADC12CLK	1	1

(1) X = Don't care

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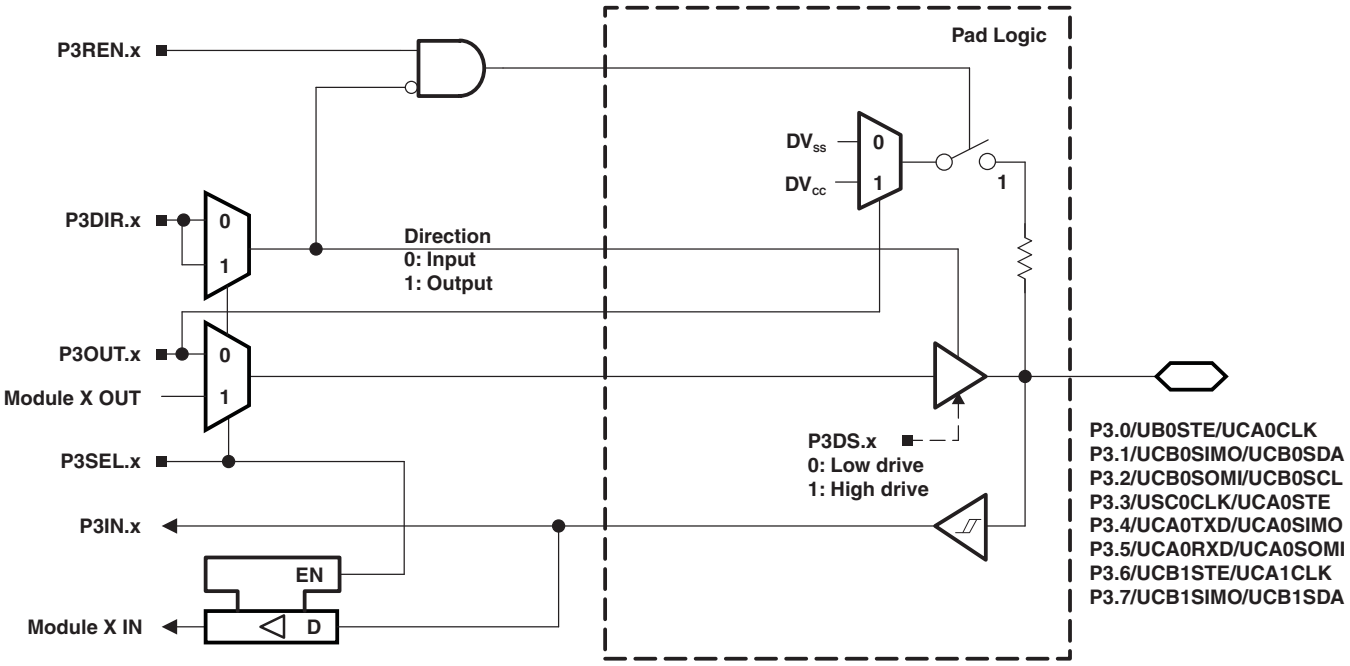
Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger



Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/UCA0CLK	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK[2][3]	X	1
P3.1/UCB0SIMO/UCB0SDA	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA[2][4]	X	1
P3.2/UCB0SOMI/UCB0SCL	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL[2][4]	X	1
P3.3/UCB0CLK/UCA0STE	3	P3.3 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE[2]	X	1
P3.4/UCA0TXD/UCA0SIMO	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO[2]	X	1
P3.5/UCA0RXD/UCA0SOMI	5	P3.5 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI[2]	X	1
P3.6/UCB1STE/UCA1CLK	6	P3.6 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK[2][5]	X	1
P3.7/UCB1SIMO/UCB1SDA	7	P3.7 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA[2][4]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI A0/B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) UCA1CLK function takes precedence over UCB1STE function. If the pin is required as UCA1CLK input or output, USCI A1/B1 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

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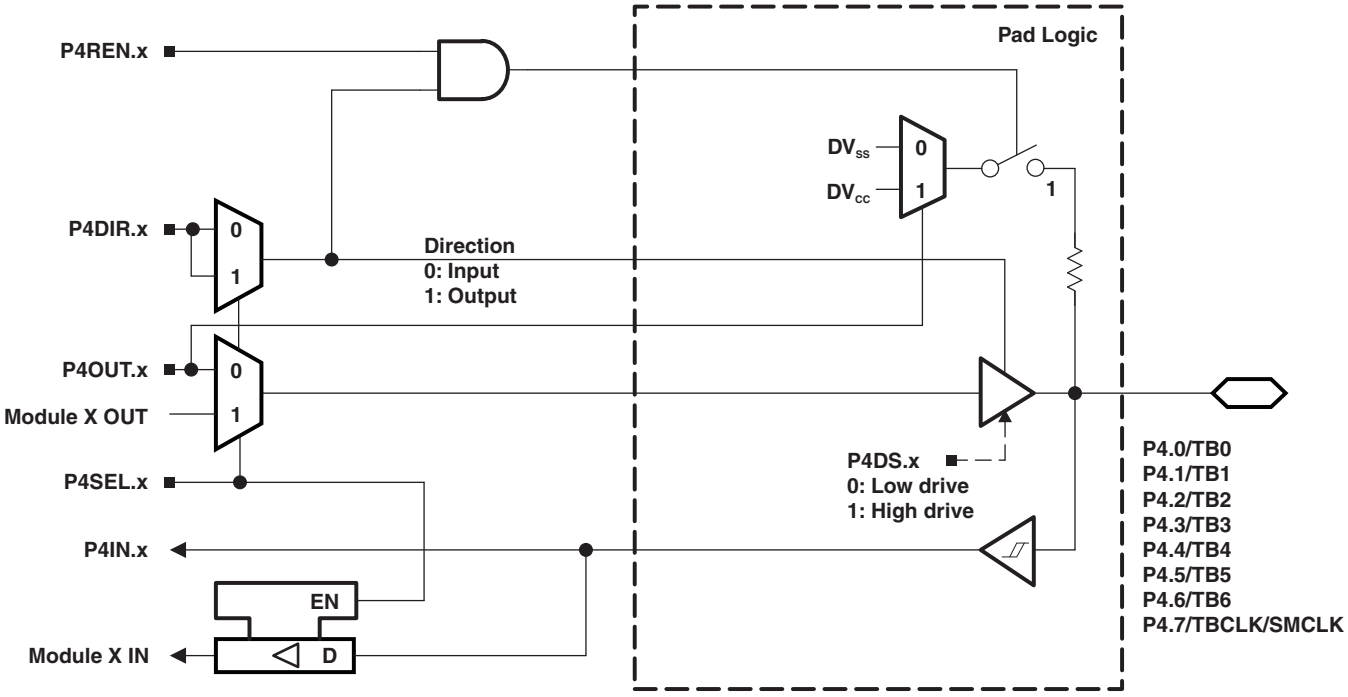
Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger



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Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0	0	4.0 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI0A and Timer_B7.CCI0B	0	1
		Timer_B7.TB0(1)	1	1
P4.1/TB1	1	4.1 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI1A and Timer_B7.CCI1B	0	1
		Timer_B7.TB1(1)	1	1
P4.2/TB2	2	4.2 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI2A and Timer_B7.CCI2B	0	1
		Timer_B7.TB2(1)	1	1
P4.3/TB3	3	4.3 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI3A and Timer_B7.CCI3B	0	1
		Timer_B7.TB3(1)	1	1
P4.4/TB4	4	4.4 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI4A and Timer_B7.CCI4B	0	1
		Timer_B7.TB4(1)	1	1
P4.5/TB5	5	4.5 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI5A and Timer_B7.CCI5B	0	1
		Timer_B7.TB5(1)	1	1
P4.6/TB6	6	4.6 (I/O)	I: 0; O: 1	0
		Timer_B7.CCI6A and Timer_B7.CCI6B	0	1
		Timer_B7.TB6(1)	1	1
P4.7/TBCLK/SMCLK	7	4.7 (I/O)	I: 0; O: 1	0
		Timer_B7.TBCLK	0	1
		SMCLK	1	1

(1) Setting TBOUTH causes all Timer_B configured outputs to be set to high impedance.

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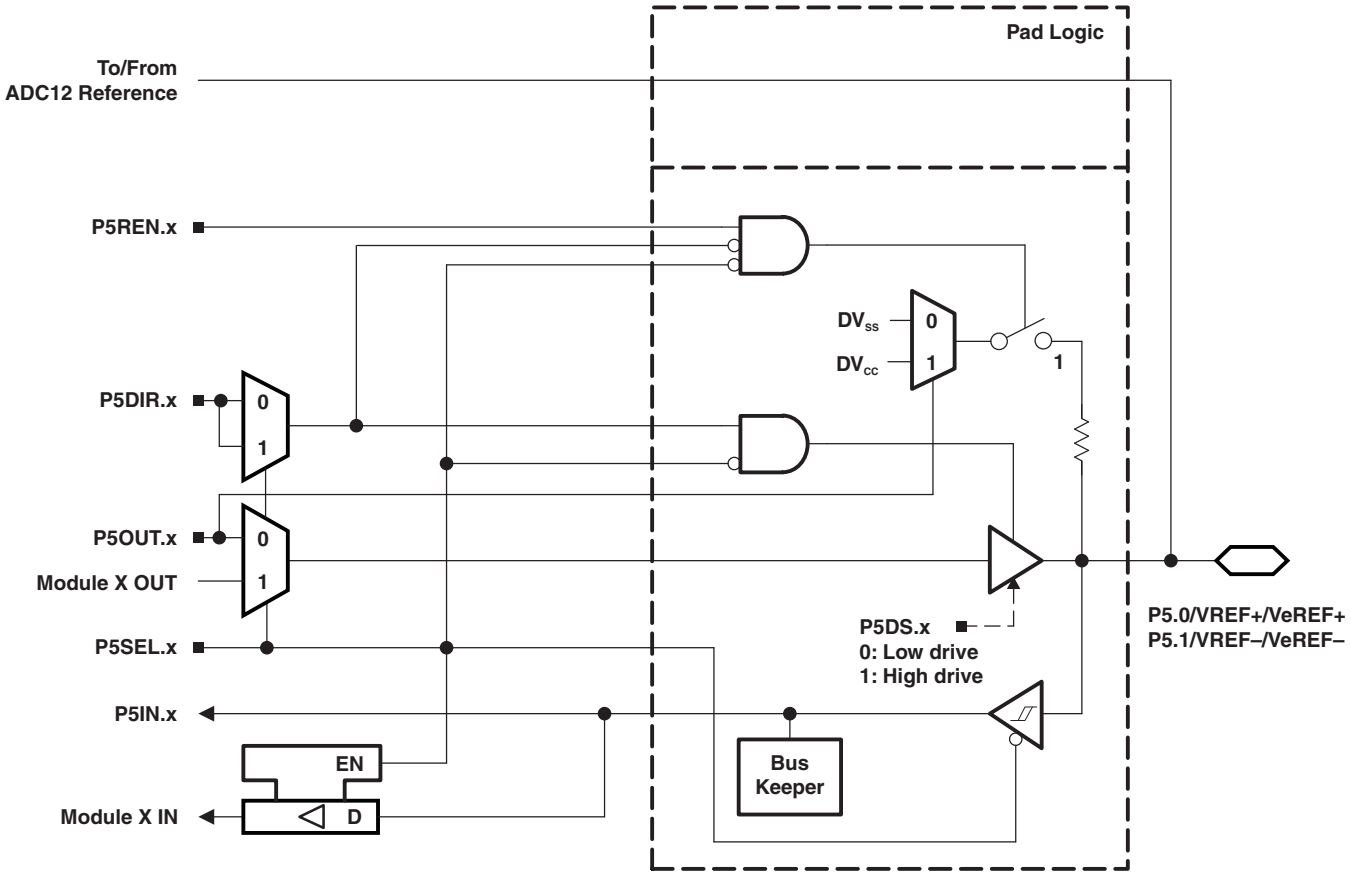
Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger



Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/VREF+/VeREF+	0	P5.0 (I/O) (2)	I: 0; O: 1	0	X
		VeREF+ (3)	X	1	0
		VREF+ (4)	X	1	1
P5.1/VREF–/VeREF–	1	P5.1 (I/O) (2)	I: 0; O: 1	0	X
		VeREF– (5)	X	1	0
		VREF– (6)	X	1	1

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A.
(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin.
(5) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A.
(6) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF– reference is available at the pin.

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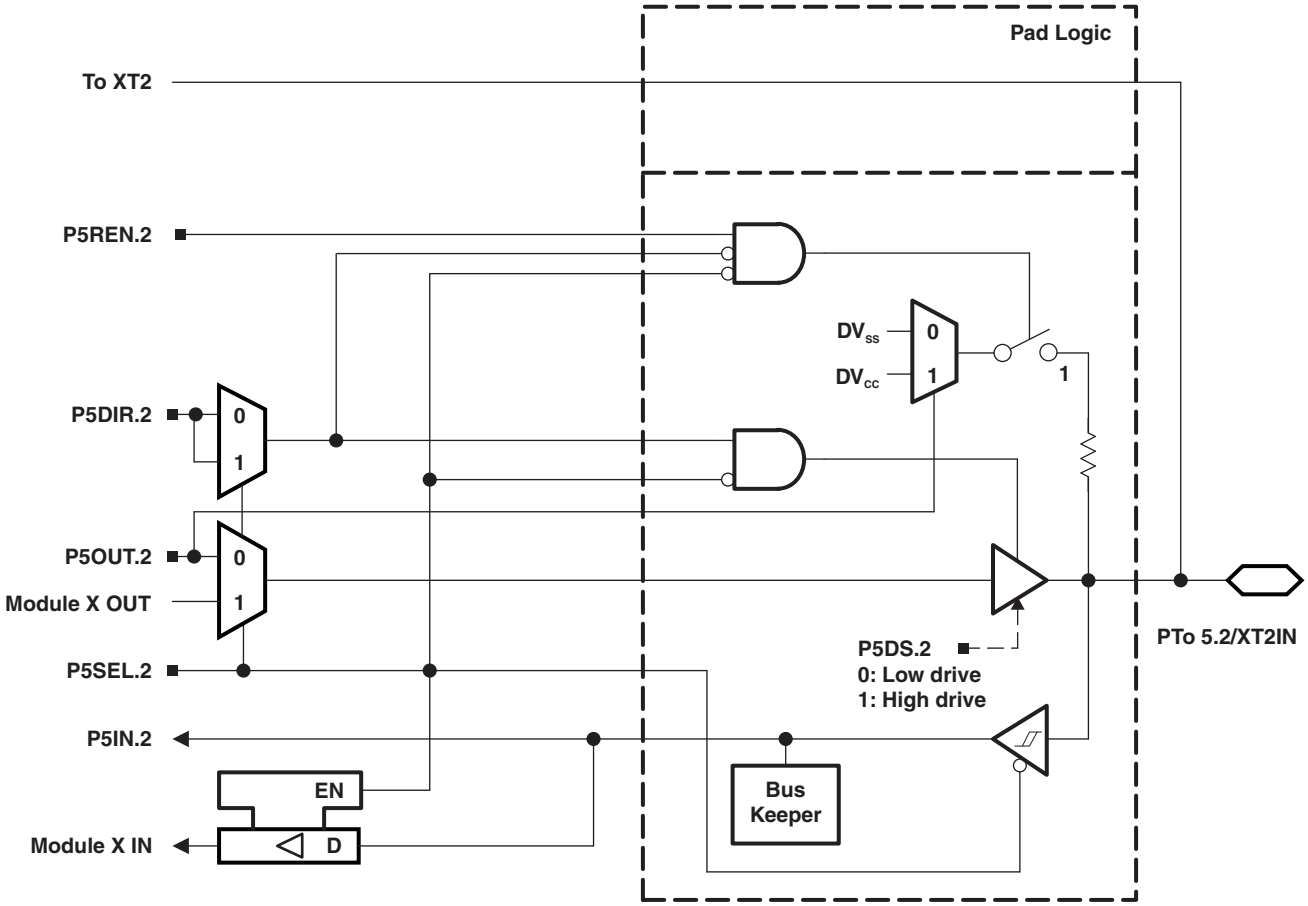
Port P5, P5.2, Input/Output With Schmitt Trigger



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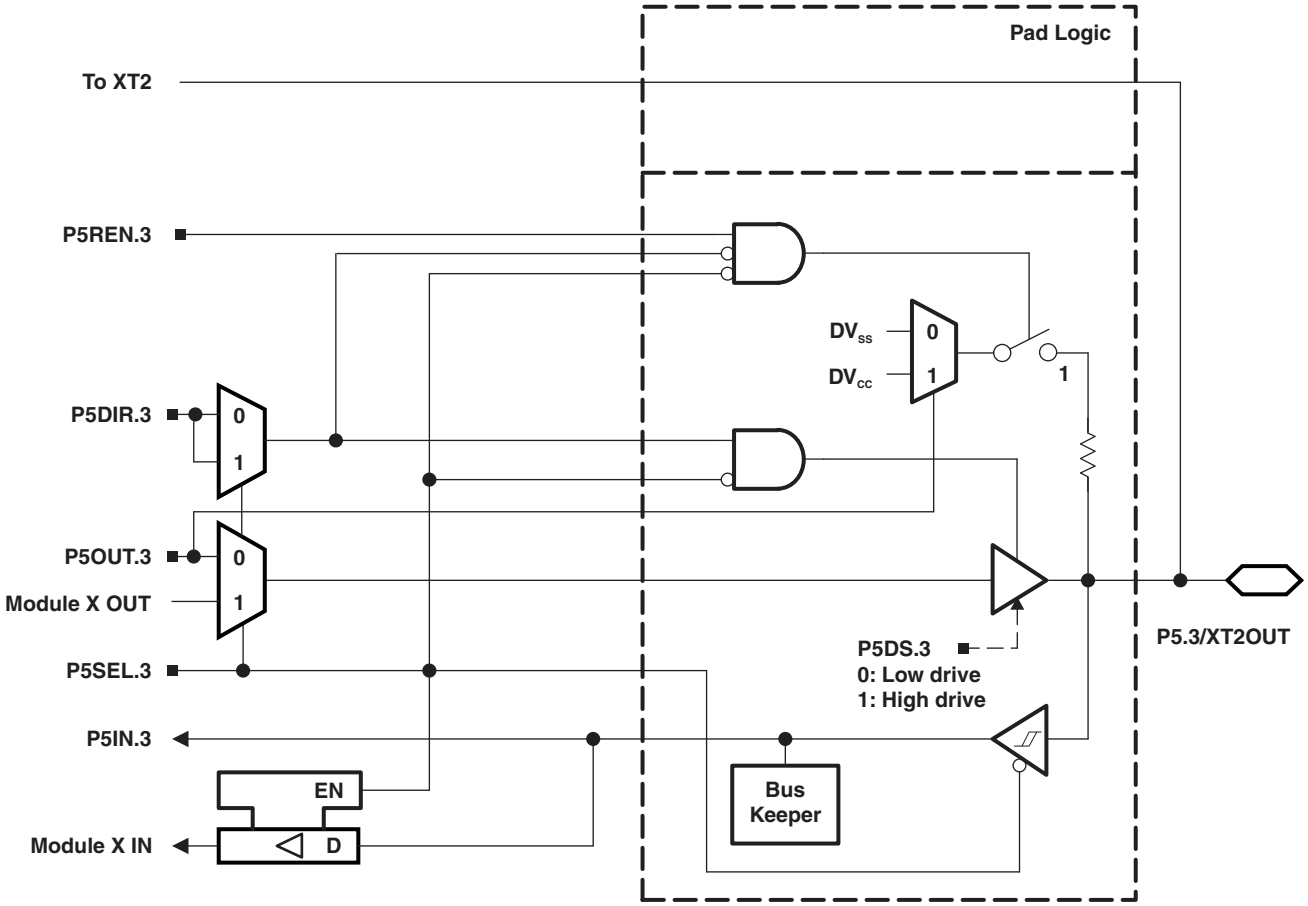
Port P5, P5.3, Input/Output With Schmitt Trigger



Port P5 (P5.2) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode(3)	X	1	X	0
		P5.3 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

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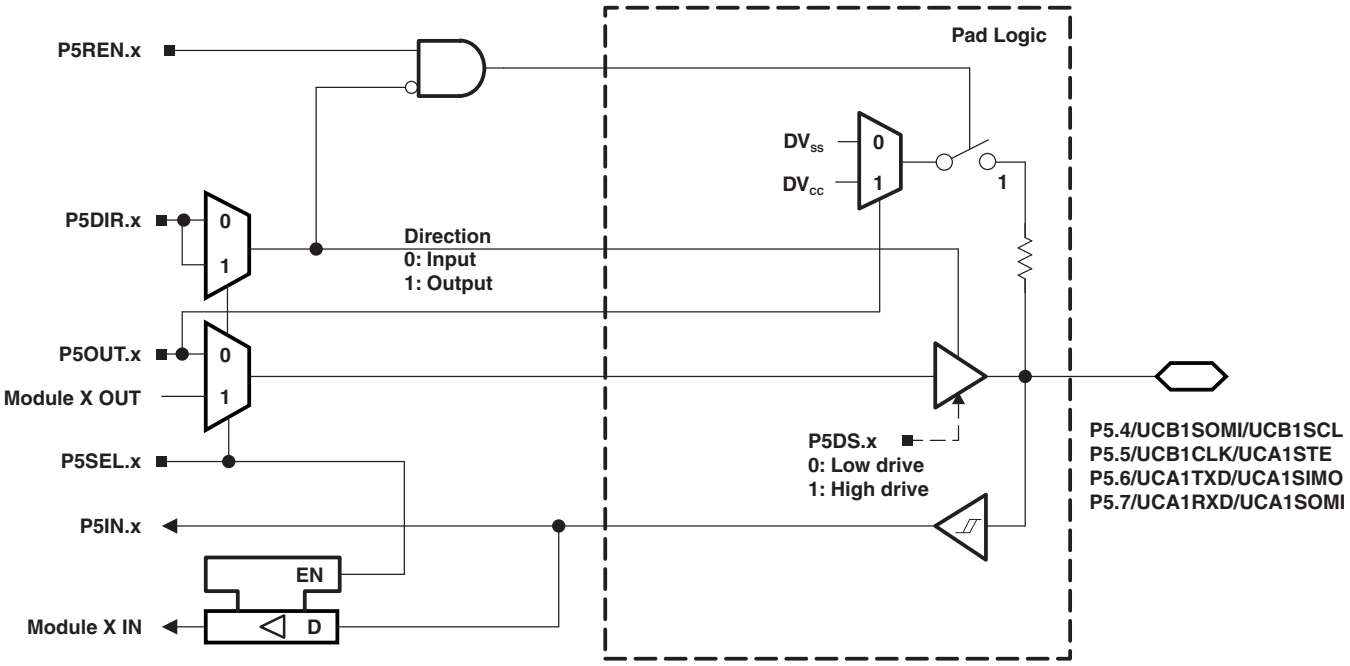
Port P5, P5.4 to P5.7, Input/Output With Schmitt Trigger



Port P5 (P5.4 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P5DIR.x	P5SEL.x
P5.4/UCB1SOMI/UCB1SCL	4	P5.4 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL[2][3]	X	1
P5.5/UCB1CLK/UCA1STE	5	P5.5 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE[2]	X	1
P5.6/UCA1TXD/UCA1SIMO	6	P5.6 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO[2]	X	1
P5.7/UCA1RXD/UCA1SOMI	7	P5.7 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI[2]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

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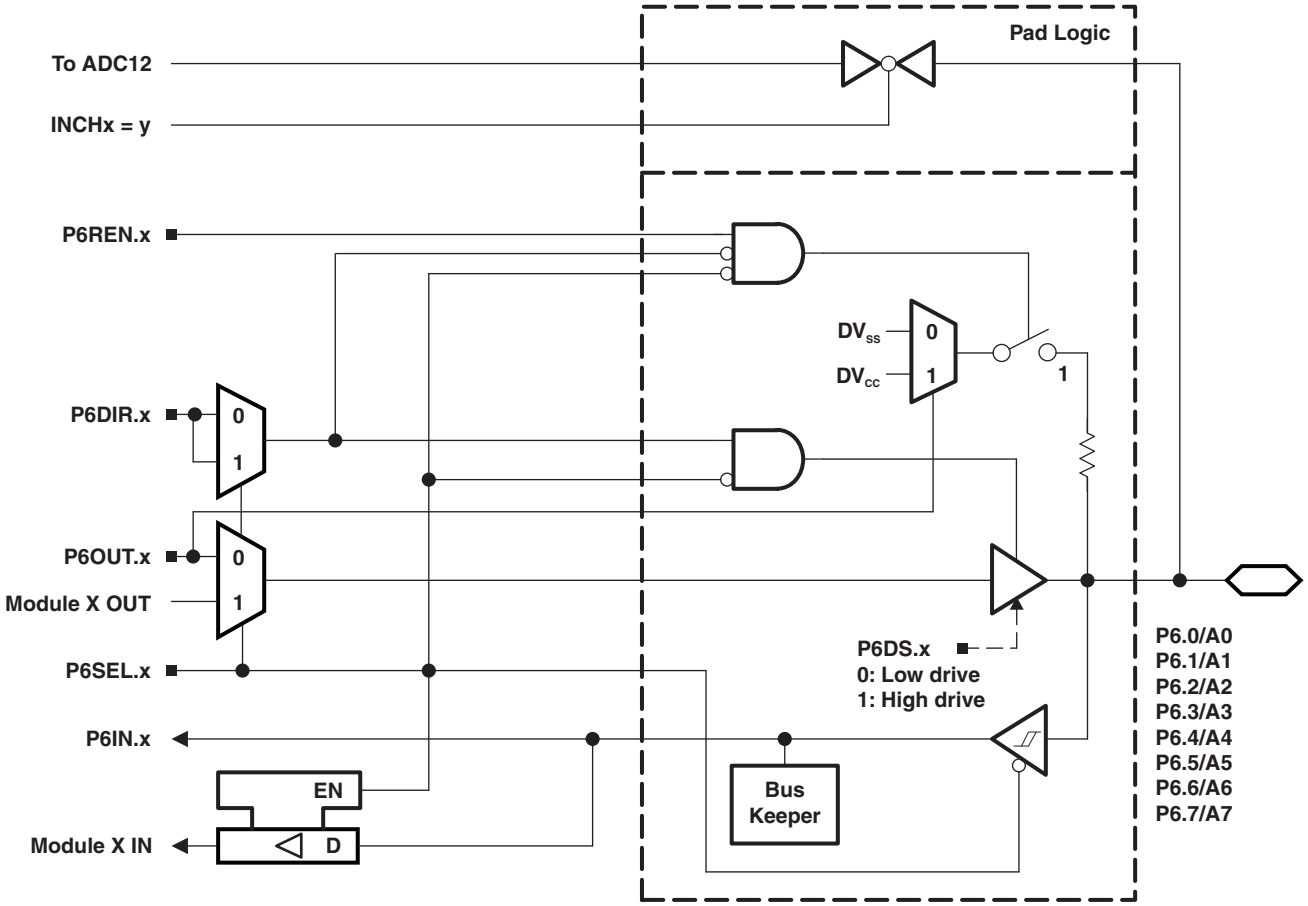
Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger



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Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]		
			P6DIR.x	P6SEL.x	INCHx
P6.0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	X
		A0[2][3]	X	X	0
P6.1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	X
		A1[2][3]	X	X	1
P6.2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	X
		A2[2][3]	X	X	2
P6.3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	X
		A3[2][3]	X	X	3
P6.4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	X
		A4[2][3]	X	X	4
P6.5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	X
		A5[1][2][3]	X	X	5
P6.6/A6	6	P6.6 (I/O)	I: 0; O: 1	0	X
		A6[2][3]	X	X	6
P6.7/A7	7	P6.7 (I/O)	I: 0; O: 1	0	X
		A7[2][3]	X	X	7

(1) X = Don't care
(2) Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

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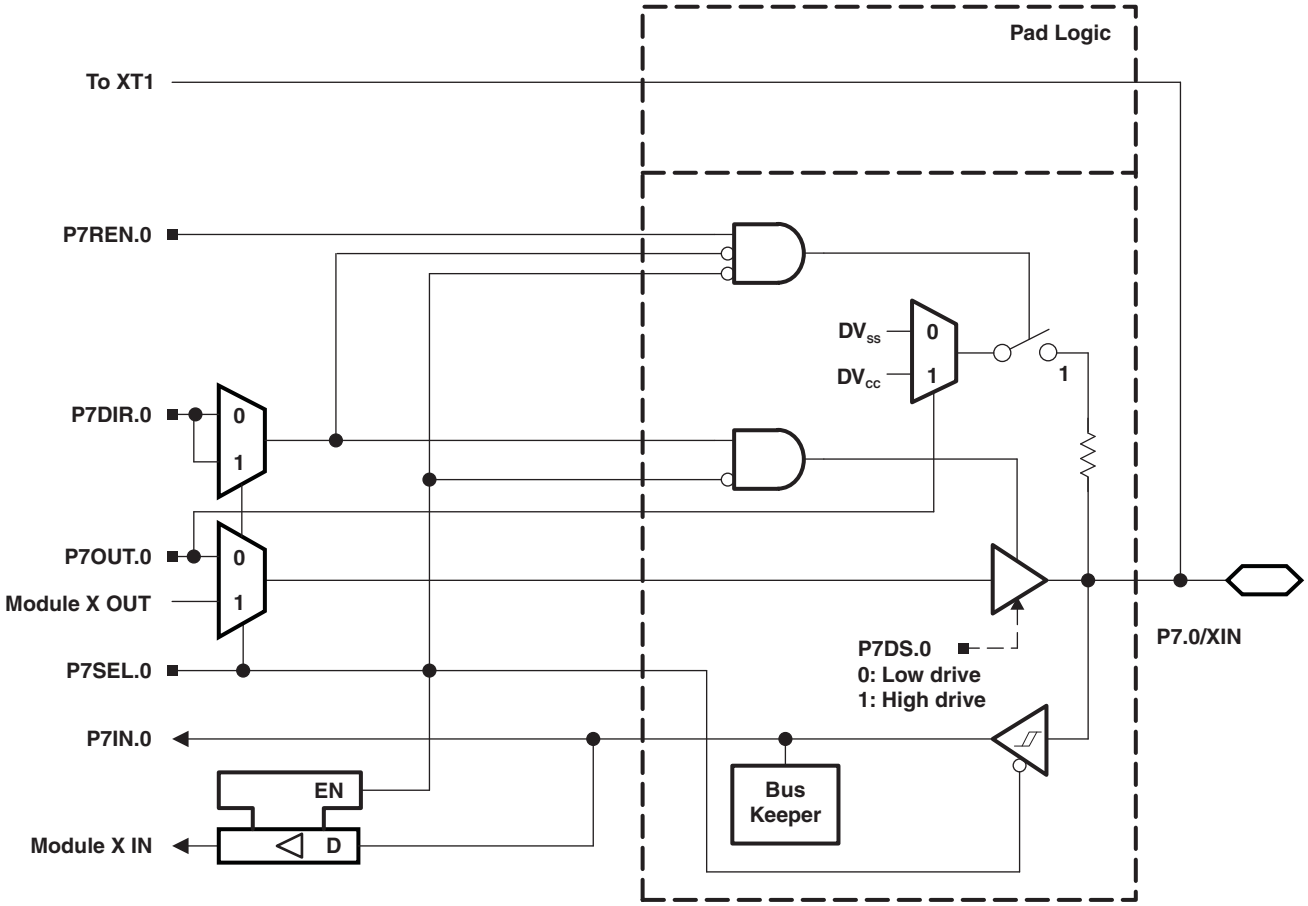
Port P7, P7.0, Input/Output With Schmitt Trigger



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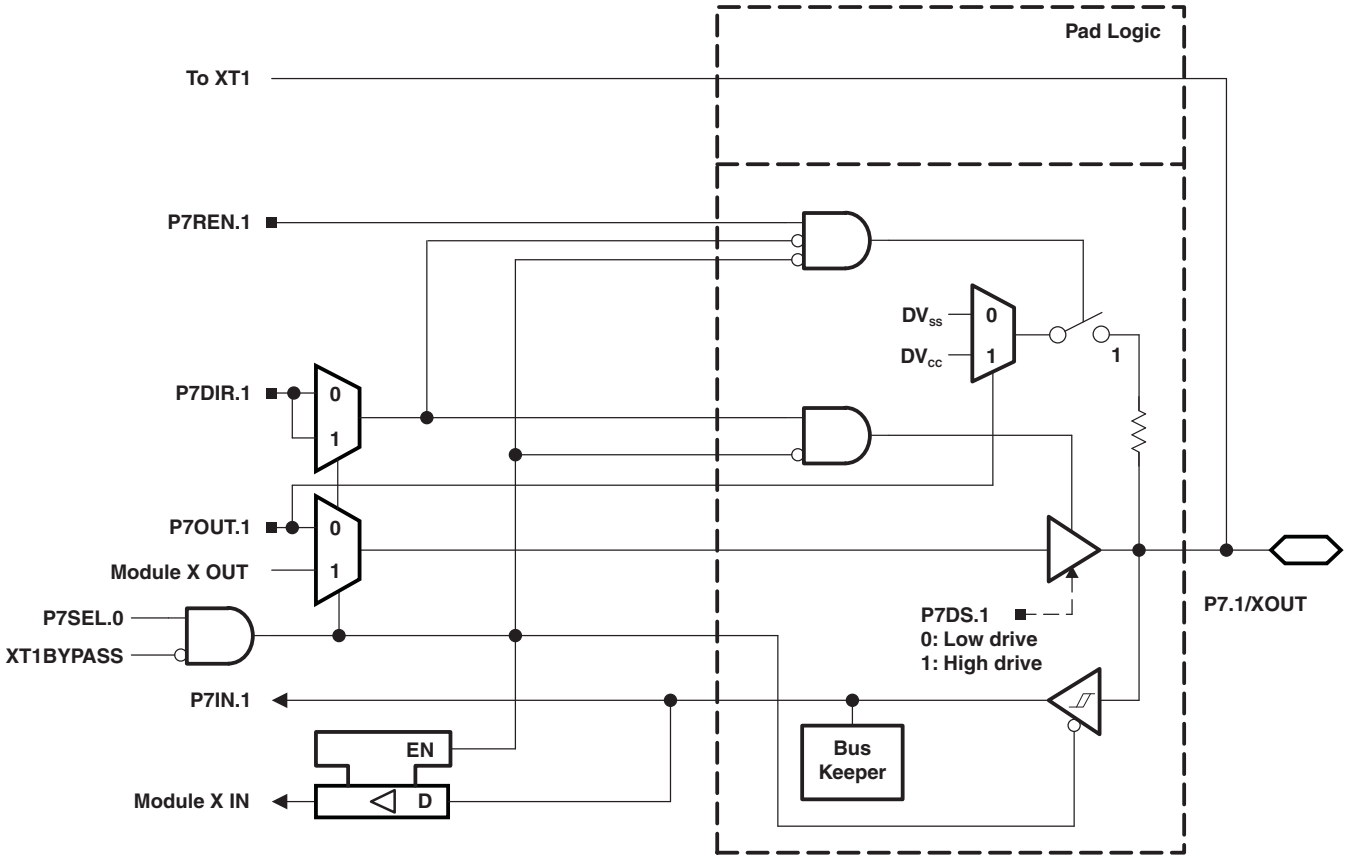
Port P7, P7.1, Input/Output With Schmitt Trigger



Port P7 (P7.0 and P7.1) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P7DIR.x	P7SEL.0	P7SEL.1	XT1BYPASS
P7.0/XIN	0	P7.0 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode(2)	X	1	X	0
		XIN bypass mode(2)	X	1	X	1
P7.1/XOUT	1	P7.1 (I/O)	I: 0; O: 1	0	X	X
		XOUT crystal mode(3)	X	1	X	0
		P7.1 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P7SEL.0 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P7.0 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.0 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.1 can be used as general-purpose I/O.

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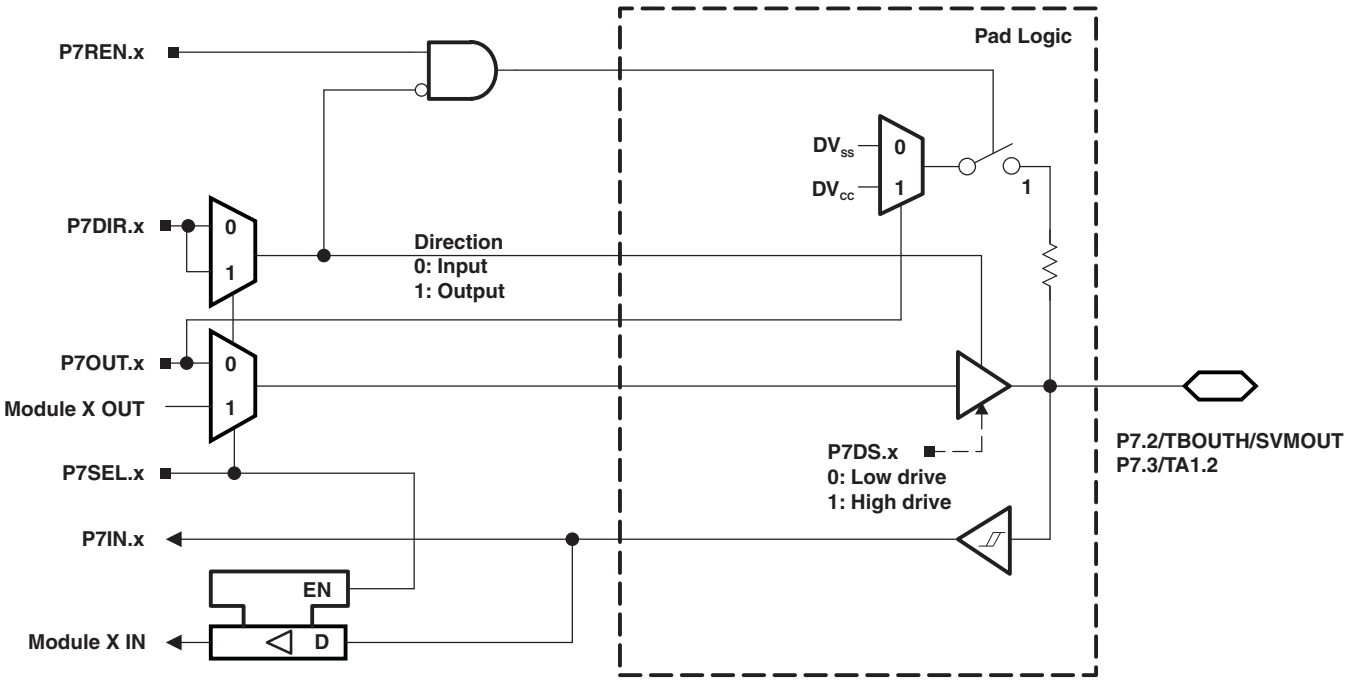
Port P7, P7.2 and P7.3, Input/Output With Schmitt Trigger



Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P7DIR.x	P7SEL.x
P7.2/TBOUTH/SVMOUT	2	P7.2 (I/O)	I: 0; O: 1	0
		TBOUTH	0	1
		SVMOUT	1	1
P7.3/TA1.2	3	P7.3 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI2B	0	1
		Timer1_A3.TA2	1	1

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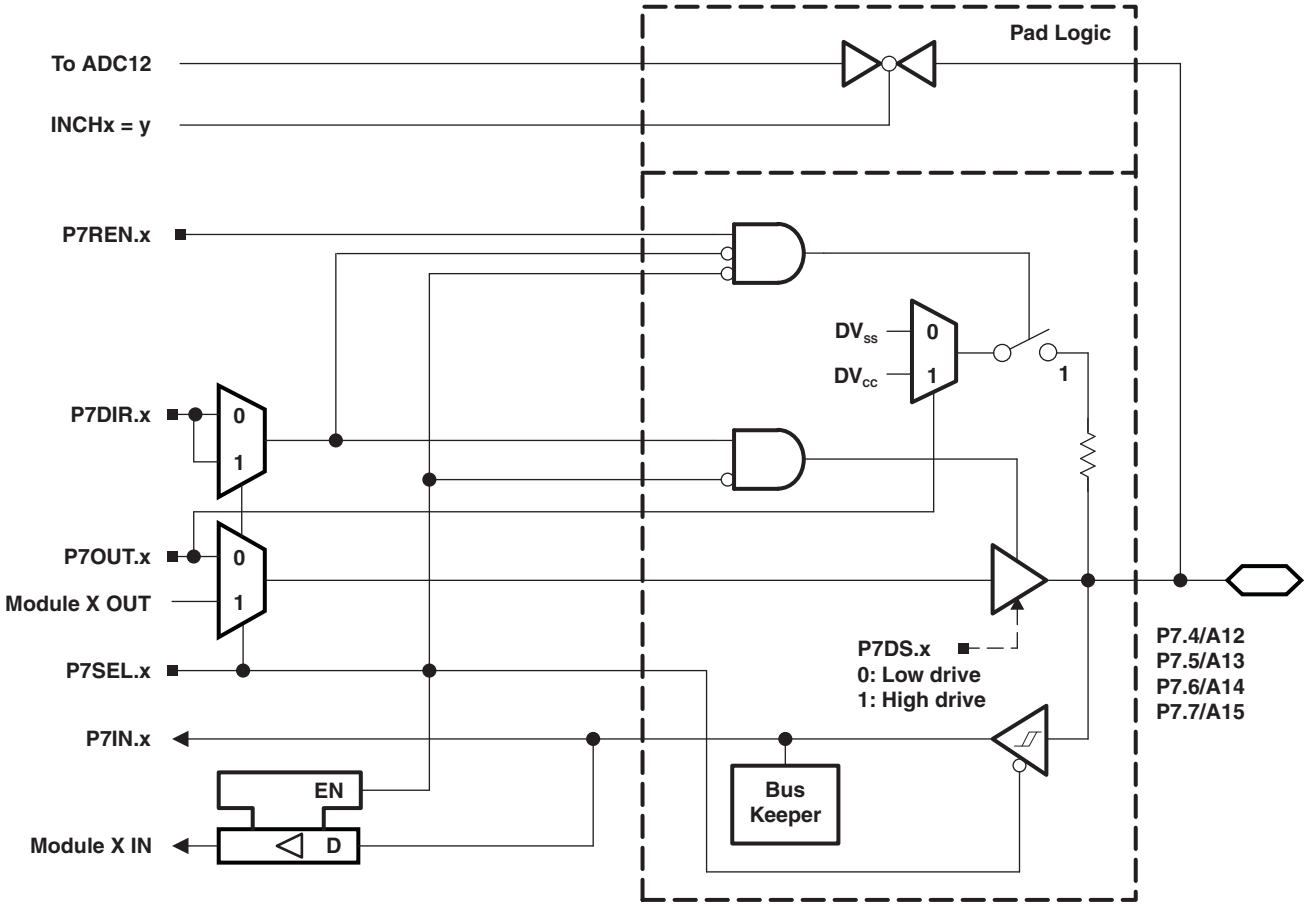
Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger



Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P7DIR.x	P7SEL.x	INCHx
P7.4/A12	4	P7.4 (I/O)	I: 0; O: 1	0	X
		A12(2)(3)	X	X	12
P7.5/A13	5	P7.5 (I/O)	I: 0; O: 1	0	X
		A13(4)(5)	X	X	13
P7.6/A14	6	P7.6 (I/O)	I: 0; O: 1	0	X
		A14(4)(5)	X	X	14
P7.7/A15	7	P7.7 (I/O)	I: 0; O: 1	0	X
		A15(4)(5)	X	X	15

(1) X = Don't care
(2) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.
(4) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(5) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

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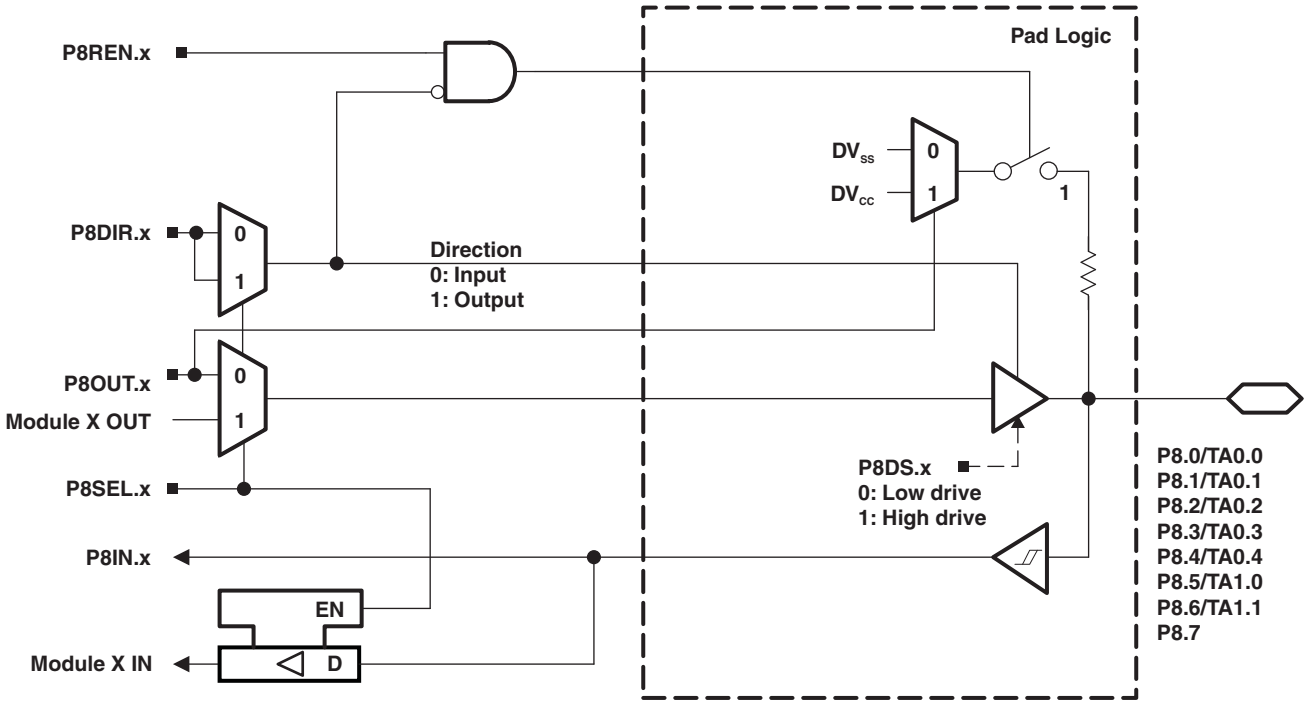
Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger



Port P8 (P8.0 to P8.7) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.0/TA0.0	0	P8.0 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI0B	0	1
		Timer0_A5.TA0	1	1
P8.1/TA0.1	1	P8.1 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI1B	0	1
		Timer0_A5.TA1	1	1
P8.2/TA0.2	2	P8.2 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI2B	0	1
		Timer0_A5.TA2	1	1
P8.3/TA0.3	3	P8.3 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI3B	0	1
		Timer0_A5.TA3	1	1
P8.4/TA0.4	4	P8.4 (I/O)	I: 0; O: 1	0
		Timer0_A5.CCI4B	0	1
		Timer0_A5.TA4	1	1
P8.5/TA1.0	5	P8.5 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI0B	0	1
		Timer1_A3.TA0	1	1
P8.6/TA1.1	6	P8.6 (I/O)	I: 0; O: 1	0
		Timer1_A3.CCI1B	0	1
		Timer1_A3.TA1	1	1
P8.7	7	P8.7 (I/O)	I: 0; O: 1	0

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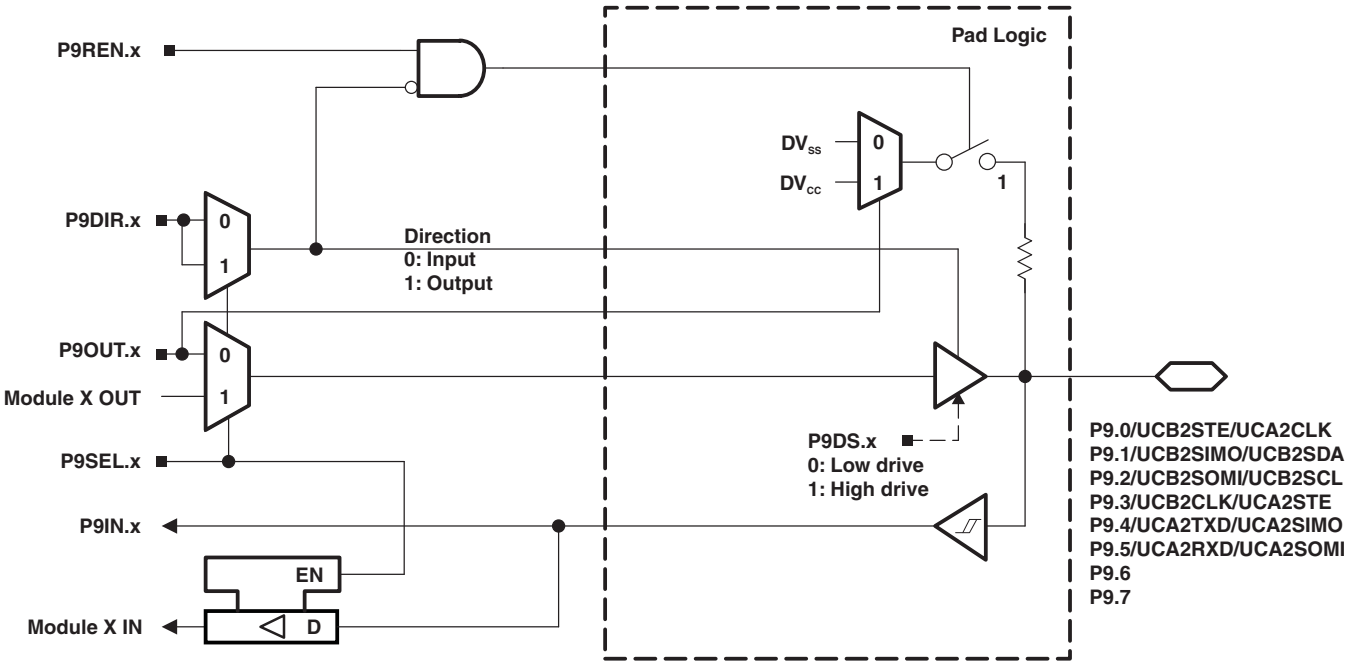
Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger



Port P9 (P9.0 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS[1]	
			P9DIR.x	P9SEL.x
P9.0/UCB2STE/UCA2CLK	0	P9.0 (I/O)	I: 0; O: 1	0
		UCB2STE/UCA2CLK[2][3]	X	1
P9.1/UCB2SIMO/UCB2SDA	1	P9.1 (I/O)	I: 0; O: 1	0
		UCB2SIMO/UCB2SDA[2][4]	X	1
P9.2/UCB2SOMI/UCB2SCL	2	P9.2 (I/O)	I: 0; O: 1	0
		UCB2SOMI/UCB2SCL[2][4]	X	1
P9.3/UCB2CLK/UCA2STE	3	P9.3 (I/O)	I: 0; O: 1	0
		UCB2CLK/UCA2STE[2]	X	1
P9.4/UCA2TXD/UCA2SIMO	4	P9.4 (I/O)	I: 0; O: 1	0
		UCA2TXD/UCA2SIMO[2]	X	1
P9.5/UCA2RXD/UCA2SOMI	5	P9.5 (I/O)	I: 0; O: 1	0
		UCA2RXD/UCA2SOMI[2]	X	1
P9.6	6	P9.6 (I/O)	I: 0; O: 1	0
P9.7	7	P9.7 (I/O)	I: 0; O: 1	0

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA2CLK function takes precedence over UCB2STE function. If the pin is required as UCA2CLK input or output, USCI A2/B2 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.

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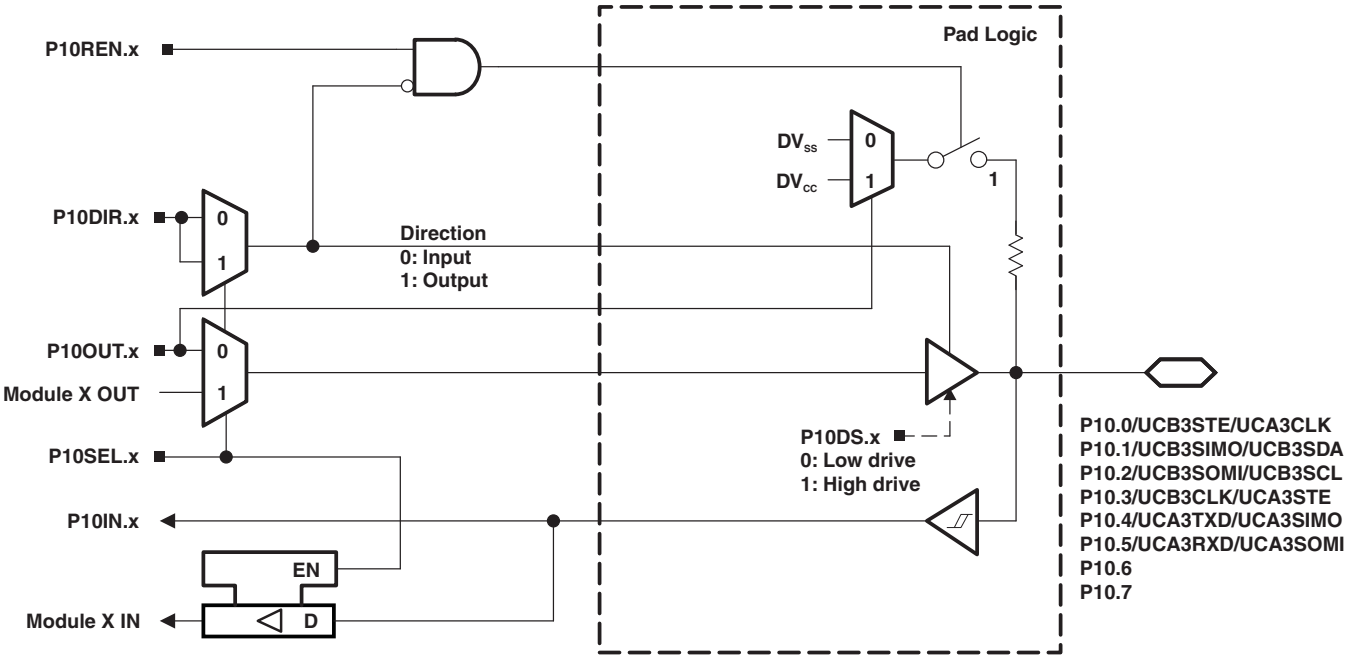
Port P10, P10.0 to P10.7, Input/Output With Schmitt Trigger



Port P10 (P10.0 to P10.7) Pin Functions

PIN NAME (P10.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)	
			P10DIR.x	P10SEL.x
P10.0/UCB3STE/UCA3CLK	0	P10.0 (I/O)	I: 0; O: 1	0
		UCB3STE/UCA3CLK (2) (3)	X	1
P10.1/UCB3SIMO/UCB3SDA	1	P10.1 (I/O)	I: 0; O: 1	0
		UCB3SIMO/UCB3SDA (2) (4)	X	1
P10.2/UCB3SOMI/UCB3SCL	2	P10.2 (I/O)	I: 0; O: 1	0
		UCB3SOMI/UCB3SCL (2) (4)	X	1
P10.3/UCB3CLK/UCA3STE	3	P10.3 (I/O)	I: 0; O: 1	0
		UCB3CLK/UCA3STE (2)	X	1
P10.4/UCA3TXD/UCA3SIMO	4	P10.4 (I/O)	I: 0; O: 1	0
		UCA3TXD/UCA3SIMO (2)	X	1
P10.5/UCA3RXD/UCA3SOMI	5	P10.5 (I/O)	I: 0; O: 1	0
		UCA3RXD/UCA3SOMI (2)	X	1
P10.6	6	P10.6 (I/O)	I: 0; O: 1	0
		Reserved (5)	X	1
P10.7	7	P10.7 (I/O)	I: 0; O: 1	0
		Reserved (5)	x	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA3CLK function takes precedence over UCB3STE function. If the pin is required as UCA3CLK input or output, USCI A3/B3 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(4) If the I2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(5) The secondary function on these pins are reserved for factory test purposes. Application should keep the P10SEL.x of these ports cleared to prevent potential conflicts with the application.

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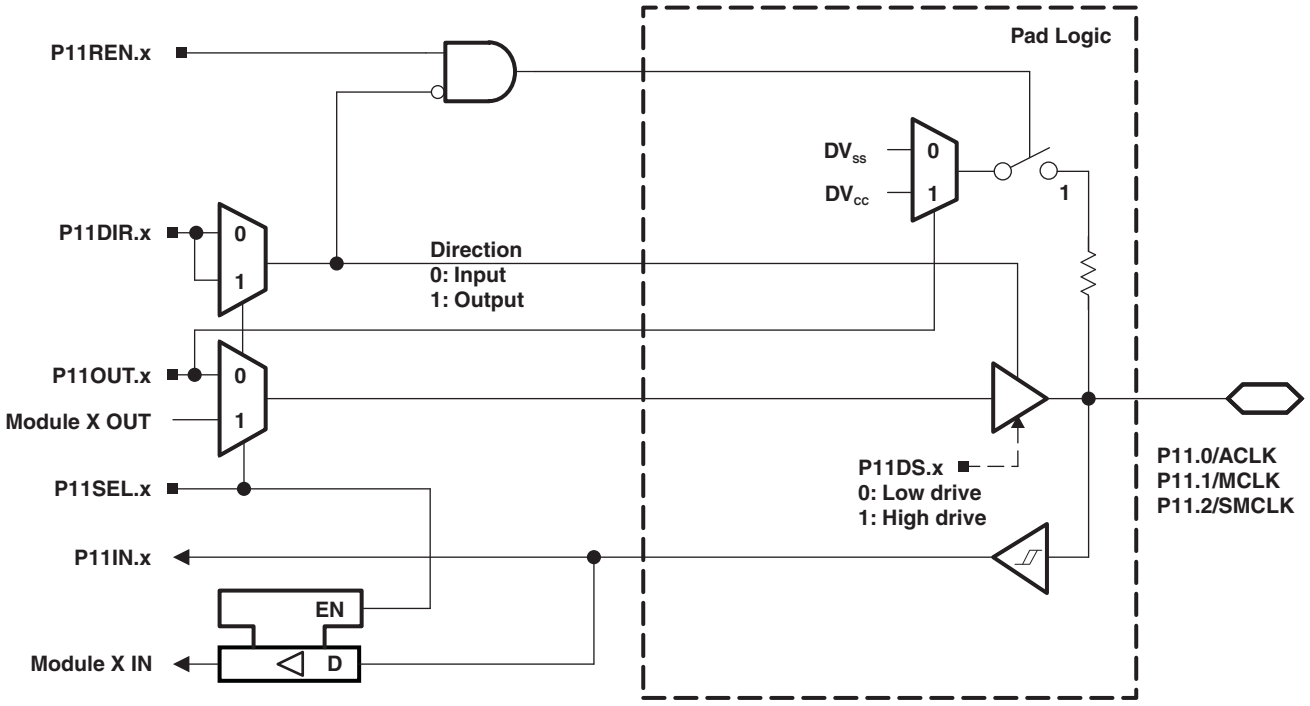
Port P11, P11.0 to P11.2, Input/Output With Schmitt Trigger



Port P11 (P11.0 to P11.2) Pin Functions

PIN NAME (P11.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P11DIR.x	P11SEL.x
P11.0/ACLK	0	P11.0 (I/O)	I: 0; O: 1	0
		ACLK	1	1
P11.1/MCLK	1	P11.1 (I/O)	I: 0; O: 1	0
		MCLK	1	1
P11.2/SMCLK	2	P11.2 (I/O)	I: 0; O: 1	0
		SMCLK	1	1

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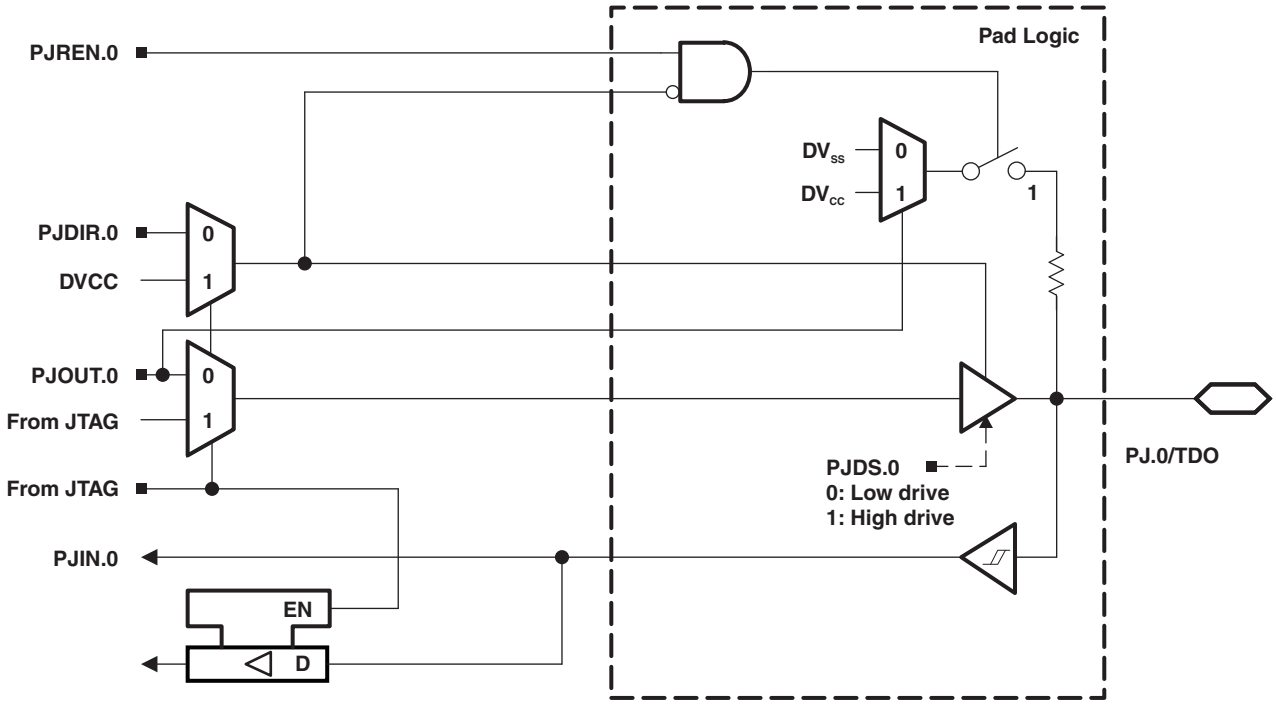
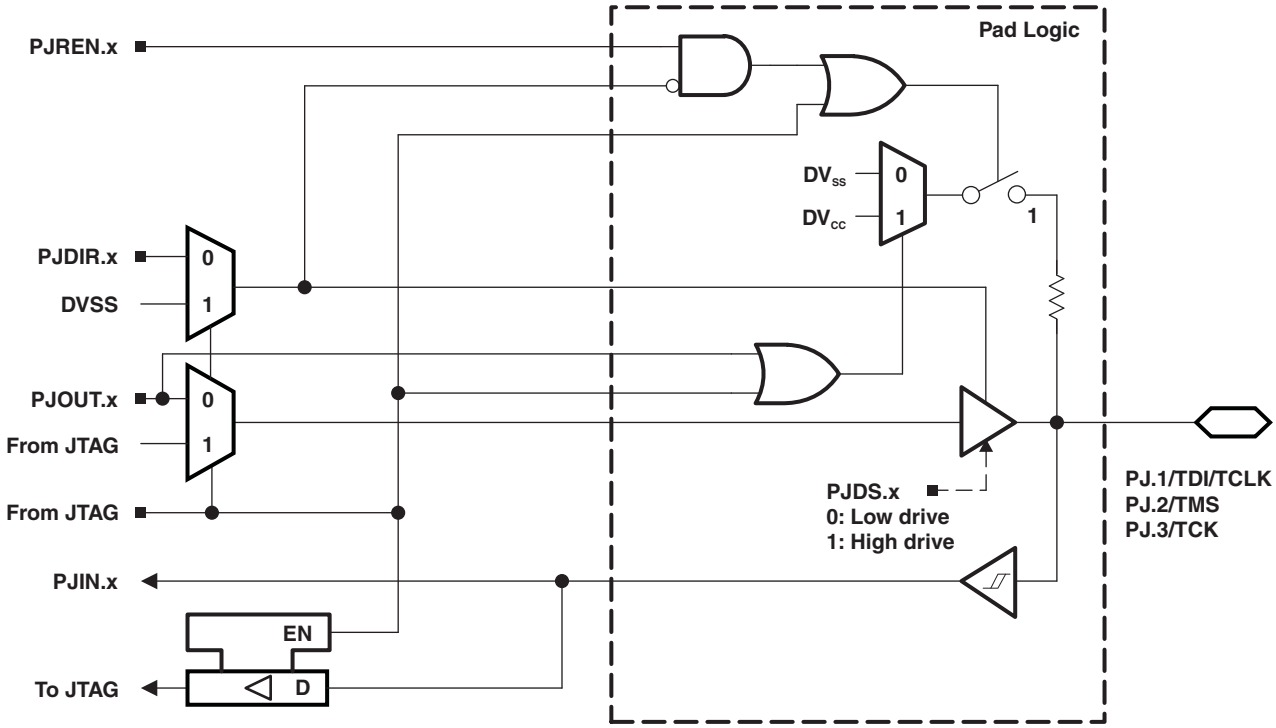
Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output



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Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)[2]	I: 0; O: 1
		TDO[3]	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)[2]	I: 0; O: 1
		TDI/TCLK[3][4]	X
PJ.2/TMS	2	PJ.2 (I/O)[2]	I: 0; O: 1
		TMS[3][4]	X
PJ.3/TCK	3	PJ.3 (I/O)[2]	I: 0; O: 1
		TCK[3][4]	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

PRODUCT PREVIEW

Data Sheet Revision History

REVISION	DESCRIPTION
SLAS609	Product Preview data sheet release

PRODUCT PREVIEW

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MSP430F5418IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5419IPZ	PREVIEW	LQFP	PZ	100	50	TBD	Call TI	Call TI
MSP430F5435IPN	PREVIEW	LQFP	PN	80	50	TBD	Call TI	Call TI
MSP430F5436IPZ	PREVIEW	LQFP	PZ	100	50	TBD	Call TI	Call TI
MSP430F5437IPN	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430F5438IPZ	PREVIEW	LQFP	PZ	100	50	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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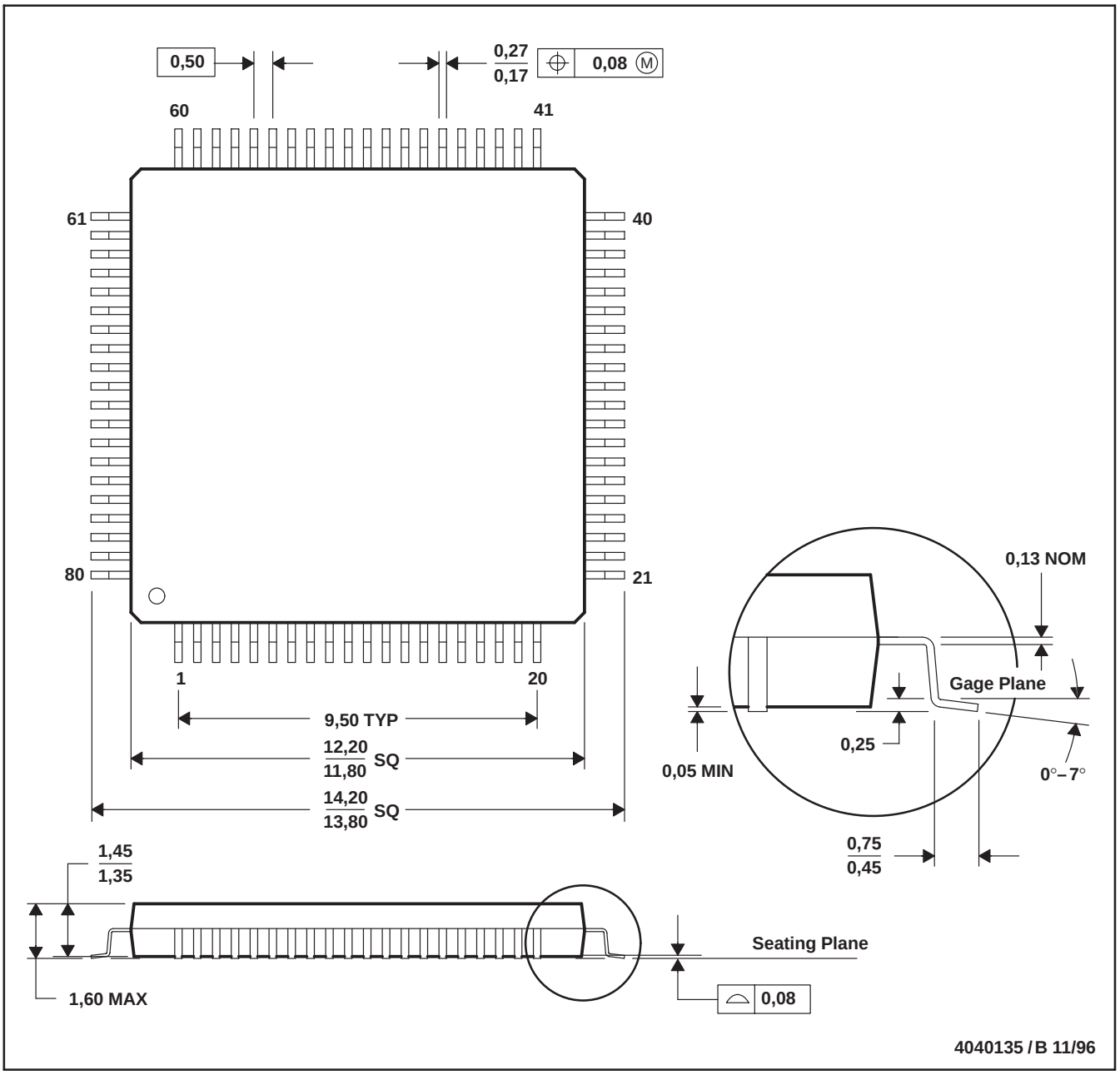
MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

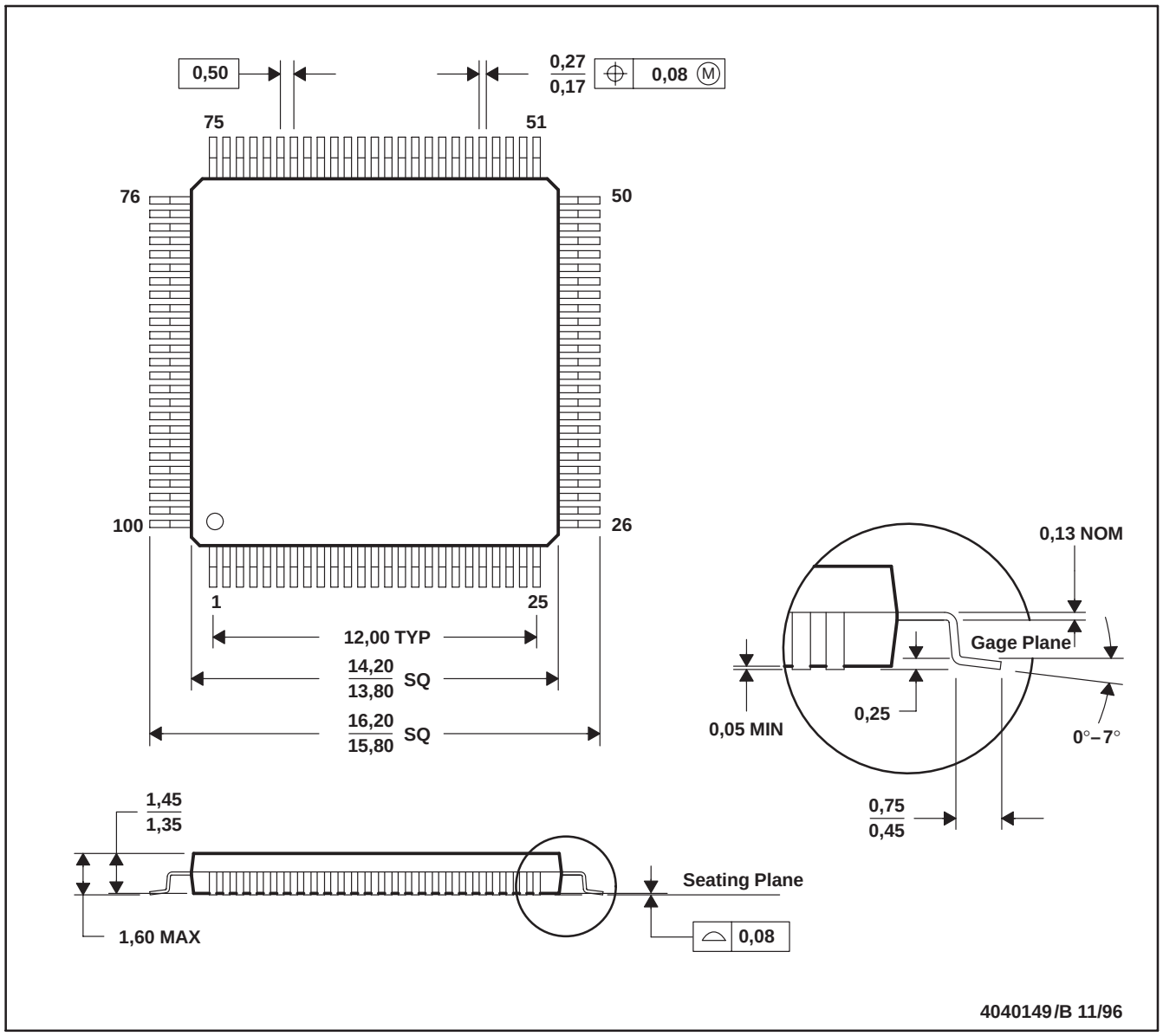
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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