

24-Bit, 192 kHz Stereo Audio CODEC

D/A Features

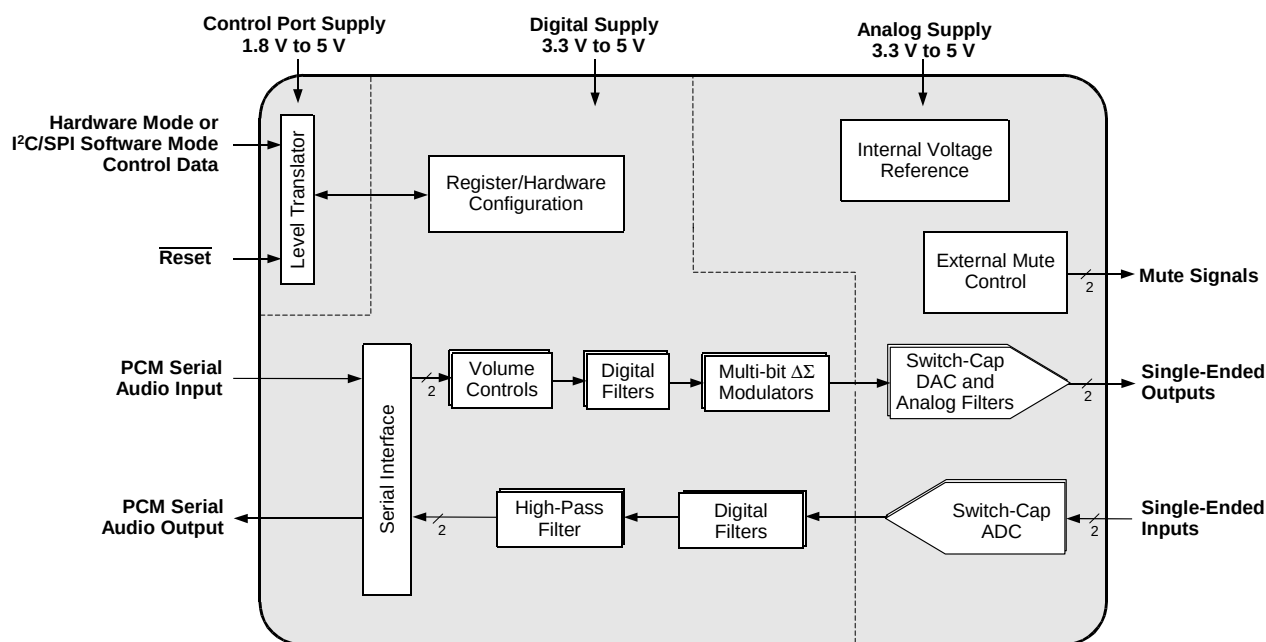
- ◆ High Performance
 - 105 dB Dynamic Range
 - -95 dB THD+N
- ◆ Selectable Serial Audio Interface Formats
 - Left-Justified up to 24-bit
 - I²S up to 24-bit
 - Right-Justified 16-, and 24-Bit
- ◆ Control Output for External Muting
- ◆ On-Chip Digital De-Emphasis
- ◆ Popguard Technology
- ◆ Multi-bit $\Delta\Sigma$ Conversion
- ◆ Digital Volume Control

A/D Features

- ◆ High Performance
 - 105 dB Dynamic Range
 - -95 dB THD+N
- ◆ Multi-bit Delta Sigma Conversion
- ◆ High-Pass Filter to remove DC Offsets
- ◆ Selectable Serial Audio Interface Formats
 - Left-Justified up to 24-bit
 - I²S up to 24-bit

System Features

- ◆ Direct Interface with Logic Levels 1.8 V to 5 V
- ◆ Internal Digital Loopback
- ◆ Stand-Alone or Control Port Functionality
- ◆ Single-Ended Analog Architecture
- ◆ Supports all Audio Sample Rates from 4 kHz to 216 kHz



Stand-Alone Mode Feature Set

- ◆ System Features
 - Serial Audio Port Master or Slave Operation
 - Single, Double, or Quad-Speed Operation
- ◆ D/A Features
 - Auto-mute on Static Samples
 - 44.1 kHz 50/15 μ s De-emphasis Available
 - Selectable Serial Audio Interface Formats
 - ◆ Left-Justified up to 24-bit
 - ◆ I²S up to 24-bit
- ◆ A/D Features
 - High-Pass Filter
 - Selectable Serial Audio Interface Formats
 - ◆ Left-Justified up to 24-bit
 - ◆ I²S up to 24-bit

Software Mode Feature Set

- ◆ System Features
 - Serial Audio Port Master or Slave Operation
 - Internal Digital Loopback Available
- ◆ D/A Features
 - Selectable Auto-mute
 - 44.1-kHz De-emphasis Filters
 - Configurable Muting Controls
 - Volume Control
 - Selectable Serial Audio Interface Formats
 - ◆ Left-Justified up to 24-bit
 - ◆ I²S up to 24-bit
 - ◆ Right Justified 16, and 24-bit
- ◆ A/D Features
 - Selectable High-Pass Filter or DC Offset Calibration
 - Selectable Serial Audio Interface Formats
 - ◆ Left-Justified up to 24-bit
 - ◆ I²S up to 24-bit

General Description

The CS4270 is a high-performance, integrated audio CODEC. The CS4270 performs stereo analog-to-digital (A/D) and digital-to-analog (D/A) conversion of up to 24-bit serial values at sample rates up to 216 kHz.

Standard 50/15 μ s de-emphasis is available for sampling rates of 44.1 kHz for compatibility with digital audio programs mastered using the 50/15 μ s pre-emphasis technique.

Integrated level translators allow easy interfacing between the CS4270 and other devices operating over a wide range of logic levels.

Independently addressable high-pass filters are available for the right and left channel of the A/D. This allows the A/D to be used in a wide variety of applications where one audio channel and one DC measurement channel is desired.

The CS4270's wide dynamic range, negligible distortion, and low noise make it ideal for applications such as DVD-recorders, digital televisions, set top boxes, effects processors, and automotive audio systems.

ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4270	24-Bit 192 kHz Stereo Audio CODEC	24-TSSOP	YES	Commercial	-10° to +85° C	Rail	CS4270-CZZ
						Tape & Reel	CS4270-CZZR
CS4270	24-Bit 192 kHz Stereo Audio CODEC	24-TSSOP	YES	Commercial	-40° to +85° C	Rail	CS4270-DZZ
						Tape & Reel	CS4270-DZZR
CDB4270	CS4270 Evaluation Board	-	-	-	-	-	CDB4270

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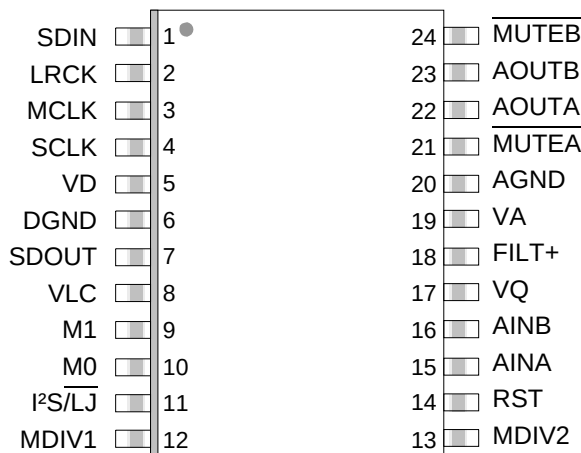
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1. PIN DESCRIPTIONS - SOFTWARE MODE

SDIN	1	24	MUTEB
LRCK	2	23	AOUTB
MCLK	3	22	AOUTA
SCLK	4	21	MUTEA
VD	5	20	AGND
DGND	6	19	VA
SDOUT	7	18	FILT+
VLC	8	17	VQ
SDA/CDOUT	9	16	AINB
SCL/CCLK	10	15	AINA
AD0/CS	11	14	RST
AD1/CDIN	12	13	AD2

Pin Name	#	Pin Description
SDIN	1	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
LRCK	2	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	Serial Clock (Input/Output) - Serial clock for the serial audio interface.
VD	5	Digital Power (Input) - Positive power supply for the digital section.
DGND	6	Digital Ground (Input) - Ground reference for the internal digital section.
SDOUT	7	Serial Audio Data Output (Output) - Output for two's complement serial audio data.
VLC	8	Control Port Power (Input) - Determines the signal level for the control port.
SDA/CDOUT	9	Serial Control Data (Input/Output) - SDA is a data I/O in I ² C mode. CDOUT is the output data line for the control port interface in SPI mode.
SCL/CCLK	10	Serial Control Port Clock (Input) - Serial clock for the serial control port.
AD0/CS	11	Address Bit 0 (I²C) / Control Port Chip Select (SPI) (Input) - AD0 is a chip address pin in I ² C mode. CS is the chip select signal for SPI format.
AD1/CDIN	12	Address Bit 1 (I²C) / Serial Control Data (Input) - AD1 is a chip address pin in I ² C mode. CDIN is the input data line for the control port interface in SPI mode.
AD2	13	Address Bit 2 (I²C) (Input) - AD2 is a chip address pin in I ² C mode.
RST	14	Reset (Input) - The device enters a low power mode when low.
AINA	15	Analog Input (Input) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
AINB	16	
VQ	17	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.
FILT+	18	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
VA	19	Analog Power (Input) - Positive power for the analog sections.
AGND	20	Analog Ground (Input) - Ground reference. Must be connected to analog ground.
MUTEA	21	Mute Control (Output) - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
MUTEB	24	
AOUTA	22	Analog Audio Output (Output) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AOUTB	23	

2. PIN DESCRIPTIONS - STAND-ALONE MODE



Pin Name	#	Pin Description
SDIN	1	Serial Audio Data Input (Input) - Input for two's complement serial audio data.
LRCK	2	Left Right Clock (Input/Output) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	3	Master Clock (Input) - Clock source for the delta-sigma modulator and digital filters.
SCLK	4	Serial Clock (Input/Output) - Serial clock for the serial audio interface.
VD	5	Digital Power (Input) - Positive power supply for the digital section.
DGND	6	Digital Ground (Input) - Ground reference for the internal digital section.
SDOUT (M/S)	7	Serial Audio Data Output (Output) - Output for two's complement serial audio data. This pin must be pulled-up or pulled-down to select Master or Slave Mode.
VLC	8	Control Port Power (Input) - Determines the signal level for the control port.
M1	9	Mode Selection (Input) - Determines the operational mode of the device.
M0	10	
I ² S/LJ	11	Serial Audio Interface Select (Input) - Selects either the left-justified or I ² S format for the Serial Audio Interface.
MDIV1	12	MCLK Divide (Input) - Configures MCLK divider to divide by 1, 1.5, 2, or 4.
MDIV2	13	
RST	14	Reset (Input) - The device enters a low power mode when low.
AINA	15	Analog Input (Input) - The full-scale analog input level is specified in the ADC Analog Characteristics specification table.
AINB	16	
VQ	17	Quiescent Voltage (Output) - Filter connection for internal quiescent voltage.
FILT+	18	Positive Voltage Reference (Output) - Positive reference voltage for the internal sampling circuits.
VA	19	Analog Power (Input) - Positive power for the analog sections.
AGND	20	Analog Ground (Input) - Ground reference. Must be connected to analog ground.
MUTEA	21	Mute Control (Output) - Each pin is active during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down.
MUTEB	24	
AOUTA	22	Analog Audio Output (Output) - The full-scale output level is specified in the DAC Analog Characteristics specification table.
AOUTB	23	

3. CHARACTERISTICS AND SPECIFICATIONS

(All Min/Max characteristics and specifications are guaranteed over the [Specified Operating Conditions](#). Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and $T_A = 25^{\circ}\text{C}$.)

SPECIFIED OPERATING CONDITIONS

(AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Nom	Max	Units
DC Power Supplies:					
Analog	VA	3.1	5.0	5.25	V
Digital	VD	3.1	3.3	5.25	V
Control Port Interface	VLC	1.7	3.3	5.25	V
Ambient Operating Temperature (Power Applied)	(-CZZ) T_{A-CZZ}	-10	-	+70	$^{\circ}\text{C}$
	(-DZZ) T_{A-DZZ}	-40	-	+85	$^{\circ}\text{C}$

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V, All voltages with respect to ground.) ([Note 1](#))

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Analog	VA	-0.3	-	+6.0	V
Digital	VD	-0.3	-	+6.0	V
Control Port Interface	VLC	-0.3	-	+6.0	V
Input Current (Note 2)	I_{in}	-10	-	+10	mA
Analog Input Voltage	V_{IN}	AGND-0.7	-	VA+0.7	V
Digital Input Voltage					
Control Port Interface	V_{IND-C}	-0.3	-	VLC+0.3	V
Digital Interface	V_{IND-D}	-0.3	-	VD+0.3	V
Ambient Operating Temperature (Power Applied)	T_{AC}	-50	-	+95	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-65	-	+150	$^{\circ}\text{C}$

Notes:

- Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.
- Any pin except supplies. Transient currents of up to ± 100 mA on the analog input pins will not cause SRC latch-up.

THERMAL CHARACTERISTICS

Parameters	Symbol	Min	Typ	Max	Units
Allowable Junction Temperature		-	-	135	$^{\circ}\text{C}$
Junction to Ambient Thermal Impedance (Note 3)					
(Multi-layer PCB) TSSOP	θ_{JA-TM}	-	70	-	$^{\circ}\text{C/W}$
(Multi-layer PCB) SOIC	θ_{JA-SM}	-	60	-	$^{\circ}\text{C/W}$
(Single-layer PCB) TSSOP	θ_{JA-TS}	-	105	-	$^{\circ}\text{C/W}$
(Single-layer PCB) SOIC	θ_{JA-SS}	-	80	-	$^{\circ}\text{C/W}$

- θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

DAC ANALOG CHARACTERISTICS (CS4270-CZZ)

(Full-Scale Output Sine Wave, 997 Hz (Note 4), $F_s = 48/96/192$ kHz; Test load $R_L = 3\text{ k}\Omega$, $C_L = 10\text{ pF}$ (see [Figure 1](#)). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5V			VA = 3.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Range	18 to 24-Bit	A-weighted	99	105	-	97	103	-	dB
		unweighted	96	102	-	94	100	-	dB
	16-Bit	A-weighted	90	96	-	90	96	-	dB
		unweighted	87	93	-	87	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-89	-	-95	-89	dB
		-20 dB	-	-82	-76	-	-80	-74	dB
		-60 dB	-	-42	-36	-	-40	-34	dB
	16-Bit	0 dB	-	-93	-87	-	-93	-87	dB
		-20 dB	-	-73	-67	-	-73	-67	dB
		-60 dB	-	-33	-27	-	-33	-27	dB

DAC ANALOG CHARACTERISTICS (CS4270-DZZ)

(Full-Scale Output Sine Wave, 997 Hz (Note 4), $F_s = 48/96/192$ kHz; Test load $R_L = 3\text{ k}\Omega$, $C_L = 10\text{ pF}$ (see [Figure 1](#)). Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified.)

Parameter			VA = 5V			VA = 3.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
Dynamic Range	18 to 24-Bit	A-weighted	95	105	-	93	103	-	dB
		unweighted	92	102	-	90	100	-	dB
	16-Bit	A-weighted	86	96	-	86	96	-	dB
		unweighted	83	93	-	83	93	-	dB
Total Harmonic Distortion + Noise									
	18 to 24-Bit	0 dB	-	-95	-85	-	-95	-85	dB
		-20 dB	-	-82	-72	-	-80	-70	dB
		-60 dB	-	-42	-32	-	-40	-30	dB
	16-Bit	0 dB	-	-93	-83	-	-93	-83	dB
		-20 dB	-	-73	-63	-	-73	-63	dB
		-60 dB	-	-33	-23	-	-33	-23	dB

- One-half LSB of triangular PDF dither added to data.

DAC ANALOG CHARACTERISTICS - ALL MODES

Parameter	Symbol	Min	Typ	Max	Unit
Interchannel Isolation (1 kHz)		-	100	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	0.25	dB
Gain Drift		-100		+100	ppm/°C
Analog Output					
Full Scale Output Voltage		$0.640 \cdot V_A$	$0.688 \cdot V_A$	$0.739 \cdot V_A$	V _{pp}
Max DC Current draw from AOUTA or AOUTB	I_{OUTmax}	-	10	-	μA
Max AC-Load Resistance (see Figure 2)	R_L	-	3	-	kΩ
Max Load Capacitance (see Figure 2)	C_L	-	100	-	pF
Output Impedance of AOUTA and AOUTB	Z_{OUT}	-	100	-	Ω

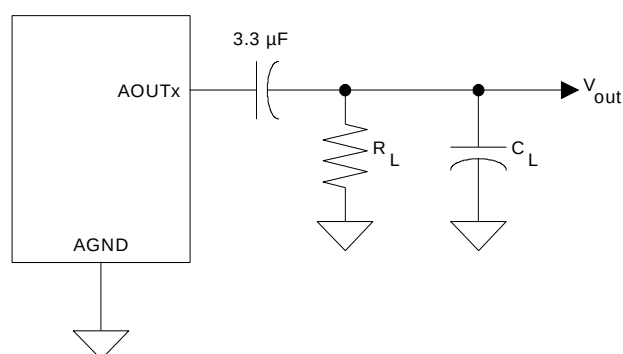


Figure 1. Output Test Load

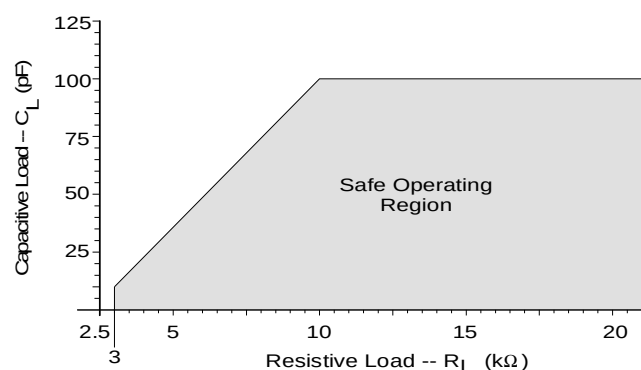


Figure 2. Maximum Loading

DAC COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

(The filter characteristics have been normalized to the sample rate (F_s) and can be referenced to the desired sample rate by multiplying the given characteristic by F_s .) (See [Note 5](#))

Parameter	Symbol	Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Note 6)	to -0.05 dB corner to -3 dB corner	0	-	.4780	F_s
		0	-	.4996	F_s
Frequency Response 10 Hz to 20 kHz		-.01	-	+.08	dB
StopBand		.5465	-	-	F_s
StopBand Attenuation (Note 7)		50	-	-	dB
Group Delay	tgd	-	10/ F_s	-	s
De-emphasis Error (Note 8)	$F_s = 32$ kHz	-	-	+1.5/+0	dB
	$F_s = 44.1$ kHz	-	-	+.05/- .25	dB
	$F_s = 48$ kHz	-	-	-.2/- .4	dB
Double-Speed Mode					
Passband (Note 6)	to -0.1 dB corner to -3 dB corner	0	-	.4650	F_s
		0	-	.4982	F_s
Frequency Response 10 Hz to 20 kHz		-.05	-	+.2	dB
StopBand		.5770	-	-	F_s
StopBand Attenuation (Note 7)		55	-	-	dB
Group Delay	tgd	-	5/ F_s	-	s
Quad-Speed Mode					
Passband (Note 6)	to -0.1 dB corner to -3 dB corner	0	-	0.397	F_s
		0	-	0.476	F_s
Frequency Response 10 Hz to 20 kHz		0	-	+0.00004	dB
StopBand		0.7	-	-	F_s
StopBand Attenuation (Note 7)		51	-	-	dB
Group Delay	tgd	-	2.5/ F_s	-	s

- Amplitude vs. Frequency plots of this data are available in [Section 11. "Appendix" on page 42](#). See [Figures 19 through 42](#).
- Response is clock dependent and will scale with F_s .
- For Single-Speed Mode, the Measurement Bandwidth is 0.5465 F_s to 3 F_s .
For Double-Speed Mode, the Measurement Bandwidth is 0.577 F_s to 1.4 F_s .
For Quad-Speed Mode, the Measurement Bandwidth is 0.7 F_s to 1 F_s .
- De-emphasis is available only in Single-Speed Mode.

ADC ANALOG CHARACTERISTICS (CS4270-CZZ)

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.

Parameter	Symbol	VA = 5V			VA = 3.3V			Unit	
		Min	Typ	Max	Min	Typ	Max		
Single-Speed Mode Fs = 48 kHz									
Dynamic Range A-weighted		99	105	-	96	102	-	dB	

9. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS (CS4270-DZZ)

Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Input is 1 kHz sine wave.

Parameter	Symbol	VA = 5V			VA = 3.3V			Unit	
		Min	Typ	Max	Min	Typ	Max		
Single-Speed Mode Fs = 48 kHz									
Dynamic Range A-weighted		97	105	-	94	102	-	dB	

10. Referred to the typical full-scale input voltage.

ADC ANALOG CHARACTERISTICS - ALL MODES

Interchannel Isolation		-	90	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-3	-	3	%
Gain Drift		-100	-	+100	ppm/°C
Analog Input Characteristics					
Full-scale Input Voltage		0.54*V _A	0.56*V _A	0.58*V _A	V _{pp}
Input Impedance		-	300	-	kΩ

ADC DIGITAL FILTER CHARACTERISTICS (Note 11)

(Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified)

Parameter		Symbol	Min	Typ	Max	Unit
Single-Speed Mode						
Passband (-0.1 dB)	(Note 12)		0	-	0.47	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband	(Note 12)		0.58	-	-	Fs
Stopband Attenuation			-95	-	-	dB
Group Delay		t _{gd}	-	12/Fs	-	s
Interchannel Phase Deviation			-	-	0.0001	deg
Double-Speed Mode						
Passband (-0.1 dB)	(Note 12)		0	-	0.45	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband	(Note 12)		0.68	-	-	Fs
Stopband Attenuation			-92	-	-	dB
Group Delay		t _{gd}	-	9/Fs	-	s
Interchannel Phase Deviation			-	-	0.0001	deg
Quad-Speed Mode						
Passband (-0.1 dB)	(Note 12)		0	-	0.24	Fs
Passband Ripple			-0.1	-	0.035	dB
Stopband	(Note 12)		0.78	-	-	Fs
Stopband Attenuation			-97	-	-	dB
Group Delay		t _{gd}	-	5/Fs	-	s
Interchannel Phase Deviation			-	-	0.0001	deg
High-Pass Filter Characteristics						
Frequency Response	-3.0 dB	(Note 13)	-	1	-	Hz
	-0.13 dB			20	-	Hz
Phase Deviation @ 20 Hz		(Note 13)	-	10	-	deg

Parameter	Symbol	Min	Typ	Max	Unit
Passband Ripple		-	-	0	dB
Filter Settling Time			$10^5/F_s$		s

11. Plots of this data are contained in [Section 11. "Appendix" on page 42](#). See [Figures 43 through 54](#).
12. The filter frequency response scales precisely with F_s .
13. Response shown is for F_s equal to 48 kHz. Filter characteristics scale with F_s .

DC ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$; AGND=DGND=0, all voltages with respect to ground; MLCK=12.288 MHz; Master Mode)

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply					
Power Supply Current (Normal Operation)	VA = 5 V	I_A	-	31	mA
	VA = 3.3 V	I_A	-	27	mA
	VD, VLC = 5 V	I_D	-	29	mA
	VD, VLC = 3.3 V	I_D	-	20	mA
Power Supply Current (Power-Down Mode) (Note 14)	VA = 5 V	I_A	-	1.51	mA
	VD, VLC = 5 V	I_D	-	0.45	mA
Power Consumption	VA = 5 V, VD = VLC = 3.3 V	Normal Operation	-	221	mW
	VA = 5 V, VD = VLC = 3.3 V	Normal Operation	-	255	mW
	VA = 5 V, VD = VLC = 3.3 V	Power-Down Mode (Note 14)	-	9.8	mW
	VA = 5 V, VD = VLC = 3.3 V	Power-Down Mode (Note 14)	-	323	mW
Power Supply Rejection Ratio (1 kHz) (Note 15)	PSRR	-	60	-	dB
Common Mode Voltage					
Nominal Common Mode Voltage	VQ	-	VA/2	-	VDC
Maximum DC Current Source/Sink from VQ		-	1	-	μA
VQ Output Impedance		-	25	-	$\text{k}\Omega$
Positive Voltage Reference					
FILT+ Nominal Voltage	FILT+	-	VA	-	VDC
Maximum DC Current Source/Sink from FILT+		-	10	-	μA
FILT+ Output Impedance		-	18	-	$\text{k}\Omega$
Mute Control					
MUTEA, MUTE B Low-Level Output Voltage		-	0	-	V
MUTEA, MUTE B High-Level Output Voltage		-	VA	-	V
Maximum MUTEA & MUTE B Drive Current		-	3	-	mA

14. Power Down Mode is defined as $\overline{\text{RST}} = \text{Low}$ with all clocks and data lines held static.
15. Valid with the recommended capacitor values on FILT+ and VQ as shown in the Typical Connection Diagram.

DIGITAL CHARACTERISTICS

Parameter (Note 16)		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	Serial Port	V_{IH}	0.7xVD	-	-	V
	Control Port		0.7xVLC	-	-	V
Low-Level Input Voltage	Serial Port	V_{IL}	-	-	0.2xVD	V
	Control Port		-	-	0.2xVLC	V
High-Level Output Voltage at $I_o = 2$ mA	Serial Port	V_{OH}	VD - 1.0	-	-	V
	Control Port		VLC - 1.0	-	-	V
	MUTEA, MUTEB		VA - 1.0	-	-	V
Low-Level Output Voltage at $I_o = 2$ mA		V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	10	μ A

16. Serial Port signals include: SCLK, LRCK, SDOUT, SDIN

Control Port signals include: SDA/CDOUT, SCL/CCLK, AD1/CDIN, AD0/ $\overline{CS}$, $\overline{RST}$

SWITCHING CHARACTERISTICS - SERIAL AUDIO PORT

(Logic "0" = AGND = 0 V; Logic "1" = VD, $C_L = 20$ pF)

Parameter		Symbol	Min	Typ	Max	Unit
Sample Rate	Single-Speed Mode	F_s	4	-	54	kHz
	Double-Speed Mode	F_s	50	-	108	kHz
	Quad-Speed Mode	F_s	100	-	216	kHz
MCLK Specifications						
MCLK Frequency (Note 17)	Stand-Alone Mode	f_{mclk}	1.024	-	55.296	MHz
	Control Port Mode	f_{mclk}	1.024	-	55.296	MHz
MCLK Duty Cycle			40	50	60	ns
Master Mode						
LRCK Duty Cycle			-	50	-	%
SCLK Period			-	$\frac{1}{(64)F_s}$	-	s
SCLK Duty Cycle			-	50	-	%
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns
SCLK falling to SDOUT valid		t_{sdo}	-	-	32	ns
SDIN valid to SCLK rising setup time		t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time		t_{sdih}	20	-	-	ns
Slave Mode						
LRCK Duty Cycle			40	50	60	%
SCLK Period (Note 17)	Single-Speed Mode	t_{sclkw}	$\frac{1}{(128)F_s}$	-	-	s
	Double-Speed Mode	t_{sclkw}	$\frac{1}{(128)F_s}$	-	-	s
	Quad-Speed Mode	t_{sclkw}	$\frac{1}{(64)F_s}$	-	-	s
SCLK Duty Cycle			45	50	55	ns
SCLK falling to LRCK edge		t_{slr}	-10	-	10	ns

SCLK falling to SDOUT valid	t_{sdo}	-	-	32	ns
SDIN valid to SCLK rising setup time	t_{sdis}	16	-	-	ns
SCLK rising to SDIN hold time	t_{sdih}	20	-	-	ns

17. In Control Port Mode, MCLK Frequency and Functional Mode Select bits must be configured according to [Table 5](#), [Table 9](#), and [Table 8](#)

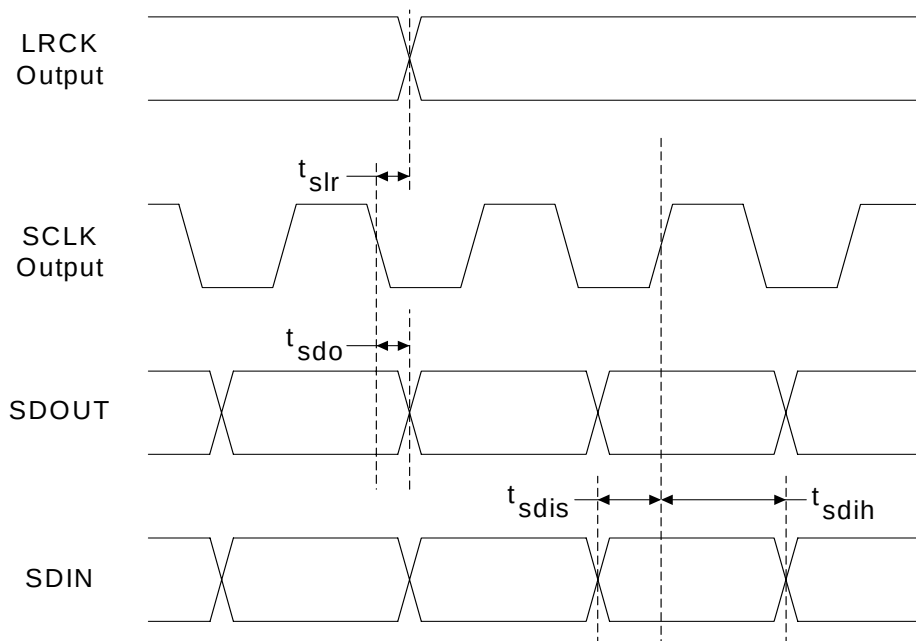


Figure 3. Master Mode Serial Audio Port Timing

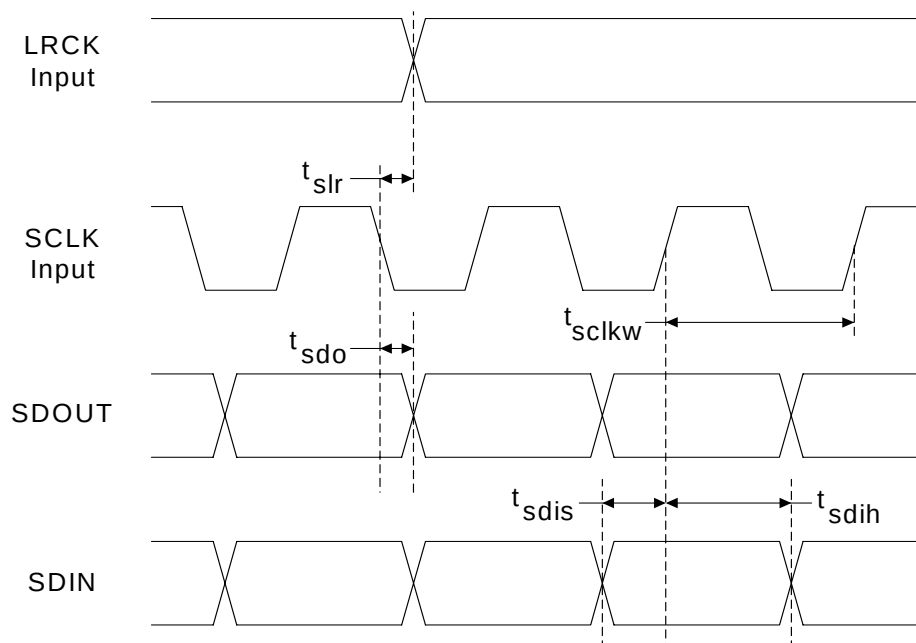


Figure 4. Slave Mode Serial Audio Port Timing

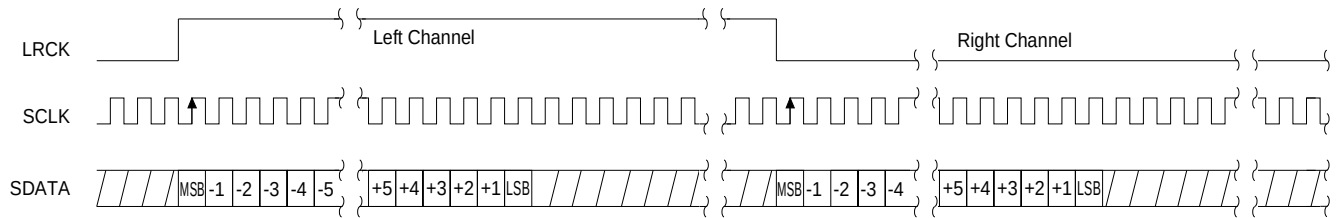


Figure 5. Format 0, Left Justified up to 24-Bit Data

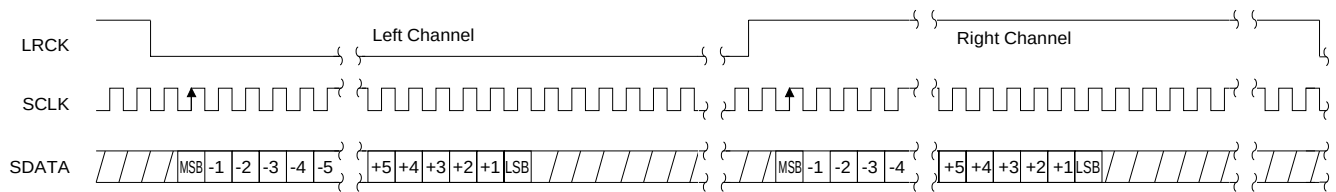
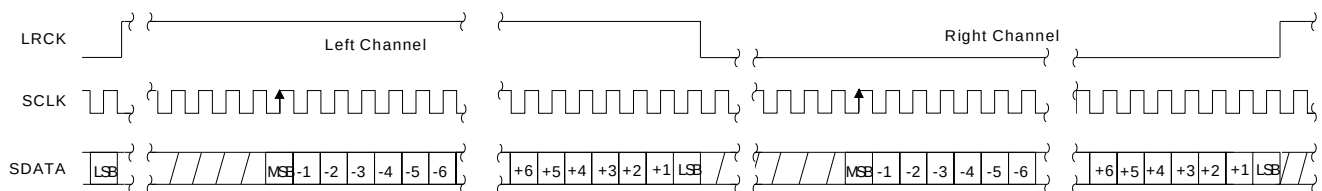


Figure 6. Format 1, I²S up to 24-Bit Data



**Figure 7. Format 2, Right Justified 16-Bit Data. (Available in Control Port Mode only)
Format 3, Right Justified 24-Bit Data. (Available in Control Port Mode only)**

SWITCHING CHARACTERISTICS - I²C MODE CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
RST Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	μ s
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	μ s
Clock Low time	t_{low}	4.7	-	μ s
Clock High Time	t_{high}	4.0	-	μ s
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	μ s
SDA Hold Time from SCL Falling (Note 18)	t_{hdd}	0	-	μ s
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	μ s
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	μ s

18. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

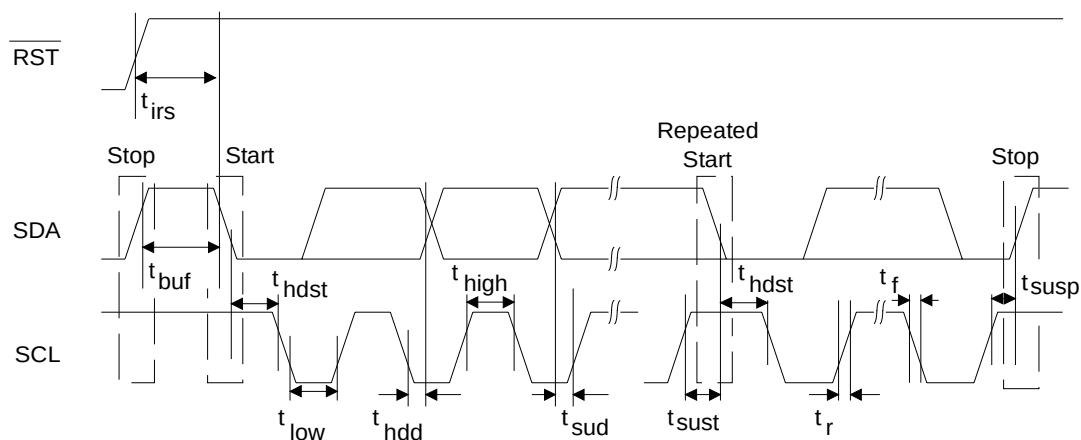


Figure 8. I²C Mode Control Port Timing

SWITCHING CHARACTERISTICS - SPI CONTROL PORT

(Inputs: logic 0 = DGND, logic 1 = VLC)

Parameter	Symbol	Min	Max	Unit
SPI Mode				
CCLK Clock Frequency	f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling	t_{srs}	500	-	ns
CCLK Edge to $\overline{\text{CS}}$ Falling (Note 19)	t_{spi}	500	-	ns
CS High Time Between Transmissions	t_{csh}	1.0	-	μs
CS Falling to CCLK Edge	t_{css}	20	-	ns
CCLK Low Time	t_{scl}	82	-	ns
CCLK High Time	t_{sch}	82	-	ns
CDIN to CCLK Rising Setup Time	t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time (Note 20)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN (Note 21)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN (Note 21)	t_{f2}	-	100	ns

19. t_{spi} only needed before first falling edge of $\overline{\text{CS}}$ after $\overline{\text{RST}}$ rising edge. $t_{\text{spi}} = 0$ at all other times.

20. Data must be held for sufficient time to bridge the transition time of CCLK.

21. For $F_{\text{SCK}} < 1 \text{ MHz}$

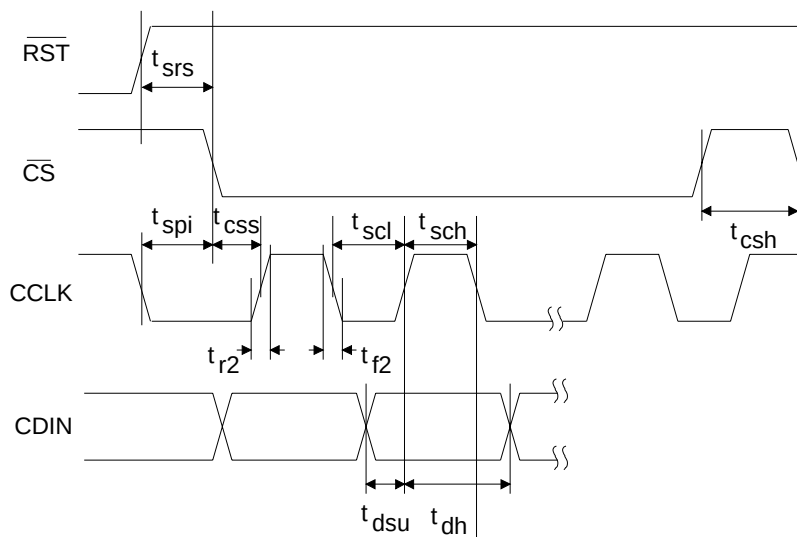


Figure 9. SPI Control Port Timing

4. TYPICAL CONNECTION DIAGRAM

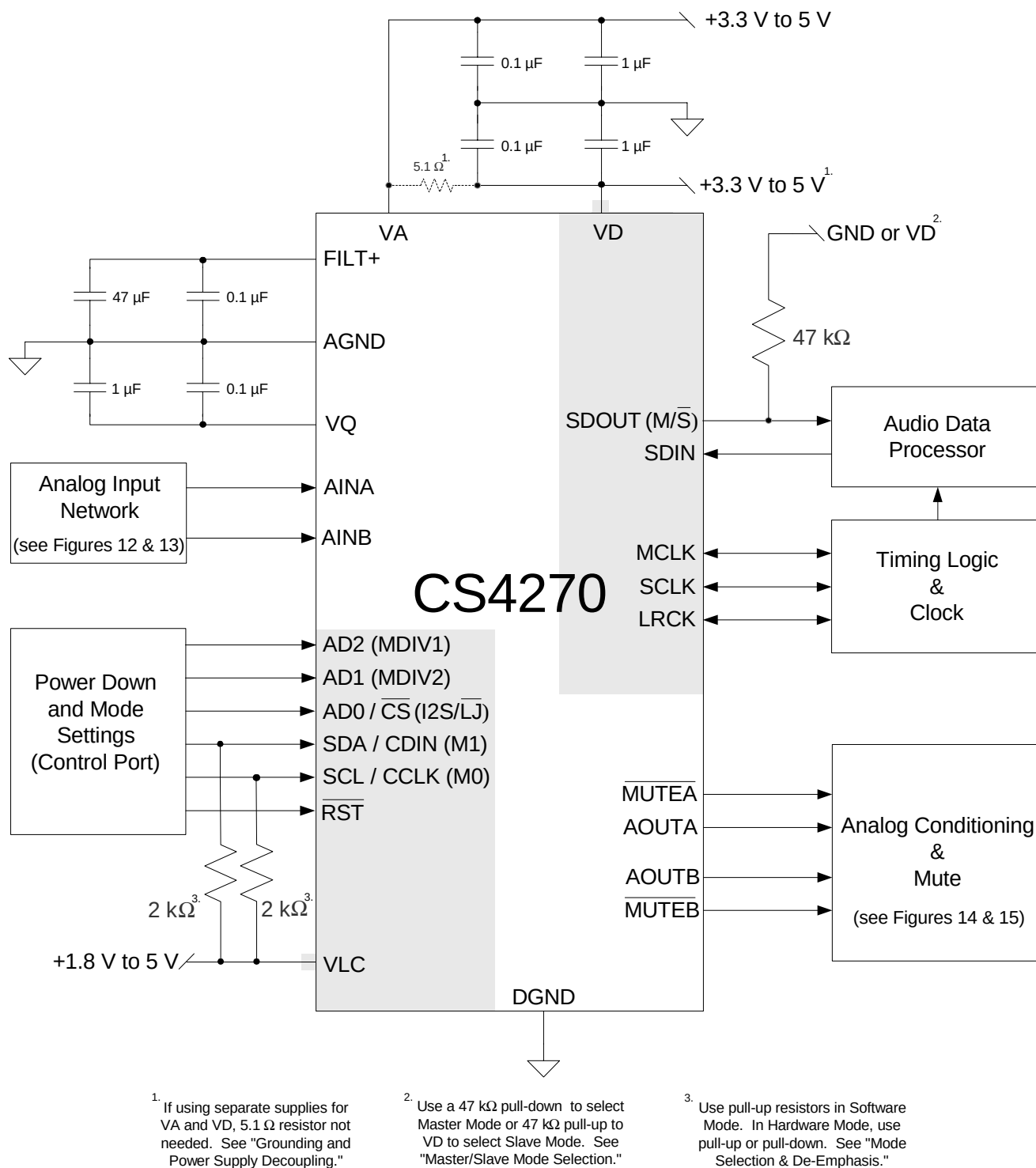


Figure 10. CS4270 Typical Connection Diagram

5. APPLICATIONS

5.1 Stand-Alone Mode

5.1.1 Recommended Power-Up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supplies, clocks and configuration pins are stable. It is also recommended that reset be enabled if the analog or digital supplies drop below the minimum specified operating voltages to prevent power glitch related issues.

5.1.2 Master/Slave Mode

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to F_s and SCLK is equal to $64 \times F_s$.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be $48 \times$ or $64 \times F_s$ to maximize system performance.

In Stand-Alone Mode, the CS4270 will enter Slave Mode when SDOUT ($M/\bar{S}$) is pulled low through a $47\text{ k}\Omega$ resistor. Master Mode may be accessed by placing a $47\text{ k}\Omega$ pull-up to VD on the SDOUT ($M/\bar{S}$) pin.

Configuration of clock ratios in each of these modes is outlined in [Table 2](#).

5.1.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in [Table 1](#).

Mode	Sampling Frequency
<i>Single-Speed</i>	4-54 kHz
<i>Double-Speed</i>	50-108 kHz
<i>Quad-Speed</i>	100-216 kHz

Table 1. Speed Modes

5.1.4 Clock Ratio Selection

Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios are shown in the [Table 2](#).

Master Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	64	Fs	0	0
	384	64	Fs	0	1
	512	64	Fs	1	0
	1024	64	Fs	1	1
Double-Speed	128	64	Fs	0	0
	192	64	Fs	0	1
	256	64	Fs	1	0
	512	64	Fs	1	1
Quad-Speed	64	64	Fs	0	0
	96	64	Fs	0	1
	128	64	Fs	1	0
	256	64	Fs	1	1
Slave Mode					
	MCLK/LRCK	SCLK/LRCK	LRCK	MDIV2	MDIV1
Single-Speed	256	32, 48, 64, 128	Fs	0	0
	384	32, 48, 64, 96	Fs	0	1
	512	32, 48, 64, 128	Fs	1	0
	1024	32, 48, 64, 96	Fs	1	1
Double-Speed	128	32, 48, 64	Fs	0	0
	192	32, 48, 64	Fs	0	1
	256	32, 48, 64	Fs	1	0
	512	32, 48, 64	Fs	1	1
Quad-Speed	64	32, 48, 64	Fs	0	0
	96	32, 48, 64	Fs	0	1
	128	32, 48, 64	Fs	1	0
	256	32, 48, 64	Fs	1	1

Table 2. Clock Ratios - Stand-Alone Mode

5.1.5 Interpolation Filter

In Stand-Alone Mode, the fast roll-off interpolation filter is used. Filter specifications can be found in [Section 3](#). Plots of the data are contained in [Section 11. "Appendix" on page 42](#).

5.1.6 High-Pass Filter

The operational amplifiers in the input circuitry driving the CS4270 may generate a small DC offset into the ADC. The CS4270 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. In Stand-Alone Mode, the high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. This function cannot be disabled in Stand-Alone Mode.

5.1.7 Mode Selection & De-Emphasis

The sample rate, F_s , can be adjusted from 4 kHz to 216 kHz and De-emphasis, optimized for 44.1 kHz, is available in Single-Speed Mode. In Stand-Alone Master Mode, the CS4270 must be set to the proper mode via the mode pins, M1 and M0. In Slave Mode, the CS4270 auto-detects Speed Mode and the M0 pin becomes De-emphasis select. Stand-alone definitions of the mode pins are shown in [Table 3](#).

Mode 1	Mode 0	Mode	Sample Rate (F_s)	De-Emphasis
0	0	Single-Speed Mode	4 kHz - 54 kHz	Off
0	1	Single-Speed Mode	4 kHz - 54 kHz	44.1 kHz
1	0	Double-Speed Mode	50 kHz - 108 kHz	Off
1	1	Quad-Speed Mode	100 kHz - 216 kHz	Off

Table 3. CS4270 Stand-Alone Mode Control

5.1.8 Serial Audio Interface Format Selection

Either I²S or Left-Justified serial audio data format may be selected in Stand-Alone Mode. The selection will affect both the input and output format. Placing a 10 k Ω pull-up to VD on the I²S/LJ pin will select the I²S format, while placing a 10 k Ω pull-down to DGND on the I²S/LJ pin will select the left justified format.

5.2 Control Port Mode

5.2.1 Recommended Power-Up Sequence - Access to Control Port Mode

1. Pull $\overline{\text{RST}}$ low until the power supply, MCLK, and LRCK are stable.
2. Release $\overline{\text{RST}}$. The control port will be accessible.
3. Initiate a SPI or I²C transaction as described in [Section 6.1](#) or [Section 6.2](#), respectively.

5.2.2 Master / Slave Mode Selection

The CS4270 supports operation in either Master Mode or Slave Mode.

In Master Mode, LRCK and SCLK are outputs and are synchronously generated on-chip. LRCK is equal to F_s and SCLK is equal to $64 \times F_s$.

In Slave Mode, LRCK and SCLK are inputs, requiring external generation that is synchronous to MCLK. It is recommended that SCLK be $48 \times$ or $64 \times F_s$ to maximize system performance.

Configuration of clock ratios in each of these modes will be outlined in the [Table 10](#) and [Table 9](#).

In Control Port Mode the CS4270 will default to Slave Mode. The user may change this default setting by changing the status of the M/ $\overline{\text{S}}$ bits in the Functional Control Register (03h).

5.2.3 System Clocking

The CS4270 will operate at sampling frequencies from 4 kHz to 216 kHz. This range is divided into three speed modes as shown in [Table 4](#).

Mode	Sampling Frequency
Single-Speed	4-54 kHz
Double-Speed	50-108 kHz
Quad-Speed	100-216 kHz

Table 4. Speed Modes

5.2.4 Clock Ratio Selection

In Control Port Master Mode, the user must configure the mode bits (M0, M1, M2) to set the speed mode and select the appropriate clock ratios. Depending on whether the CS4270 is in Master or Slave Mode, different MCLK/LRCK and SCLK/LRCK ratios may be used. These ratios as well as the Control Port Register Bits are shown in [Table 5](#), [Table 9](#) and [Section 8.3 on page 35](#).

Master Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	64	Fs	0	0	0
	384	64	Fs	0	0	1
	512	64	Fs	0	1	0
	768	64	Fs	0	1	1
	1024	64	Fs	1	0	0
Double-Speed	128	64	Fs	0	0	0
	192	64	Fs	0	0	1
	256	64	Fs	0	1	0
	384	64	Fs	0	1	1
	512	64	Fs	1	0	0
Quad-Speed	64	64	Fs	0	0	0
	96	64	Fs	0	0	1
	128	64	Fs	0	1	0
	192	64	Fs	0	1	1
	256	64	Fs	1	0	0
Slave Mode						
	MCLK/LRCK	SCLK/LRCK	LRCK	MCLK Freq<2>	MCLK Freq<1>	MCLK Freq<0>
Single-Speed	256	32, 64, 128	Fs	0	0	0
	384	32, 48, 64, 96, 128	Fs	0	0	1
	512	32, 64, 128	Fs	0	1	0
	768	32, 48, 64, 96, 128	Fs	0	1	1
	1024	32, 64, 128	Fs	1	0	0

Table 5. Clock Ratios - Control Port Mode

Master Mode						
Double-Speed	128	32, 48, 64	Fs	0	0	0
	192	32, 48, 64	Fs	0	0	1
	256	32, 48, 64	Fs	0	1	0
	384	32, 48, 64	Fs	0	1	1
	512	32, 64	Fs	1	0	0
Quad-Speed	64	32	Fs	0	0	0
	96	48, 64	Fs	0	0	1
	128	32, 64	Fs	0	1	0
	192	48, 64	Fs	0	1	1
	256	32, 64	Fs	1	0	0

Table 5. Clock Ratios - Control Port Mode (Continued)

5.2.5 Internal Digital Loopback

In Control Port Mode, the CS4270 supports an internal digital loopback mode in which the output of the ADC is routed to the input of the DAC. This mode may be activated by setting the Digital Loopback bit in the ADC & DAC Ctrl register (04h).

When this bit is set, the status of the DAC_DIF(4:3) bits in register 04h will be disregarded by the CS4270. Any changes made to the DAC_DIF(4:3) bits while the Digital Loopback bit is set will have no impact on operation until the Digital Loopback bit is released, at which time the Digital Interface Format of the DAC will operate according to the format selected in the DAC_DIF(4:3) bits. While the Digital Loopback bit is set, data will be present on the SDOUT pin in the format selected in the ADC_DIF(0) bit in register 04h.

5.2.6 Auto-Mute

The Auto-Mute function is controlled by the status of the Auto Mute bit in the Mute register. When set, the DAC output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting are done independently for each channel. The common mode on the output will be retained and the Mute Control pin for that channel will become active during the mute period. The muting function is affected, similar to volume control changes, by the Soft and ZeroCross bits in the Transition and Control register. The Auto Mute bit is set by default.

5.2.7 High-Pass Filter and DC Offset Calibration

The input circuitry driving the CS4270 may generate a small DC offset into the A/D converter. The CS4270 includes a high-pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

The high-pass filter continuously subtracts a measure of the DC offset from the output of the decimation filter. The high-pass filter can be enabled if the hpf_freeze bit is set during normal operation, the current value of the DC offset for the corresponding channel is frozen and this DC offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system DC offset calibration by:

1. Running the CS4270 with the high-pass filter enabled until the filter settles. See the Digital Filter Characteristics for filter settling time.
2. Disabling the high-pass filter and freezing the stored DC offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS4270.

5.2.8 De-Emphasis

One de-emphasis mode is available via the Control Port and is optimized for 44.1 kHz sampling rate.

5.2.9 Oversampling Modes

The CS4270 operates in one of three oversampling modes based on the input sample rate. Mode selection is determined by the FM_&_M/S_Mode[1:0] bits in the Functional Mode register (03h). Single-Speed mode supports input sample rates up to 54 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 108 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 216 kHz and uses an oversampling ratio of 32x. See [Table 10](#) for Control Port Mode settings.

5.3 De-Emphasis Filter

The CS4270 includes on-chip digital de-emphasis. [Figure 11](#) shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, F_s . Please see [Section 5.1.7](#) for the desired de-emphasis control for Stand-Alone mode and [Section 5.2.8](#) for control port mode.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μ s pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-Speed Mode.

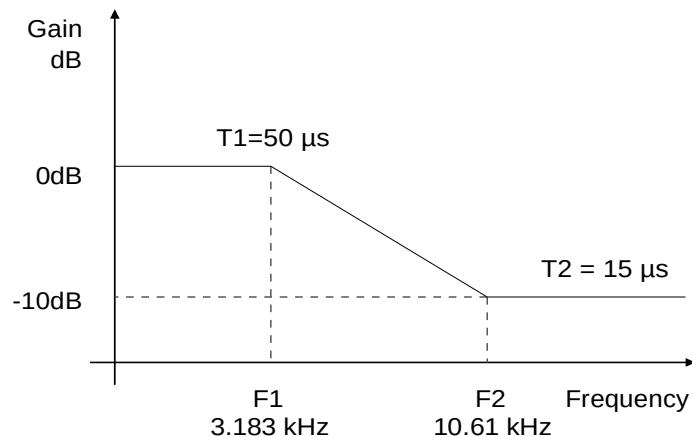


Figure 11. De-Emphasis Curve

5.4 Analog Connections

5.4.1 Input Connections

The analog modulator samples the input at 6.144 MHz. The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the input sampling frequency ($n \times 6.144 \text{ MHz}$), where $n=0,1,2,\dots$. Refer to [Figure 12](#) which shows the recommended topology of the analog input network. The capacitor values chosen not only provide the appropriate filtering of noise at the modulator sampling frequency, but also act as a charge source for the internal sampling circuits. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) must be avoided since these can degrade signal linearity.

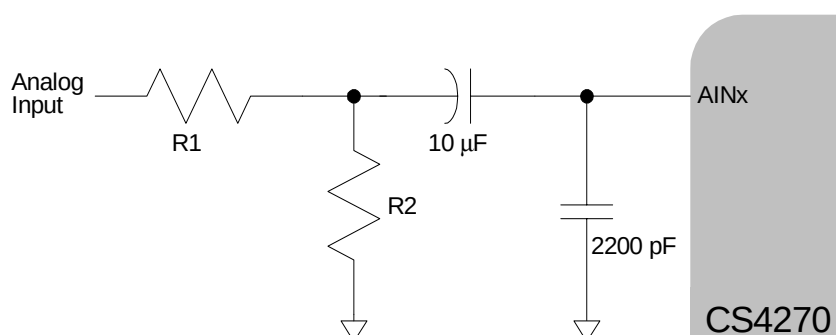


Figure 12. CS4270 Recommended Analog Input Network

Three parameters determine the values of resistors R1 and R2 as shown in [Figure 12](#): source impedance, attenuation, and input impedance. Source impedance is defined as the impedance as seen from the ADC looking back into the signal network. Analog performance is optimized for small source impedance and a source impedance above 2.5 kΩ results in degraded THD+N.

The required attenuation factor depends on the magnitude of the input signal. The full-scale input voltage scales with V_A ; for $V_A = 5 \text{ V}$, the CS5344 full-scale input magnitude is 1 Vrms. R1 and R2 should be set such that an input signal greater than the full-scale input should be attenuated to the appropriate magnitude. Typical line-level voltage in audio applications is 2 Vrms, in which case R1 and R2 must combine to form an attenuation factor of 2, thus giving the CS5344 a 1 Vrms input.

Input impedance is the impedance from the signal source to the ADC analog input pins. The target input impedance depends on the overall system specifications, but typical audio systems require an input impedance of 10 kΩ. [Table 6](#) shows the input parameters and the associated design equations. [Figure 13](#) illustrates an example configuration for a source impedance of 46 Ω, an attenuation factor of 1, and input impedance of 9.8 kΩ.

Source Impedance	$\frac{(R1 \times R2)}{R1 + R2}$
Attenuation Factor	$\frac{R2}{R1 + R2}$
Input Impedance	$(R1 + R2)$

Table 6. Analog Input Design Parameters

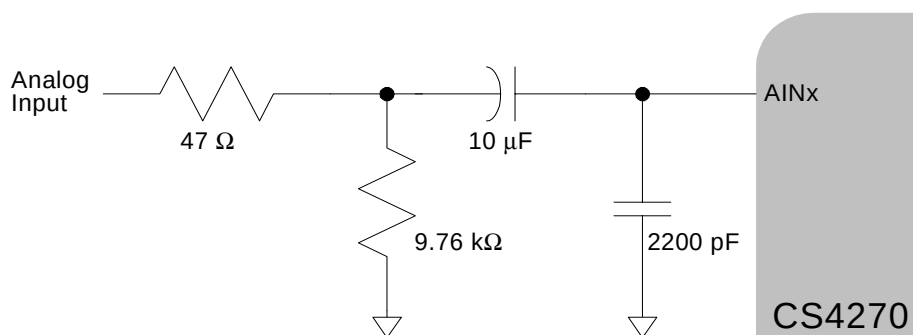
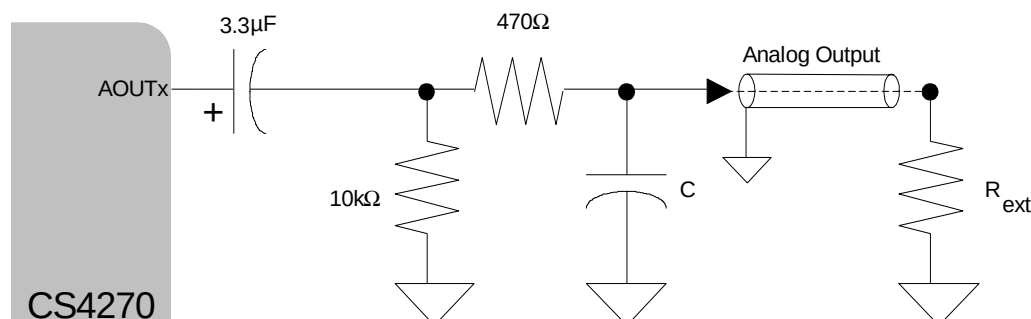


Figure 13. CS5344 Example Analog Input Network

5.4.2 Output Connections

The analog output filter present in the CS4270 is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 19 - 42. The recommended external analog circuitry is shown in Figure 14.



$$C = \frac{R_{\text{ext}} + 470}{4\pi F_S (R_{\text{ext}} \bullet 470)} \text{ For best 20 kHz response}$$

Figure 14. CS4270 Recommended Analog Output Filter

5.5 Mute Control

The Mute Control pins become active during power-up initialization, reset, muting, when the MCLK to LRCK ratio is incorrect, and during power-down. The MUTE pins are intended to be used as control for an external mute circuit in order to add off-chip mute capability.

The CS4270 also features Auto-Mute, which is enabled by default. The Auto-Mute function causes the MUTE pin corresponding to an individual channel to activate following the reception of 8192 consecutive static-level audio samples on the respective channel. A single transition of data on the channel will cause the corresponding MUTE pin to deactivate.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system

designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. The MUTE pins are active-low. See Figure 15 for a suggested active-low mute circuit.

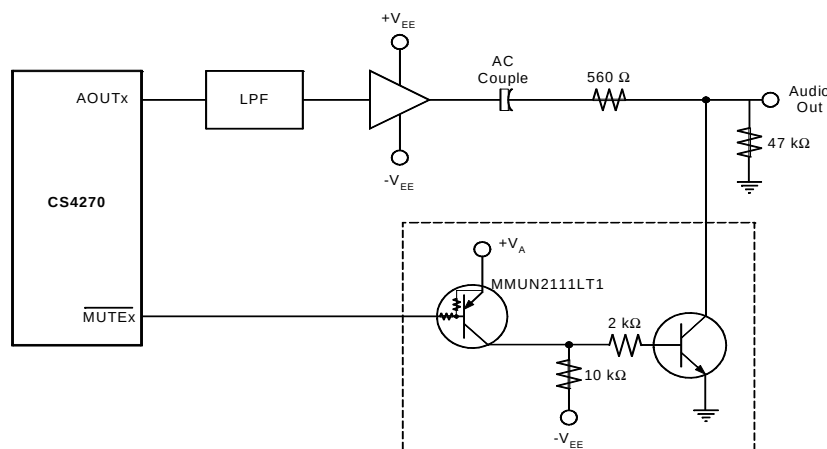


Figure 15. Suggested Active-Low Mute Circuit

5.6 Synchronization of Multiple Devices

In systems where multiple ADCs are required, care must be taken to achieve simultaneous sampling. To ensure synchronous sampling, the MCLK and LRCK must be the same for all of the CS4270's in the system. If only one MCLK source is needed, one solution is to place one CS4270 in Master Mode, and slave all of the other CS4270's to the one master. If multiple MCLK sources are needed, a possible solution would be to supply all clocks from the same external source and time the CS4270 reset with the inactive edge of MCLK. This will ensure that all converters begin sampling on the same clock edge.

5.7 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4270 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 10 shows the recommended power arrangements, with VA and VD connected to clean supplies. VD, which powers the digital filter, may be run from the system digital supply (VD) or may be powered from the analog supply (VA) via a resistor. In this case, no additional devices should be powered from VD. Power supply decoupling capacitors should be as near to the CS4270 as possible, with the low value ceramic capacitor being the nearest. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the modulators. The VREF and VCOM decoupling capacitors, particularly the 0.1 μF, must be positioned to minimize the electrical path from VREF and AGND. The CDB4270 evaluation board demonstrates the optimum layout and power supply arrangements. To minimize digital noise, connect the CS4270 digital outputs only to CMOS inputs.

6. CONTROL PORT INTERFACE

The Control Port is used to load all the internal settings of the CS4270. The operation of the Control Port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

The Control Port has 2 modes: SPI and I²C, with the CS4270 operating as a slave to control messages in both modes. If I²C operation is desired, AD0/ $\overline{\text{CS}}$ should be tied to VLC or DGND. If the CS4270 ever detects a high to low transition on AD0/ $\overline{\text{CS}}$ after power-up, SPI mode will be selected.

Upon release of the $\overline{\text{RST}}$ pin, the CS4270 will wait approximately 10 ms before it begins its start-up sequence. The part defaults to Stand-Alone Mode, in which all operational modes are controlled as described in [Section 5.1 on page 22](#). If the user initiates communication to the part through the SPI or I²C interface, the part enters Control-Port Mode and all operational modes are controlled by the Control Port registers. If system requirements do not allow writing to the control port immediately following the release of $\overline{\text{RST}}$, the SDIN line should be held at logic "0" until the proper serial mode can be selected.

6.1 SPI™ Mode

In SPI mode, $\overline{\text{CS}}$ is the CS4270 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 1001111. All control signals are inputs and data is clocked in on the rising edge of CCLK.

[Figure 16](#) shows the operation of the Control Port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first 7 bits on CDIN form the chip address, and must be 1001111. The eighth bit is a read/write indicator (R/W), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP. See [Table 9 on page 35](#).

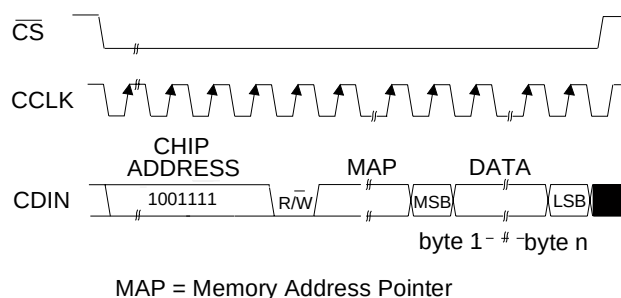


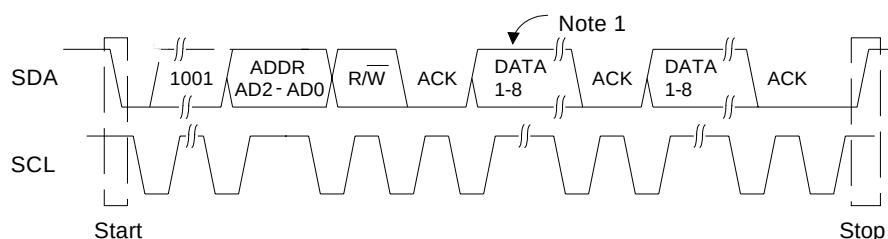
Figure 16. Control Port Timing, SPI mode

The CS4270 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block writes to successive registers.

6.2 I²C Mode

In I²C mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 17. There is no $\overline{CS}$ pin. Pins AD0, AD1, and AD2 form the partial chip address and should be tied to VLC or DGND as required. The upper 4 bits of the 7-bit address field must be 1001. To communicate with the CS4270, the three lower bits of the chip address field should match the setting on the AD0, AD1, and AD2 pins. The eighth bit of the address byte is the R/W bit (high for a read, low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. If the operation is a write, the MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS4270 has MAP auto increment capability, enabled by the INCR bit in the MAP. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 17. Control Port Timing, I²C Mode

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR - Auto MAP Increment Enable
 Default = '0'.
 0 - Disabled
 1 - Enabled

MAP(3:0) - Memory Address Pointer
 Default = '0000'.

Table 7. Memory Address Pointer

7. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	ID	id<3>	id<2>	id<1>	id<0>	rev<3>	rev<2>	rev<1>	rev<0>
		1	1	0	0	0	0	0	1
02h	Power Control	Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN
		0	0	0	0	0	0	0	0
03h	Funct Mode	Reserved	Reserved	FM_&_M/S_Mode1	FM_&_M/S_Mode0	MCLK freq<2>	MCLK freq<1>	MCLK freq<0>	PopGuard Disable
		0	0	1	1	0	0	0	0
04h	Serial Format	ADC HPF Freeze A	ADC HPF Freeze B	Digital Loopback	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0
		0	0	0	0	0	0	0	0
05h	Transition Control	DAC Single Vol	soft_dac	zc_dac	Invert ADC ch B	Invert ADC ch A	Invert DAC ch B	Invert DAC ch A	De-Emph
		0	1	1	0	0	0	0	0
06h	Mute	Reserved	Reserved	Auto Mute	Mute ADC SP ch B	Mute ADC SP ch A	Mute Polarity	Mute DAC ch B	Mute DAC ch A
		0	0	1	0	0	0	0	0
07h	Vol Ctrl AOUTA	dacA vol<7>	dacA vol<6>	dacA vol<5>	dacA vol<4>	dacA vol<3>	dacA vol<2>	dacA vol<1>	dacA vol<0>
		0	0	0	0	0	0	0	0
08h	Vol Ctrl AOUTB	dacB vol<7>	dacB vol<6>	dacB vol<5>	dacB vol<4>	dacB vol<3>	dacB vol<2>	dacB vol<1>	dacB vol<0>
		0	0	0	0	0	0	0	0

8. REGISTER DESCRIPTION

** All registers are read/write in I²C mode and SPI mode, unless otherwise noted**

8.1 Chip ID - Address 01h

7	6	5	4	3	2	1	0
id<3>	id<2>	id<1>	id<0>	rev<3>	rev<2>	rev<1>	rev<0>

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1100b (01h) and the remaining bits (b3:b0) are for the chip revision.

8.2 Power Control - Address 02h

7	6	5	4	3	2	1	0
Freeze	Reserved	PDN_ADC	Reserved	Reserved	Reserved	PDN_DAC	PDN

8.2.1 Freeze (Bit 7)

Function:

This function allows modifications to be made to certain control port bits without the changes taking effect until the Freeze bit is disabled. To make multiple changes to these bits take effect simultaneously, set the Freeze bit, make all changes, then clear the Freeze bit. The bits affected by the Freeze function are listed below:

- Register 05h (Bits 7:0)
- Register 06h (Bits 7:0)
- Register 07h (Bits 7:0)
- Register 08h (Bits 7:0)

8.2.2 PDN_ADC (Bit 5)

Function:

The ADC portion of the device will enter a low-power state whenever this bit is set.

8.2.3 PDN_DAC (Bit 1)

Function:

The DAC portion of the device will enter a low-power state whenever this bit is set.

8.2.4 Power Down (Bit 0)

Function:

The device will enter a low-power state whenever this bit is set. The contents of the control registers are retained when the device is in power-down.

8.3 Mode Control - Address 03h

7	6	5	4	3	2	1	0
Reserved	Reserved	FM_&_M/S_ Mode1	FM_&_M/S_ Mode0	MCLK freq<2>	MCLK freq<1>	MCLK freq<0>	PopGuard Disable

8.3.1 ADC Functional Mode & Master / Slave Mode (Bits 5:4)

Function:

In Control Port Master Mode, the user must configure the CS4270 Speed Mode with these bits. In Control Port Slave Mode, the CS4270 auto-detects speed mode.

FM_&_M/S_ Mode1	FM_&_M/S_ Mode0	Mode
0	0	Single-Speed Mode: 4 to 54 kHz sample rates
0	1	Double-Speed Mode: 50 to 108 kHz sample rates
1	0	Quad-Speed Mode: 100 to 216 kHz sample rates
1	1	Slave Mode (default)

Table 8. Functional Mode Selection

8.3.2 Ratio Select (Bits 3:1)

Function:

These bits are used to select the clocking ratios.

MCLK freq<2>	MCLK freq<1>	MCLK freq<0>	Mode
0	0	0	Divide by 1 (default)
0	0	1	Divide by 1.5
0	1	0	Divide by 2
0	1	1	Divide by 3
1	0	0	Divide by 4

Table 9. MCLK Divider Configuration

8.3.3 PopGuard Disable (Bit 0)

Function:

Disables PopGuard when set. PopGuard is enabled by default.

8.4 ADC and DAC Control - Address 04h

7	6	5	4	3	2	1	0
ADC HPF Freeze A	ADC HPF Freeze B	Digital Loopback	DAC_DIF1	DAC_DIF0	Reserved	Reserved	ADC_DIF0

8.4.1 ADC HPF Freeze A (Bit 7)

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled. The current DC offset value will be frozen and continuously subtracted from the conversion result. [Section 5.2.7 "High-Pass Filter and DC Offset Calibration" on page 26.](#)

8.4.2 ADC HPF Freeze B (Bit 6)

Function:

When this bit is set, the internal high-pass filter for the selected channel will be disabled. The current DC offset value will be frozen and continuously subtracted from the conversion result. [Section 5.2.7 “High-Pass Filter and DC Offset Calibration” on page 26.](#)

8.4.3 Digital Loopback (Bit 5)

Function:

When this bit is set, an internal digital loopback from the ADC to the DAC will be enabled. Please refer to [Section 5.2.5 “Internal Digital Loopback” on page 26.](#)

8.4.4 DAC Digital Interface Format (Bits 4:3)

Function:

The DAC Digital Interface Format and the options are detailed in [Table 10](#) and Figures 5 through 7.

DAC_DIF1	DAC_DIF0	Description	Format	Figure
0	0	Left Justified, up to 24-bit data (default)	0	5
0	1	I ² S, up to 24-bit data	1	6
1	0	Right Justified, 16-bit Data	2	7
1	1	Right Justified, 24-bit Data	3	7

Table 10. DAC Digital Interface Formats

8.4.5 ADC Digital Interface Format (Bit 0)

Function:

The required relationship between LRCK, SCLK and SDOUT for the ADC is defined by the ADC Digital Interface Format. The options are detailed in [Table 11](#) and may be seen in [Figures 5 and 6.](#)

ADC_DIF	Description	Format	Figure
0	Left Justified, up to 24-bit data (default)	0	5
1	I ² S, up to 24-bit data	1	6

Table 11. ADC Digital Interface Formats

8.5 Transition Control - Address 05h

7	6	5	4	3	2	1	0
DAC Single Volume	soft_dac	zc_dac	invert ADC ch B	invert ADC ch A	invert DAC ch B	invert DAC ch A	De-emph

8.5.1 DAC Single Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte (07h) and the B Channel Byte (08h) is ignored when this function is enabled. Volume and muting functions are affected by the Soft Ramp and ZeroCross functions below.

8.5.2 Soft Ramp or Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods. See [Table 12 on page 37](#).

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See [Table 9 on page 35](#).

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictate that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See [Table 9 on page 35](#).

Soft	ZeroCross	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled
1	1	Soft Ramp and Zero Cross enabled (default)

Table 12. Soft Cross or Zero Cross Mode Selection

8.5.3 Invert Signal Polarity (Bits 4:1)

Function:

When set, this bit activates an inversion of the signal polarity for the appropriate channel. This is useful if a board layout error has occurred or in other situations where a 180 degree phase shift is desirable.

8.5.4 De-Emphasis Control (Bit 0)

Function:

Implementation of the standard 50/15 μ s digital de-emphasis filter on the DAC output requires reconfiguration of the digital filter to maintain the proper filter response for 44.1 kHz sample rate. [Figure 18](#) shows the filter response. **NOTE:** De-emphasis is available only in Single-Speed Mode.

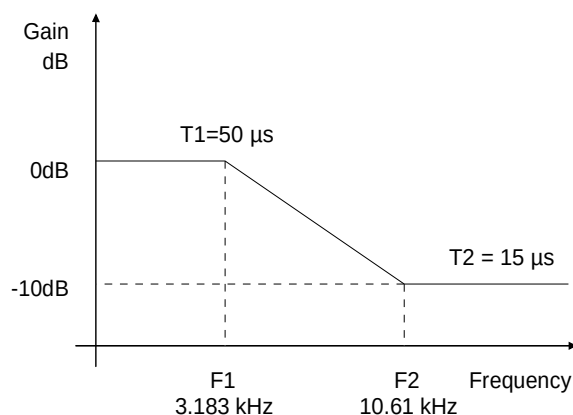


Figure 18. De-Emphasis Curve

8.6 Mute Control - Address 06h

7	6	5	4	3	2	1	0
		Auto Mute	Mute ADC SP ch B	Mute ADC SP ch A	mute polarity	Mute DAC SP ch B	Mute DAC SP ch B

8.6.1 Auto-Mute (Bit 5)

Function:

When set, enables the Auto-Mute function. [Section 5.2.6 “Auto-Mute” on page 26.](#)

8.6.2 ADC Channel A & B Mute (Bits 4:3)

Function:

When this bit is set, the output of the ADC for the selected channel will be muted.

8.6.3 Mute Polarity (Bit 2)

Function:

The MUTEA and MUTEB pins (pins 24 and 21) are active low by default. When this bit is set, these pins are active high.

8.6.4 DAC Channel A & B Mute (Bits 1:0)

Function:

When this bit is set, the output of the DAC for the selected channel will be muted.

8.7 DAC Channel A Volume Control - Address 07h

7	6	5	4	3	2	1	0
dacA vol<7>	dacA vol<6>	dacA vol<5>	dacA vol<4>	dacA vol<3>	dacA vol<2>	dacA vol<1>	dacA vol<0>

Function:

See [Section 8.8 DAC Channel B Volume Control - Address 08h](#).

8.8 DAC Channel B Volume Control - Address 08h

7	6	5	4	3	2	1	0
dacB vol<7>	dacB vol<6>	dacB vol<5>	dacB vol<4>	dacB vol<3>	dacB vol<2>	dacB vol<1>	dacB vol<0>

Function:

The digital volume control allows the user to attenuate the signal in 0.5 dB increments from 0 to -127 dB. The vol<0> bit activates a 0.5 dB attenuation when set, and no attenuation when cleared. The Vol[7:1] bits activate attenuation equal to their decimal value (in dB). Example volume settings are decoded as shown in [Table 13](#). The volume changes are implemented as dictated by the DACSoft and DACZero-Cross bits in the Transition Control register (see [Section 8.5.2](#)).

Binary Code	Volume Setting
00000000	0 dB
00000001	-0.5 dB
00101000	-20 dB
00101001	-20.5 dB
11111110	-127 dB
11111111	-127.5 dB

Table 13. Digital Volume Control

9. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

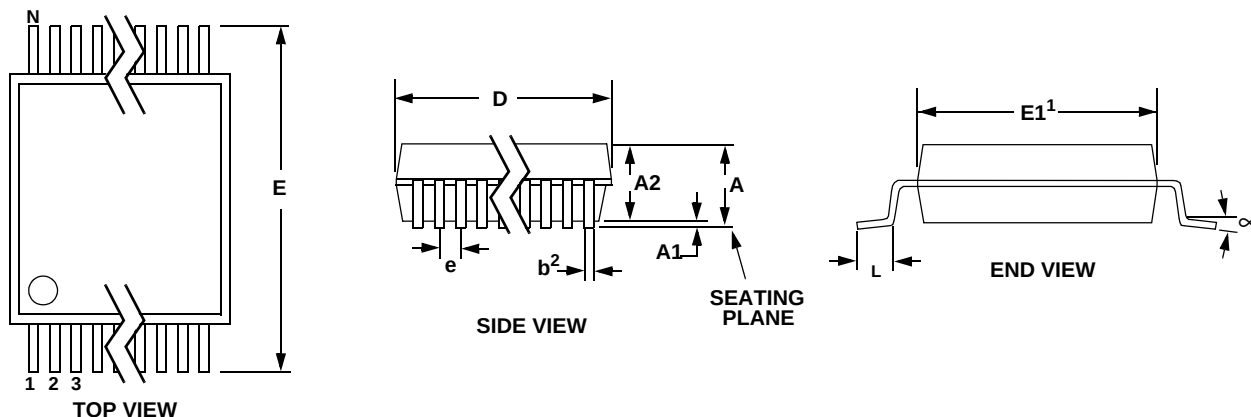
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

10. PACKAGE DIMENSIONS

24L TSSOP (4.4 mm BODY) PACKAGE DRAWING



DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.47	--	--	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.029	0.50	0.60	0.75	
μ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

11.APPENDIX

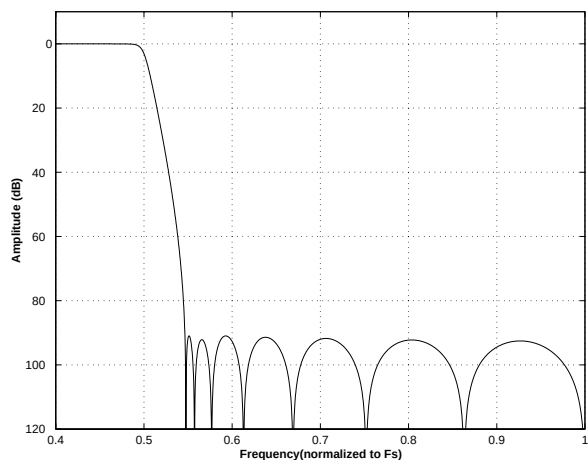


Figure 19. DAC Single-Speed (fast) Stopband Rejection

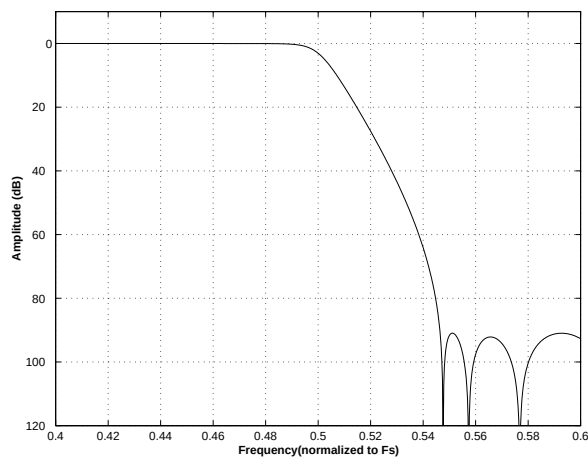


Figure 20. DAC Single-Speed (fast) Transition Band

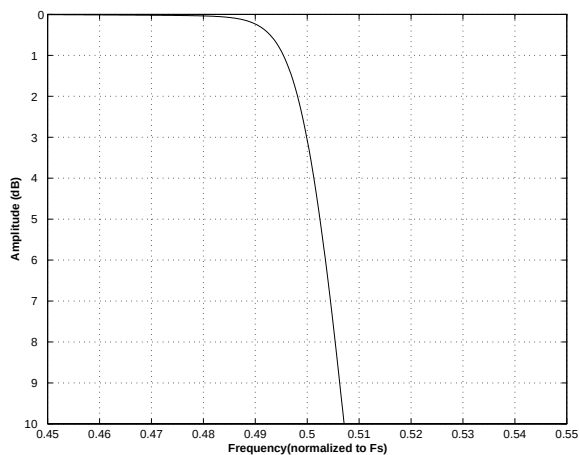


Figure 21. DAC Single-Speed (fast) Transition Band (detail)

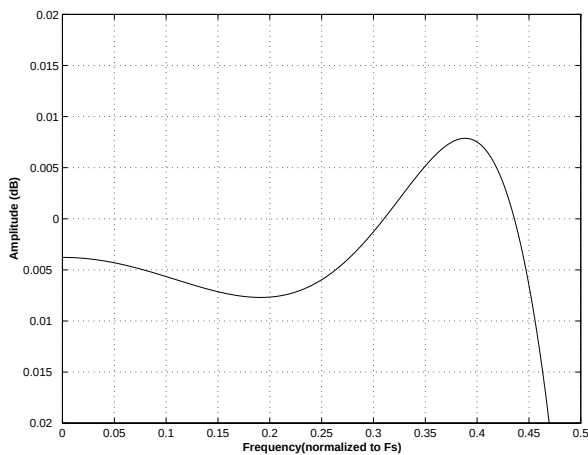


Figure 22. DAC Single-Speed (fast) Passband Ripple

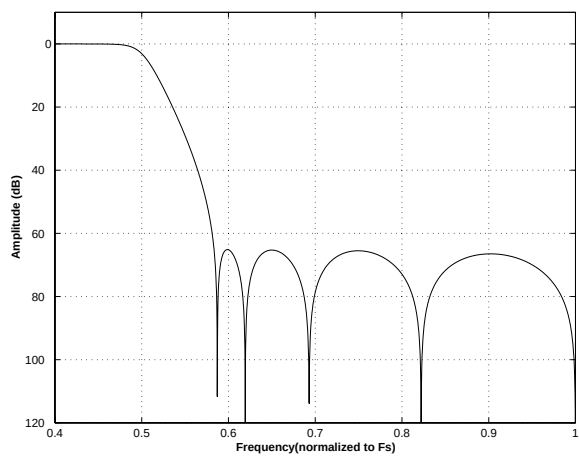


Figure 23. DAC Single-Speed (slow) Stopband Rejection

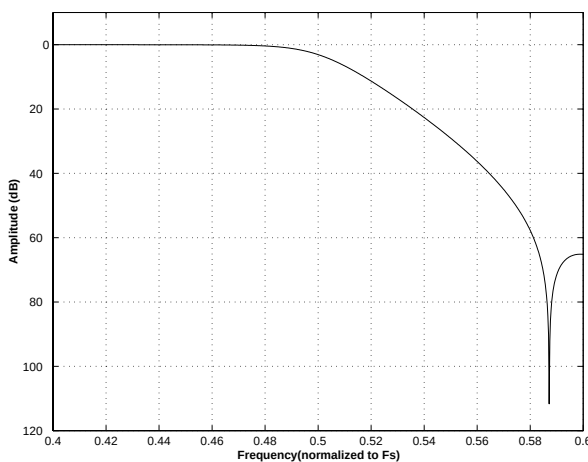


Figure 24. DAC Single-Speed (slow) Transition Band

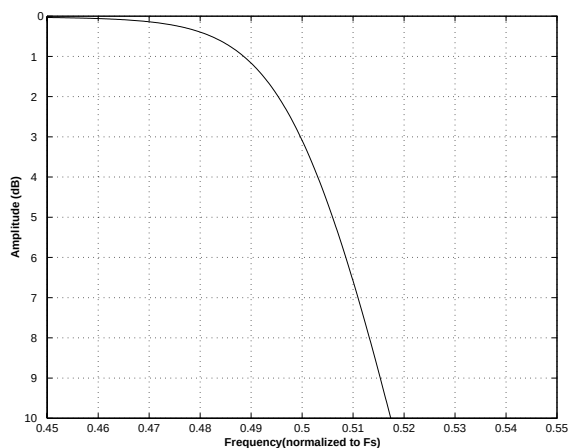


Figure 25. DAC Single-Speed (slow) Transition Band (detail)

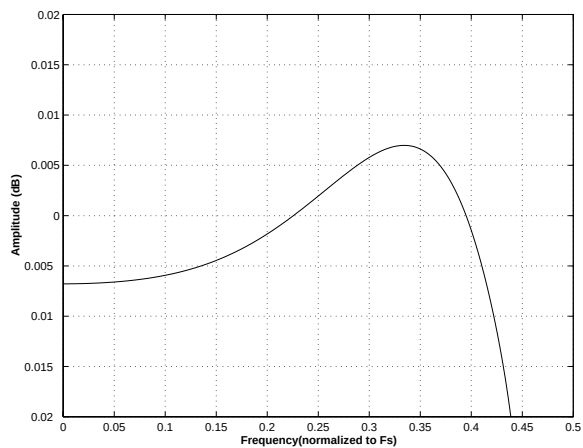


Figure 26. DAC Single-Speed (slow) Passband Ripple

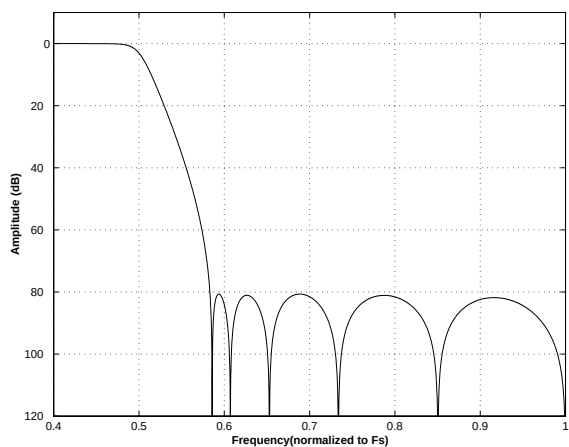


Figure 27. DAC Double-Speed (fast) Stopband Rejection

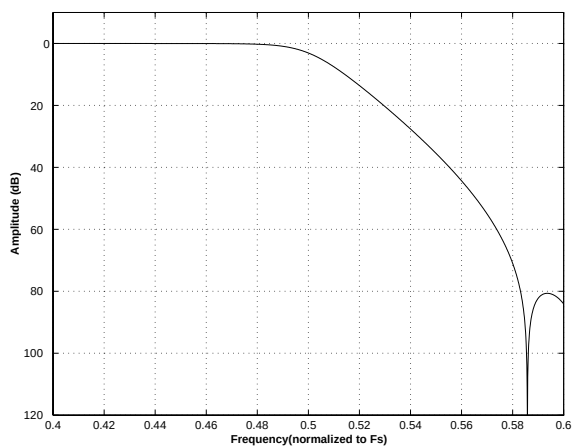


Figure 28. DAC Double-Speed (fast) Transition Band

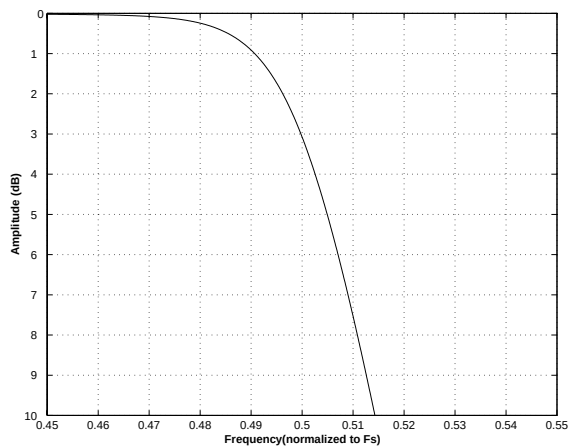


Figure 29. DAC Double-Speed (fast) Transition Band (detail)

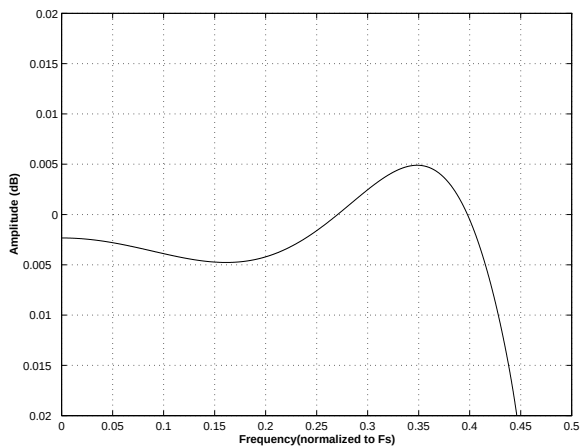
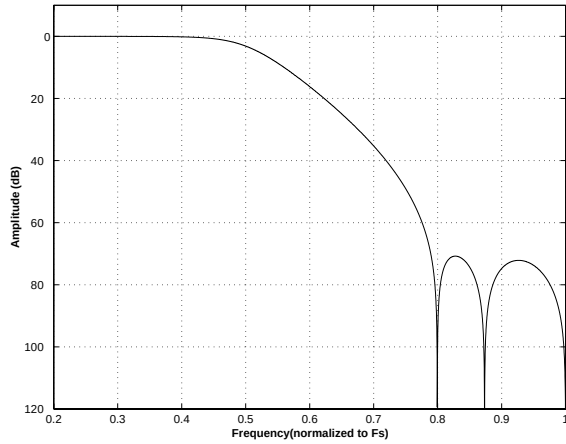
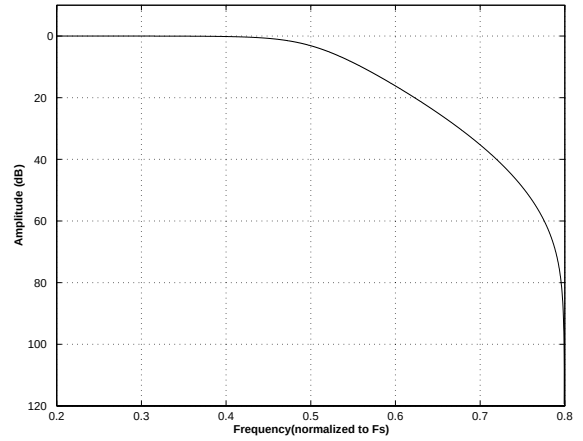
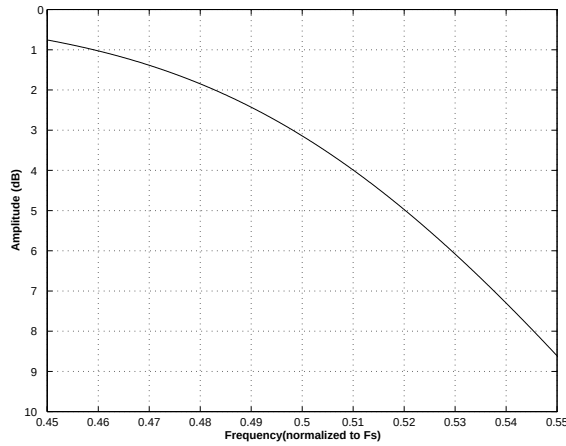
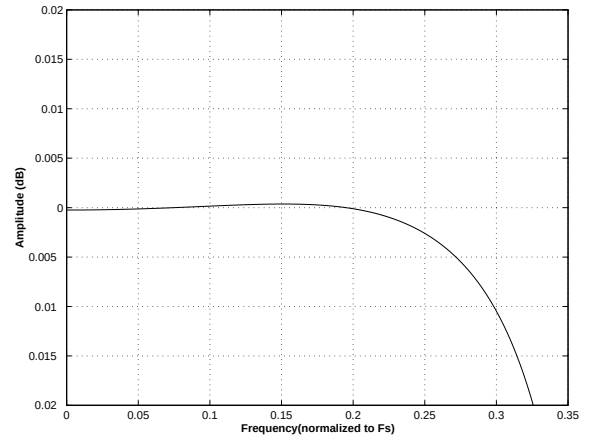
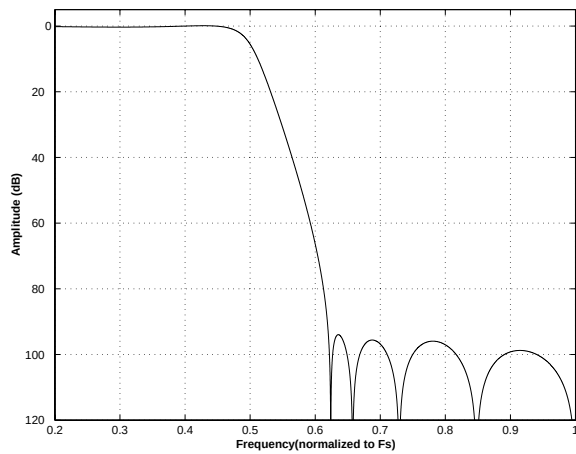
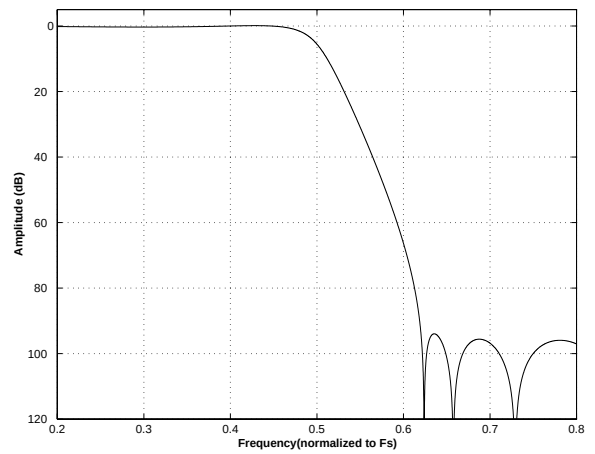


Figure 30. DAC Double-Speed (fast) Passband Ripple


Figure 31. DAC Double-Speed (slow) Stopband Rejection

Figure 32. DAC Double-Speed (slow) Transition Band

Figure 33. DAC Double-Speed (slow) Transition Band (detail)

Figure 34. DAC Double-Speed (slow) Passband Ripple

Figure 35. DAC Quad-Speed (fast) Stopband Rejection

Figure 36. DAC Quad-Speed (fast) Transition Band

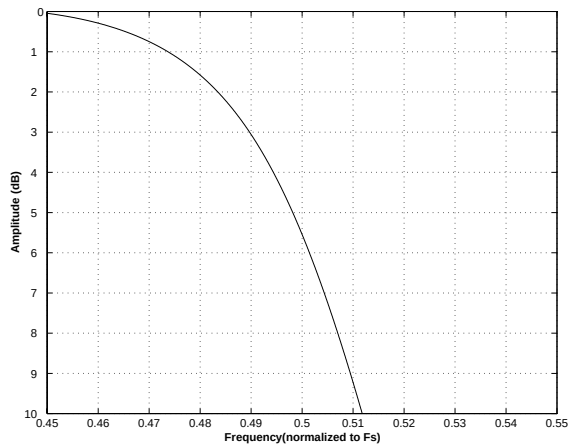


Figure 37. DAC Quad-Speed (fast) Transition Band (detail)

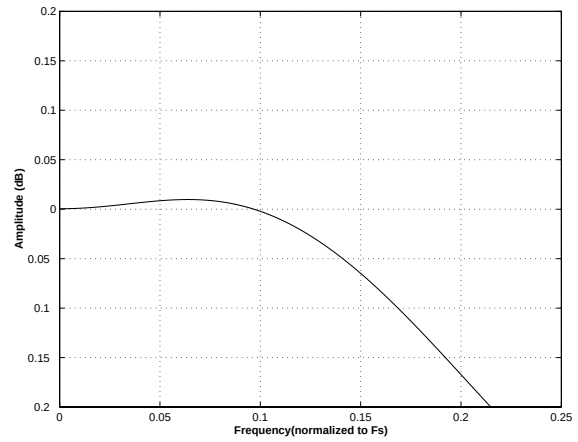


Figure 38. DAC Quad-Speed (fast) Passband Ripple

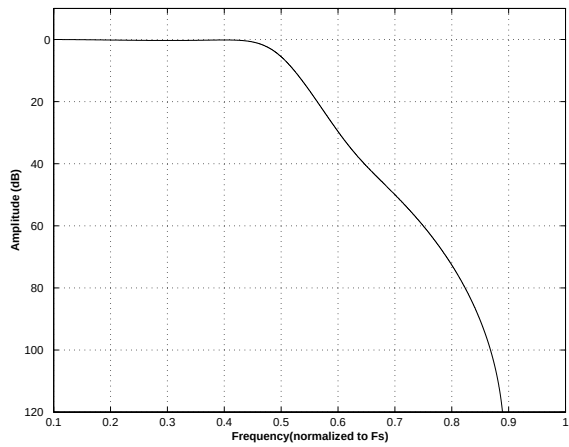


Figure 39. DAC Quad-Speed (slow) Stopband Rejection

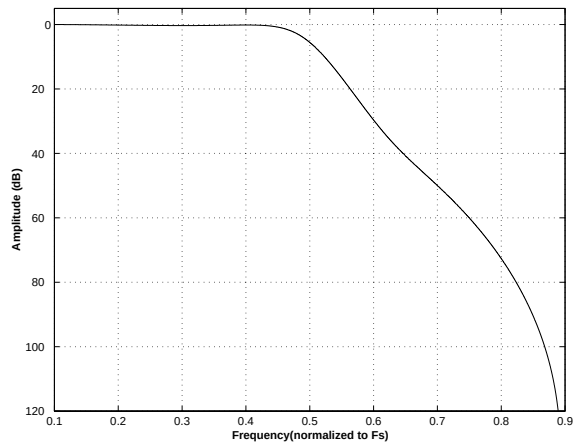


Figure 40. DAC Quad-Speed (slow) Transition Band

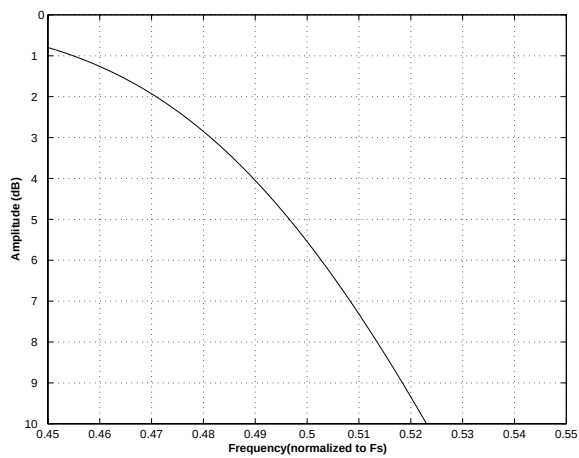


Figure 41. DAC Quad-Speed (slow) Transition Band (detail)

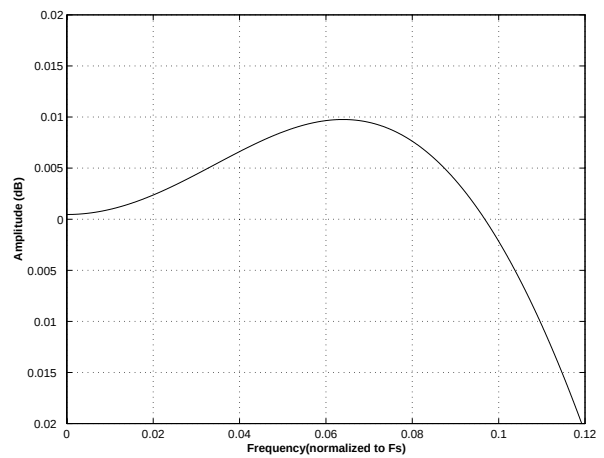
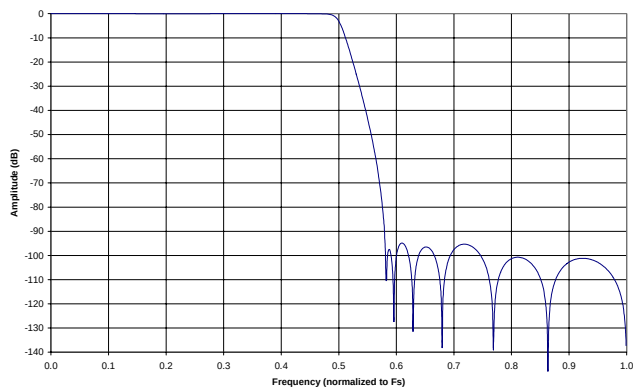
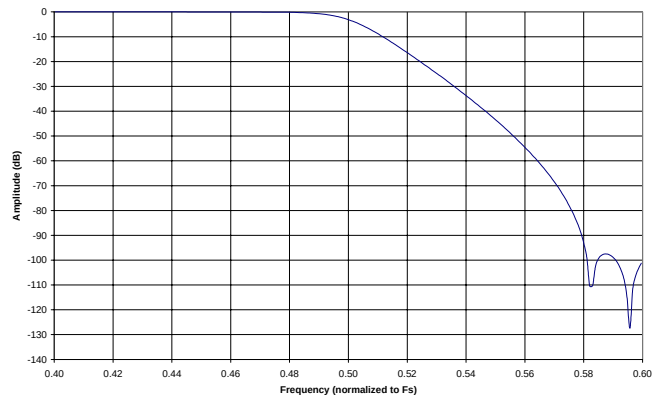
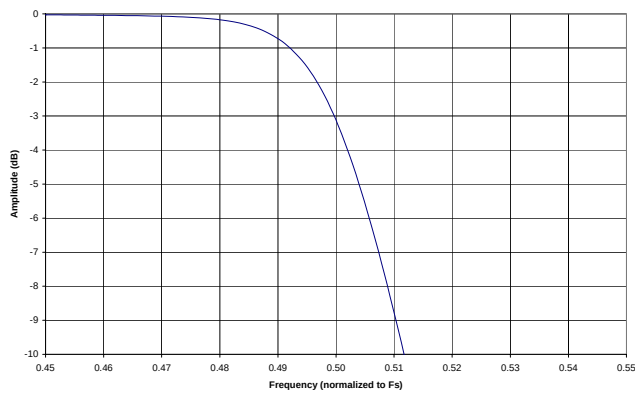
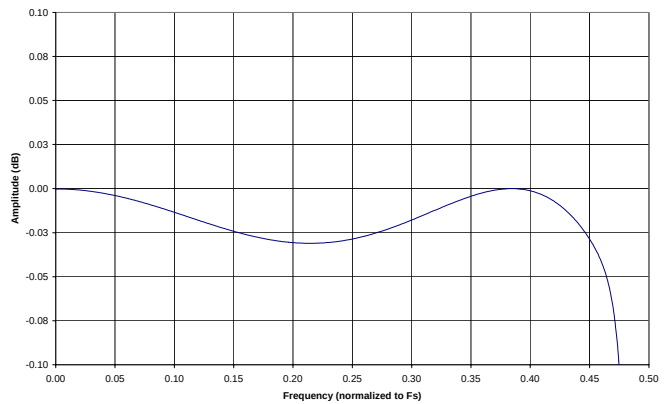
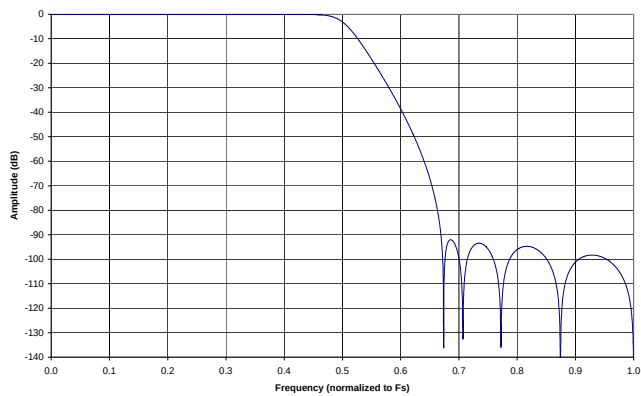
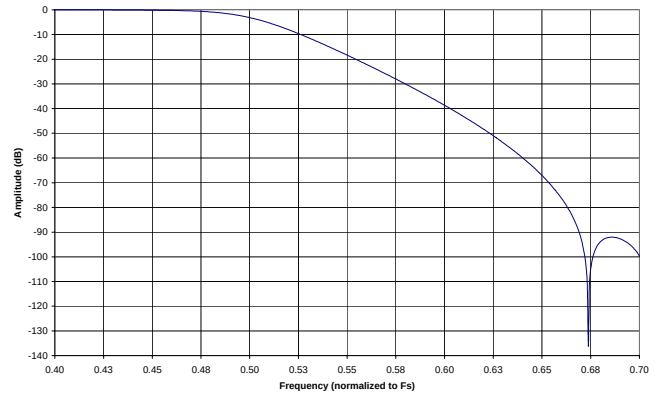
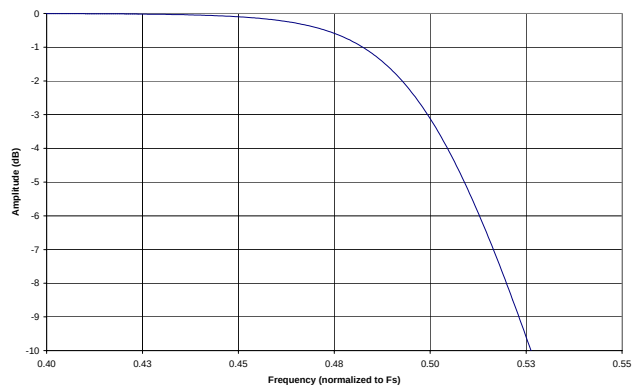
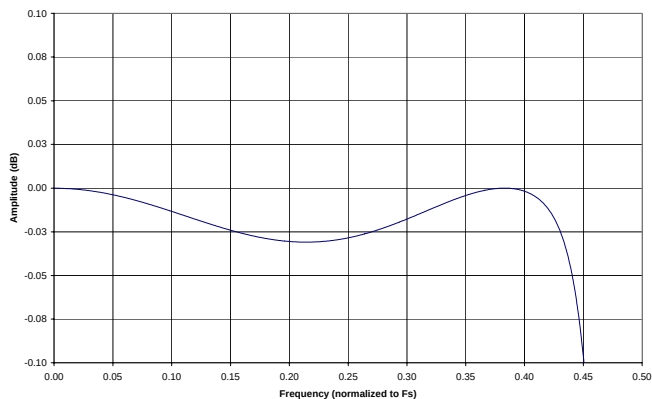
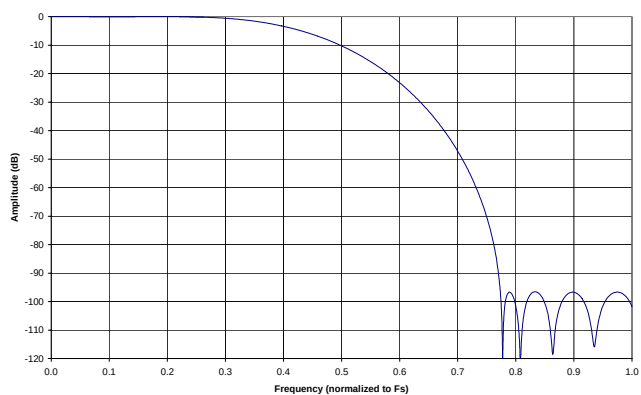
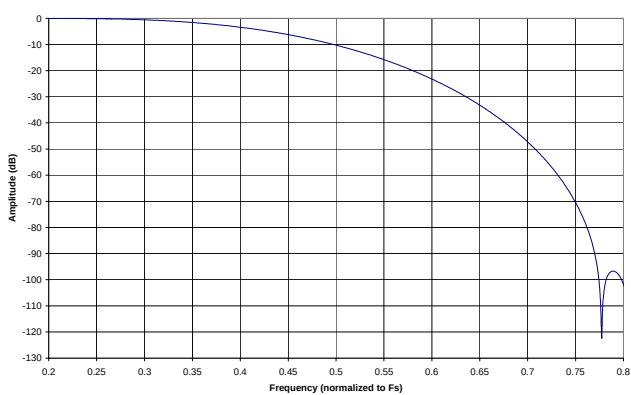
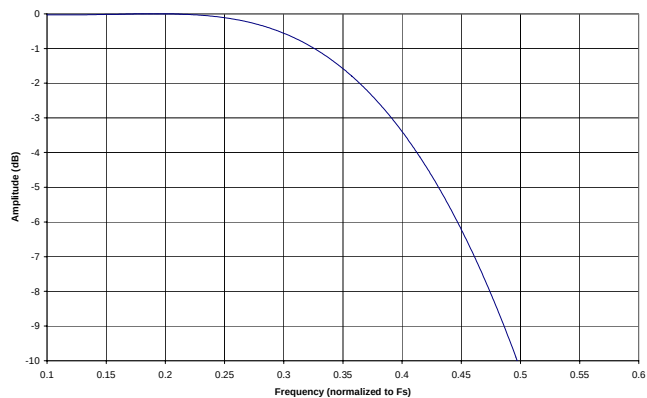
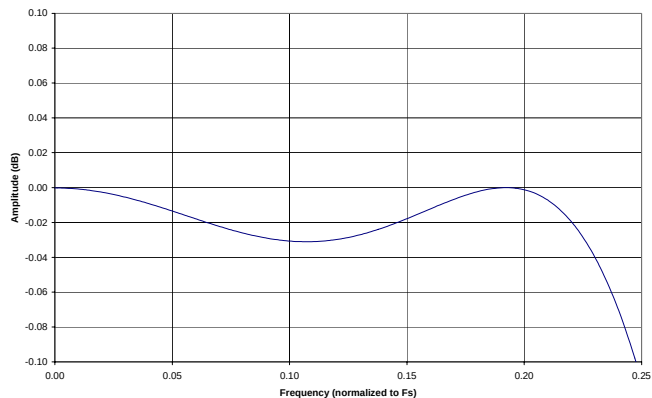


Figure 42. DAC Quad-Speed (slow) Passband Ripple


Figure 43. ADC Single-Speed Mode Stopband Rejection

Figure 44. ADC Single-Speed Mode Transition Band

Figure 45. ADC Single-Speed Mode Transition Band (Detail)

Figure 46. ADC Single-Speed Mode Passband Ripple

Figure 47. ADC Double-Speed Mode Stopband Rejection

Figure 48. ADC Double-Speed Mode Transition Band


Figure 49. ADC Double-Speed Mode Transition Band (Detail)

Figure 50. ADC Double-Speed Mode Passband Ripple

Figure 51. ADC Quad-Speed Mode Stopband Rejection

Figure 52. ADC Quad-Speed Mode Transition Band

Figure 53. ADC Quad-Speed Mode Transition Band (Detail)

Figure 54. ADC Quad-Speed Mode Passband Ripple

12. REVISION HISTORY

Release	Date	Changes
A1	May 2005	Initial Advance Release

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

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