PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE

PM50CTJ060-3

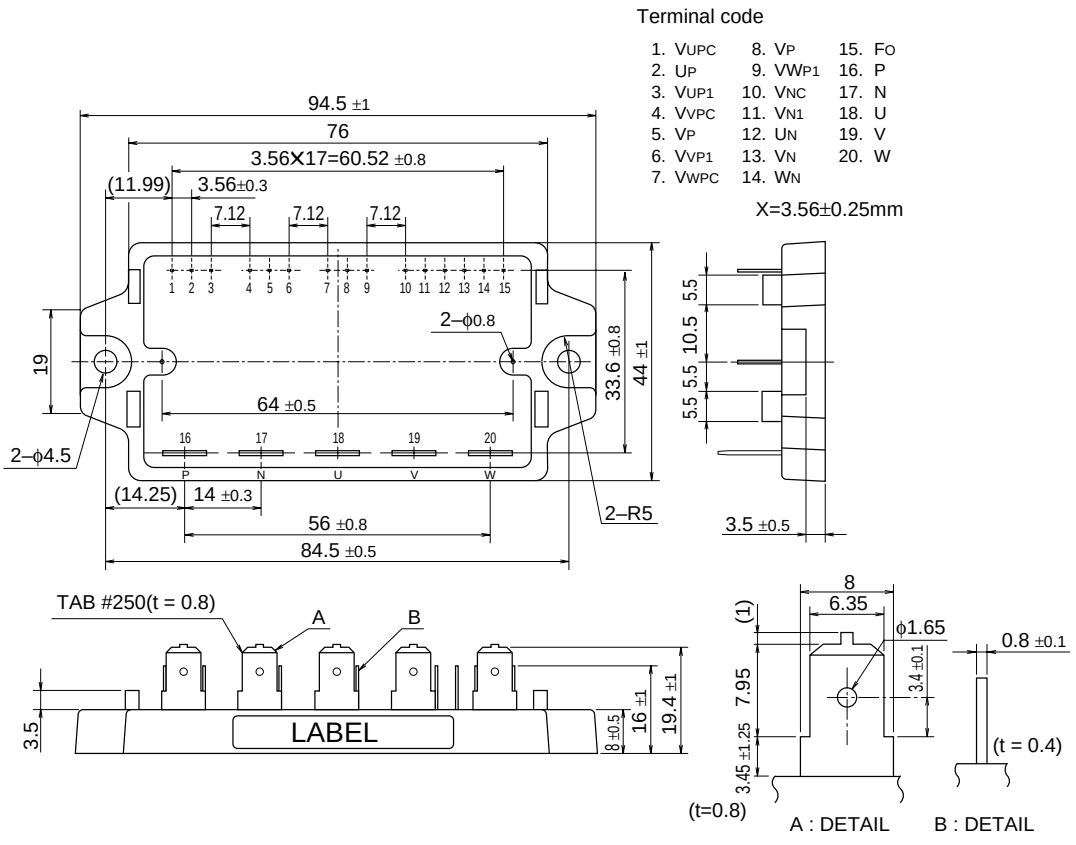
- 4th gen. planer IGBTs are integrated
- 3ϕ 50A, 600V Current-sense IGBT type inverter
- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for over-current, short-circuit, over-temperature & under-voltage
- Acoustic noise-less 3.7kW class inverter application

APPLICATION

Air-conditioner, General purpose inverter, servo drives and other motor controls

OUTLINE DRAWING

Dimensions in mm

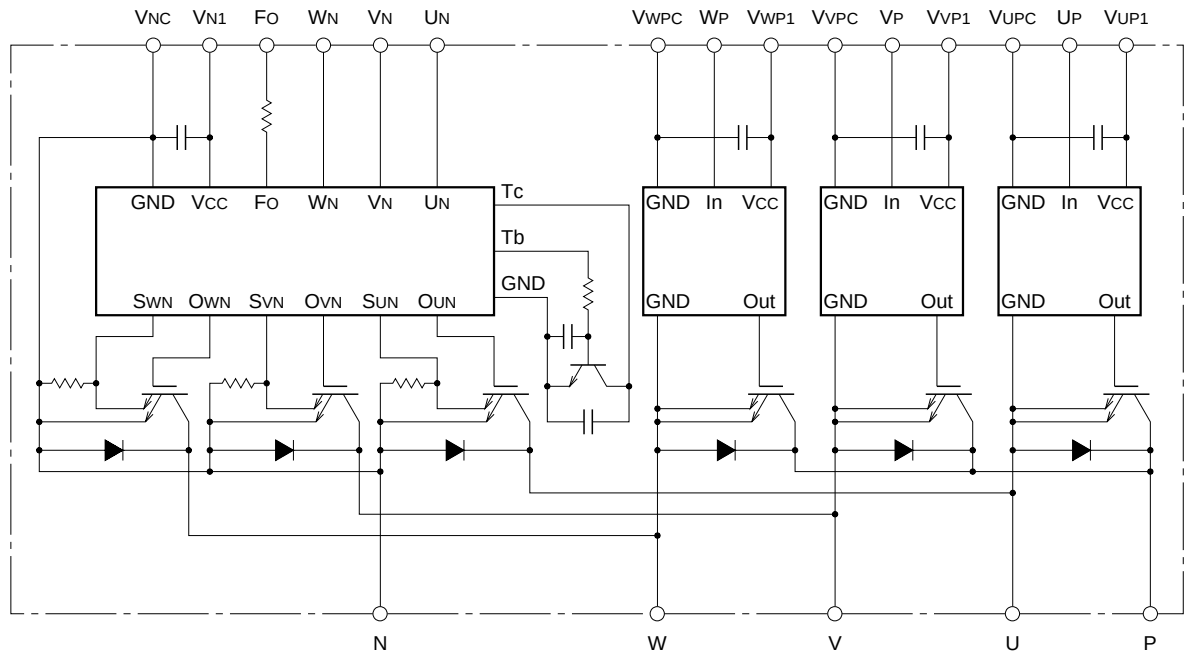


MITSUBISHI ELECTRIC

PM50CTJ060-3

INSULATED PACKAGE
FLAT-BASE TYPE

EQUIVALENT CIRCUIT DIAGRAM



MAXIMUM RATINGS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Applied between : P-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between : P-N, Surge value	500	V
V_{CES}	Collector-emitter voltage		600	V
±I_C	Collector current	T_C = 25°C	50	A
±I_{CP}	Collector current (peak)	T_C = 25°C	100	A
P_C	Collector dissipation	T_C = 25°C	100	W
T_j	Junction temperature		–20 ~ +125*	°C

* The item defines the maximum junction temperature for the power elements (IGBT/Diode) of the IPM to ensure safe operation. However, these power elements can endure junction temperature as high as 150°C instantaneously. To make use of this additional temperature allowance, a detailed study of the exact application conditions is required and, accordingly, necessary information is requested to be provided before use.

CONTROL PART

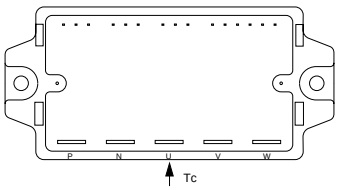
Symbol	Parameter	Conditions	Ratings	Unit
V_D	Supply voltage	Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC} V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
I_{CIN}	Input current	At : U_P, V_P, W_P, U_N, V_N, W_N terminals	20	mA
V_{FO}	Fault output supply voltage	Applied between : F_O-V_{NC}	20	V
I_{FO}	Fault output current	Sink current of F_O terminals	20	mA

MITSUBISHI ELECTRIC

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply voltage protected by OC & SC	V_D = 13.5 ~ 16.5V, Inverter part, T_j = 125°C start	400	V
T_C	Module case operating temperature	(Note 1)	–20 ~ +100	°C
T_{stg}	Storage temperature		–40 ~ +125	°C
V_{iso}	Isolation voltage	60Hz, sinusoidal, Charged part to Base, AC · 1 min.	2500	V_{rms}

Note 1 : T_C measurement point.



THERMAL RESISTANCES

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Tye.	Max.	
$R_{th(j-c)Q}$	Junction to case thermal resistances	Inverter IGBT part (per 1/6 module)	—	—	1.2	°C / W
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	—	—	2.9	°C / W
$R_{th(c-f)}$	Contact thermal resistance	Case to fin, (per 1 module) thermal grease applied	—	—	0.4	°C / W

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_D = 15V, I_{CIN} = 10mA, I_C = 50A, Pulsed (Fig. 1)	T_j = 25°C	—	1.8	2.6	V
			T_j = 125°C	—	2.0	3.0	
V_{EC}	FWD forward voltage	–I_C = 50A, V_D = 15V, I_{CIN} = 0mA (Fig. 2)		—	2.5	3.5	V
t_{on}	Switching time	V_D = 15V, I_{CIN} = 0mA↔10mA, V_{CC} = 300V, I_C = 50A, T_j = 125°C, Inductive Load (Upper-Lower Arm) (Fig. 3)		0.5	1.0	2.0	µs
t_{rr}				—	0.1	—	µs
$t_{c(on)}$				—	0.3	0.9	µs
t_{off}				—	3.0	4.0	µs
$t_{c(off)}$				—	1.0	2.0	µs
I_{CES}	Collector-emitter cutoff current	V_{CE} = V_{CES}, V_D = 15V (Fig. 4)	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	

CONTROL PART

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	V_D = 15V, I_{CIN} = 0mA	V_{N1}-V_{NC}	—	25	35	mA
			V_{XP1}-V_{XPC}	—	5	10	
$I_{th(ON)}$	Input on threshold current	At : U_P-V_{UPC}, V_P-V_{VPC}, W_P-V_{WPC}		1	3	5	mA
$I_{th(OFF)}$	Input off threshold current	U_N · V_N · W_N-V_{NC} terminals		1	3	5	mA
OC	Over current trip level	–20°C ≤ T_j ≤ 125°C, V_D = 15V (Fig. 5, 6) (Lower Arm only)		65	91	—	A
SC	Short circuit trip level	–20°C ≤ T_j ≤ 125°C, V_D = 15V (Fig. 5, 6) (Lower Arm only)		—	130	—	A
$t_{off(OC)}$	Over current delay time	V_D = 15V (Fig. 5, 6)		—	10	—	µs
OT	Over temperature protection	Baseplate	Trip level	100	110	120	°C
OT_r		Temperature detection, V_D = 15V	Reset level	—	90	—	°C
UV	Supply circuit under voltage protection	–20°C ≤ T_j ≤ 125°C (Lower Arm only)	Trip level	11.5	12.0	12.5	V
UV_r			Reset level	—	12.5	—	V
$I_{FO(H)}$	Fault output current	V_D = 15V, V_{FO} = 15V (Note 2)		—	—	0.01	mA
$I_{FO(L)}$				—	10	15	mA
t_{FO}	Minimum fault output pulse width	V_D = 15V (Note 2)		1.0	1.8	—	ms

Note 2 : Fault output is given only when the internal OC, SC, OT & UV protections schemes of lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Mounting torque	Mounting part screw : M4	0.98	1.18	1.47	N·m
—	Weight		—	80	—	g

RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage	Applied across P-N terminals	0	300	400	V
V_D		Applied between : V_{UP1}-V_{UPC}, V_{VP1}-V_{VPC} V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
$I_{CIN(ON)}$	Input on current	At : U_P, V_P, W_P, U_N, V_N, W_N terminals	5	10	20	mA
$I_{CIN(OFF)}$	Input off current		0	—	1	mA
f_{PWM}	PWM input frequency	For IPM's each input signals, (Fig. 7)	—	—	8	kHz
t_{dead}	Arm shoot-through blocking time	For IPM's each input signals, (Fig. 7)	3.5	—	—	µs

PRECAUTIONS FOR TESTING

1. Before appling any control supply voltage (V_D), the input signals should be turned on from its off state. After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “OC” and “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device. (These test should not be done by using a curve tracer or its equivalent.)

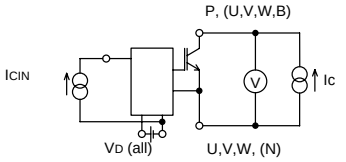


Fig.1 $V_{CE(sat)}$ Test

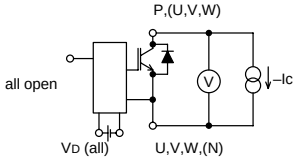


Fig.2 V_{EC} Test

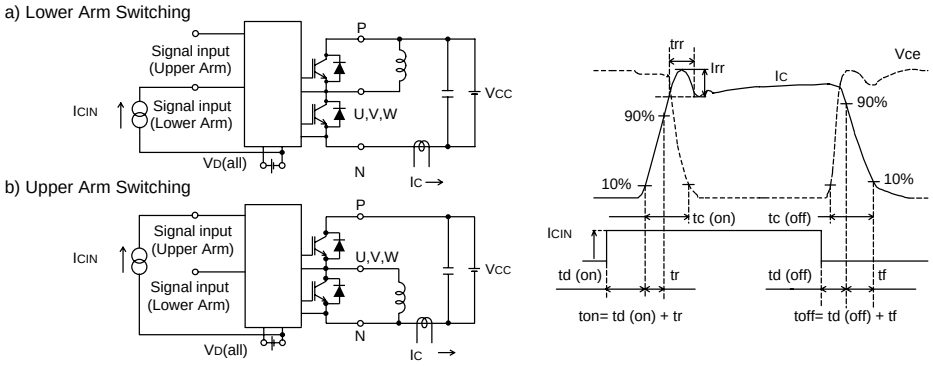


Fig. 3 Switching time Test circuit and waveform

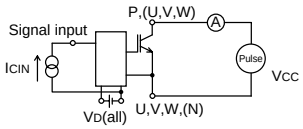


Fig.4 I_{CES} Test

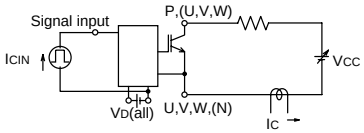


Fig. 5 OC and SC Test

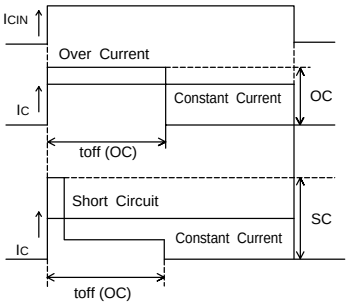


Fig. 6 OC and SC Test waveform

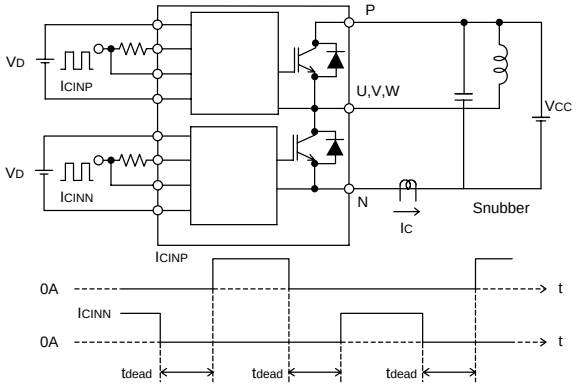
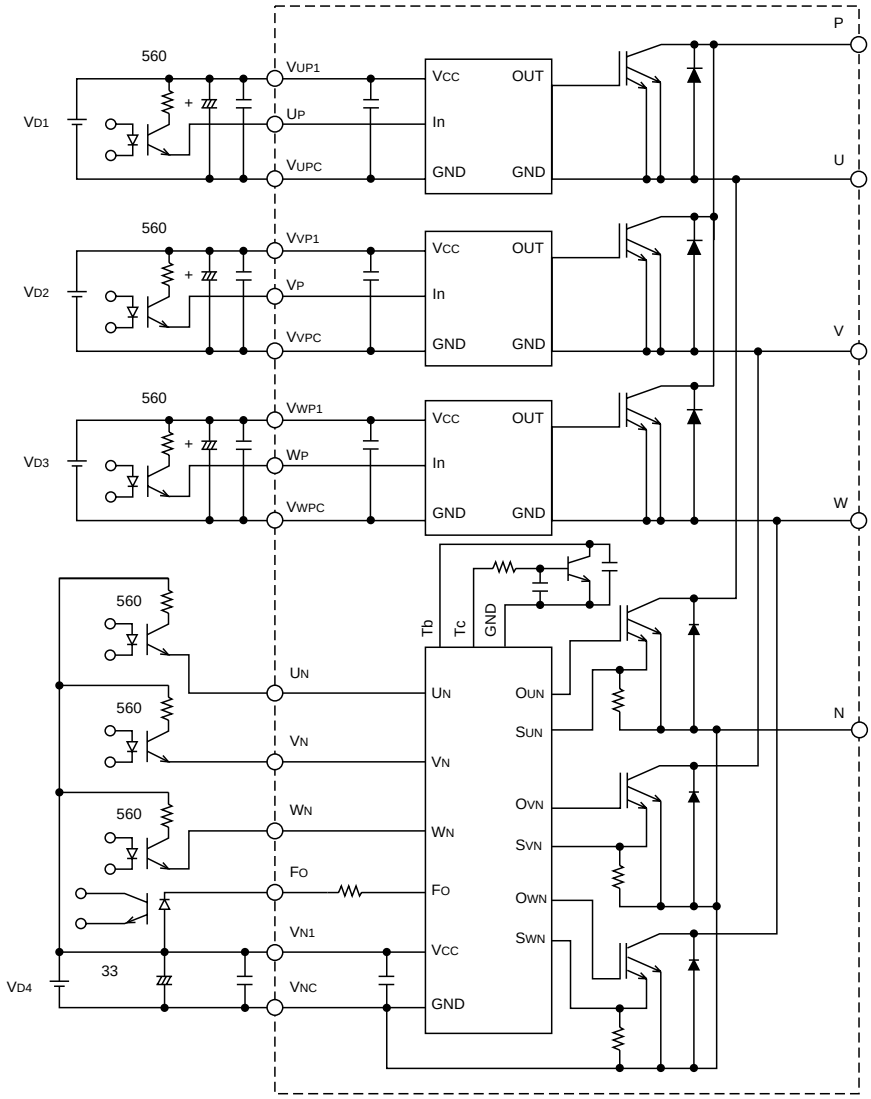


Fig. 7 Dead time measurement point example



NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each switching opto-coupler.
- Slow switching opto-coupler : CTR = 100%~200%
- Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.
- Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common-mode noise from AC line and improve noise immunity of the system.