FAIRCHILD SEMICONDUCTOR™

February 1999

# FDC6506P

## Dual P-Channel Logic Level PowerTrench™ MOSFET

### General Description

These P-Channel logic level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

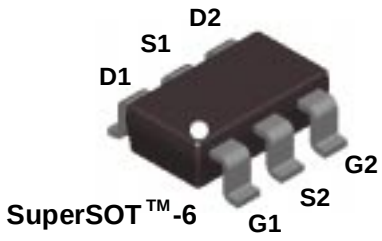
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

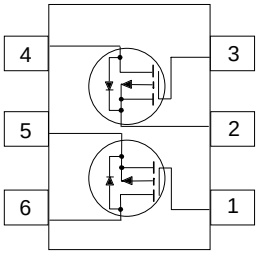
### Applications

- Load switch
- Battery protection
- Power management

### Features

- -1.8 A, -30 V. $R_{DS(on)}$ = 0.170 Ω @ $V_{GS}$ = -10 V
  $R_{DS(on)}$ = 0.280 Ω @ $V_{GS}$ = -4.5 V
- Low gate charge (2.3nC typical).
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | -30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | -1.8 | A |
| | - Pulsed | | -10 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 0.96 | W |
| | | (Note 1b) | 0.9 | |
| | | (Note 1c) | 0.7 | |
| $T_J$, $T_{stg}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 130 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 60 | °C/W |

## Package Outlines and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|
| .506 | FDC6506P | 7'' | 8mm | 3000 units |

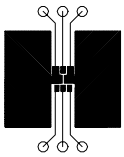
## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

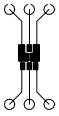
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = -250 μA | -30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250 μA, Referenced to 25°C | | -20 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -24 V, $V_{GS}$ = 0 V | | | -1 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 μA | -1 | -1.8 | -3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = -250 μA, Referenced to 25°C | | 4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = -10 V, $I_D$ = -1.8 A<br>$V_{GS}$ = -10 V, $I_D$ = -1.8 A @125°C<br>$V_{GS}$ = -4.5 V, $I_D$ = -1.4 A | | 0.14<br>0.20<br>0.22 | 0.17<br>0.27<br>0.28 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = -10 V, $V_{DS}$ = - 5 V | -10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -5 V, $I_D$ = -1.8 A | | 3 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 190 | | pF |
| $C_{oss}$ | Output Capacitance | | | 70 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 30 | | pF |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -15 V, $I_D$ = -1 A, $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 Ω | | 7 | 14 | ns |
| $t_r$ | Turn-On Rise Time | | | 8 | 16 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 14 | 25 | ns |
| $t_f$ | Turn-Off Fall Time | | | 2 | 6 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -5 V, $I_D$ = -1.8 A, $V_{GS}$ = -10 V | | 2.3 | 3.5 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 1 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 0.8 | | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | -0.8 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = -0.8 A (Note 2) | | -0.8 | -1.2 | V |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.Both devices are assumed to be operating and sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 $in^2$ pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 $in^2$ pad of 2 oz. copper.

c) 180 °C/W when mounted on a 0.0015 $in^2$ pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

## Typical Characteristics

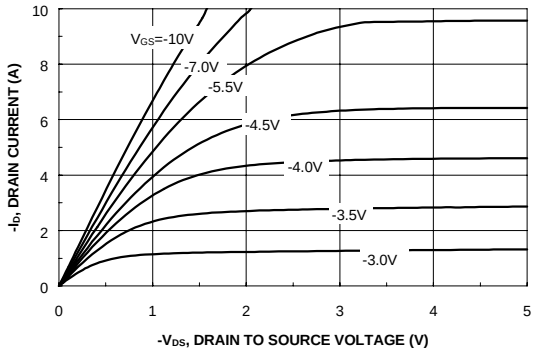



**Figure 1. On-Region Characteristics.**

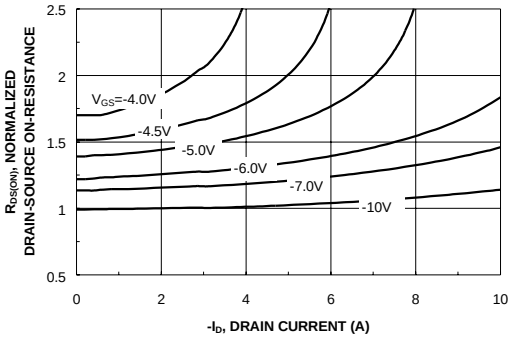



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

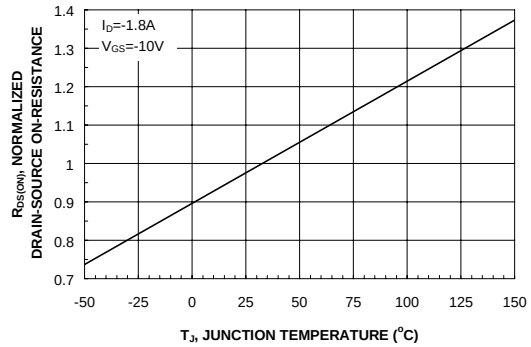



**Figure 3. On-Resistance Variation with Temperature.**

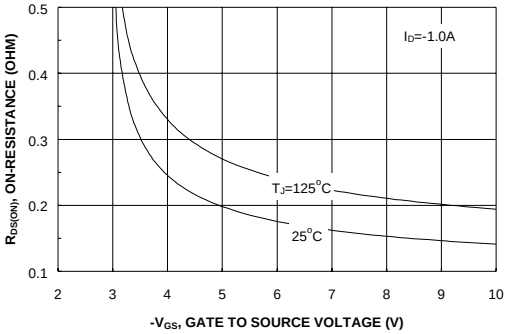



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

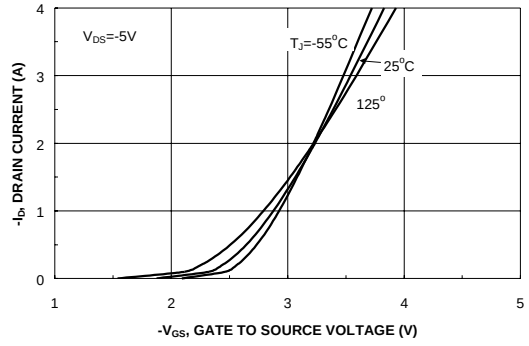



**Figure 5. Transfer Characteristics.**

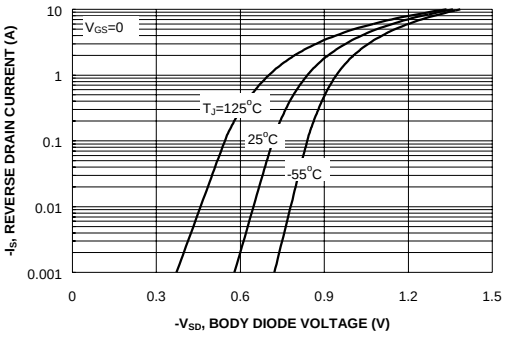



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics (continued)

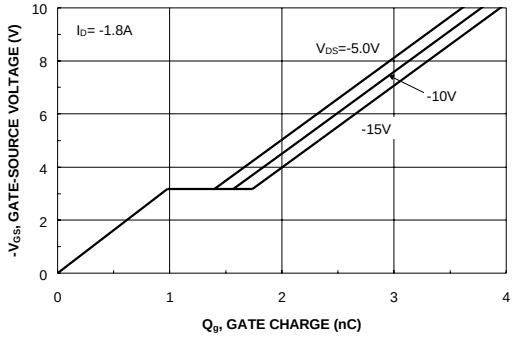



**Figure 7. Gate-Charge Characteristics.**

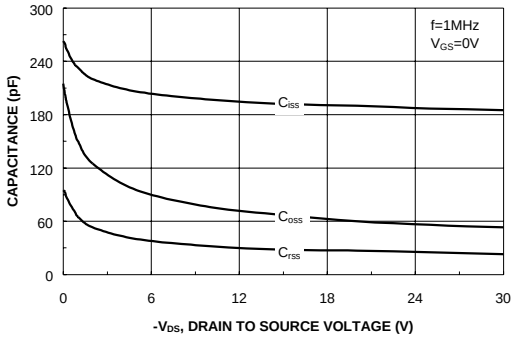



**Figure 8. Capacitance Characteristics.**

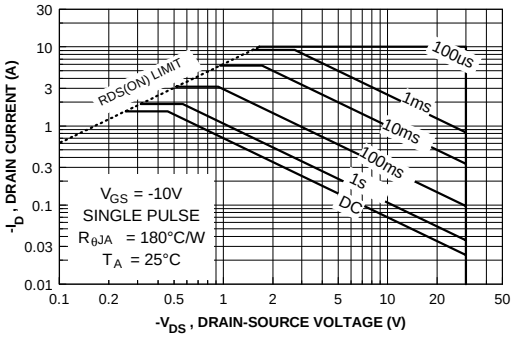



**Figure 9. Maximum Safe Operating Area.**

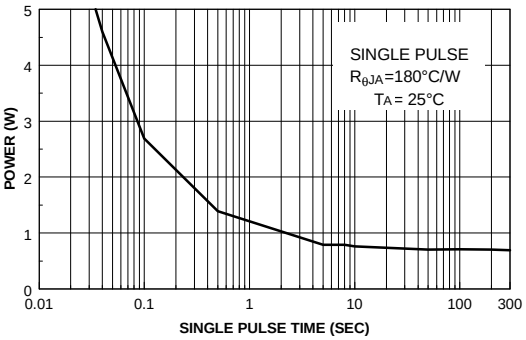



**Figure 10. Single Pulse Maximum Power Dissipation.**

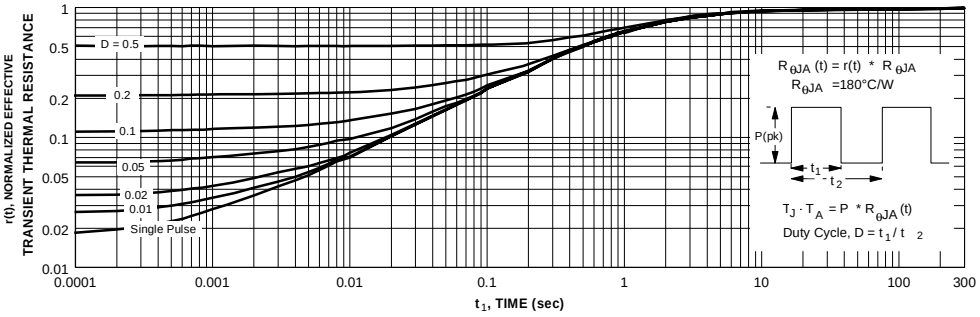
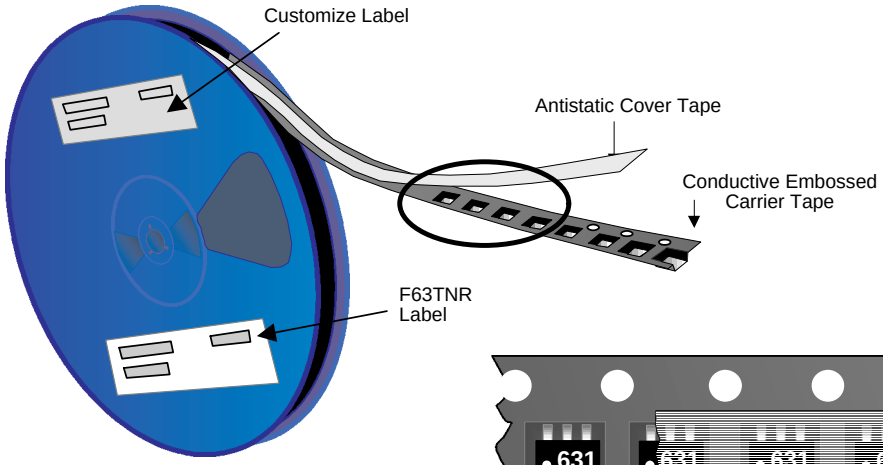



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.
Transient themal response will change depending on the circuit board design.

# SuperSOT™-6 Tape and Reel Data and Package Dimensions

**SSOT-6 Packaging**
**Configuration:** Figure 1.0

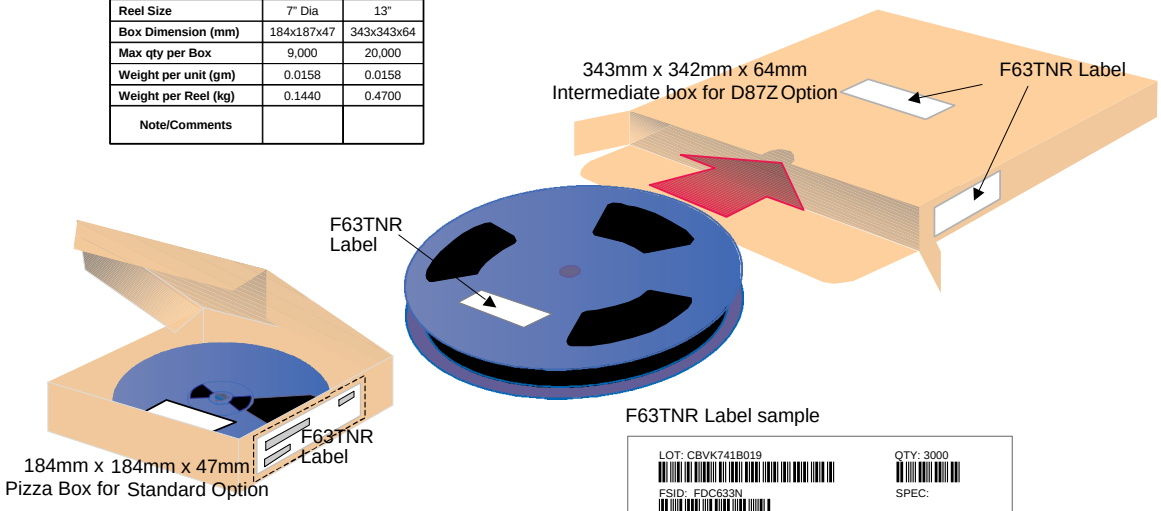






**SSOT-6 Unit Orientation**

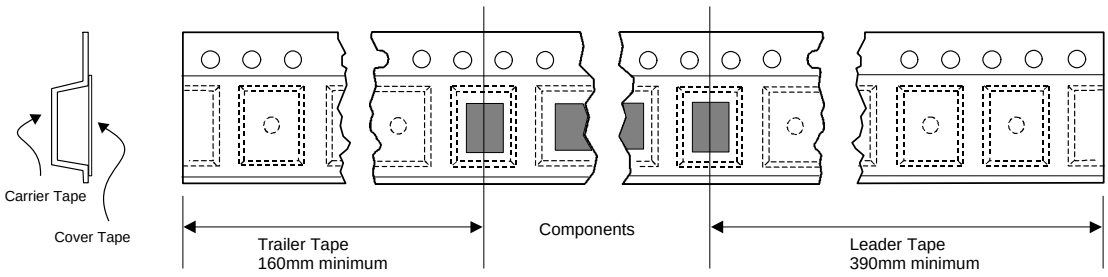
| SSOT-6 Packaging Information | | |
|---|---|---|
| **Packaging Option** | Standard (no flow code) | D87Z |
| **Packaging type** | TNR | TNR |
| **Qty per Reel/Tube/Bag** | 3,000 | 10,000 |
| **Reel Size** | 7" Dia | 13" |
| **Box Dimension (mm)** | 184x187x47 | 343x343x64 |
| **Max qty per Box** | 9,000 | 20,000 |
| **Weight per unit (gm)** | 0.0158 | 0.0158 |
| **Weight per Reel (kg)** | 0.1440 | 0.4700 |
| **Note/Comments** | | |




F63TNR Label sample



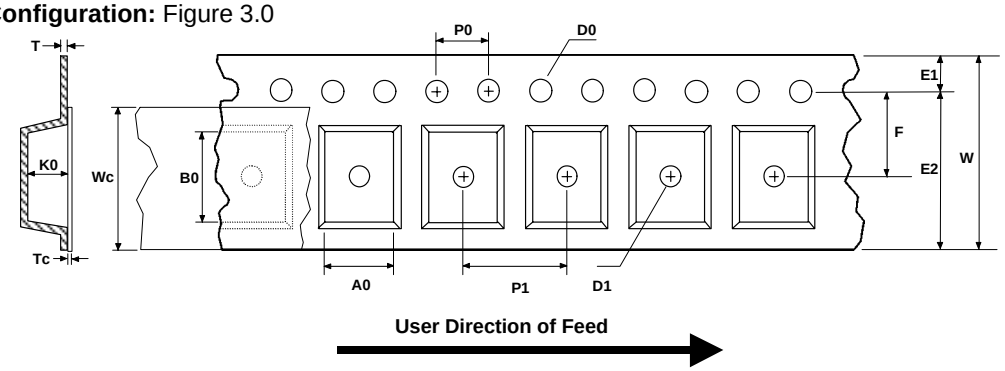

**SSOT-6 Tape Leader** **Trailer**
**Configuration:** Figure 2.0



# SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

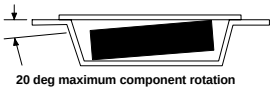
## SSOT-6 Embossed Carrier Tape

**Configuration:** Figure 3.0

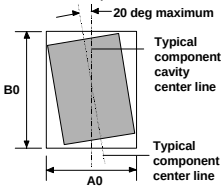



| Dimensions are in millimeter | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Pkg type** | **A0** | **B0** | **W** | **D0** | **D1** | **E1** | **E2** | **F** | **P1** | **P0** | **K0** | **T** | **Wc** | **Tc** |
| **SSOT-6** (8mm) | 3.23 +/-0.10 | 3.18 +/-0.10 | 8.0 +/-0.3 | 1.55 +/-0.05 | 1.00 +/-0.125 | 1.75 +/-0.10 | 6.25 min | 3.50 +/-0.05 | 4.0 +/-0.1 | 4.0 +/-0.1 | 1.37 +/-0.10 | 0.255 +/-0.150 | 5.2 +/-0.3 | 0.06 +/-0.02 |

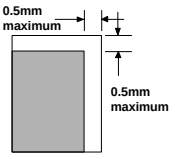
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).




Sketch A (Side or Front Sectional View)
**Component Rotation**

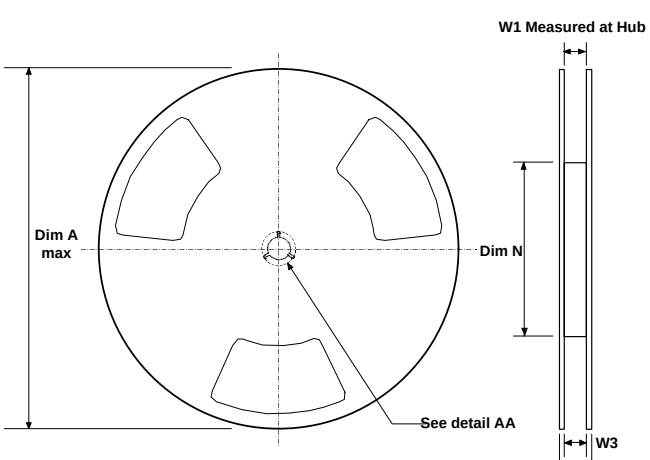



Sketch B (Top View)
**Component Rotation**

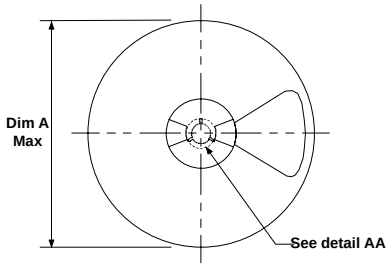



Sketch C (Top View)
**Component lateral movement**

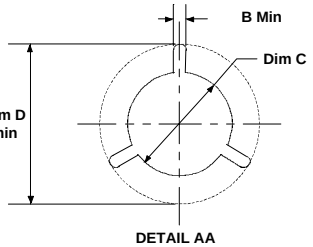
## SSOT-6 Reel Configuration: Figure 4.0




**13" Diameter Option**



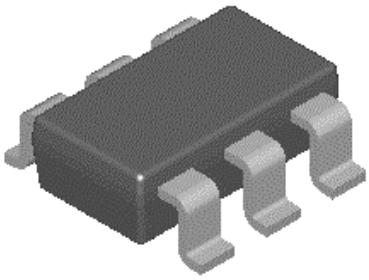

7" **Diameter Option**

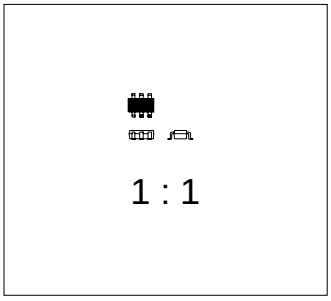



| Dimensions are in inches and millimeters | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Tape Size** | **Reel Option** | **Dim A** | **Dim B** | **Dim C** | **Dim D** | **Dim N** | **Dim W1** | **Dim W2** | **Dim W3 (LSL-USL)** |
| 8mm | 7" Dia | 7.00 177.8 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 2.165 55 | 0.331 +0.059/-0.000 8.4 +1.5/0 | 0.567 14.4 | 0.311 – 0.429 7.9 – 10.9 |
| 8mm | 13" Dia | 13.00 330 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 4.00 100 | 0.331 +0.059/-0.000 8.4 +1.5/0 | 0.567 14.4 | 0.311 – 0.429 7.9 – 10.9 |

## SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

# SuperSOT™-6 (FS PKG Code 31, 33)

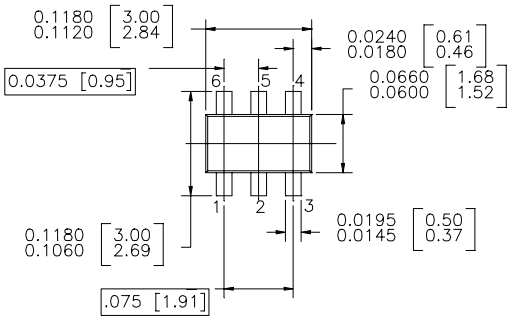


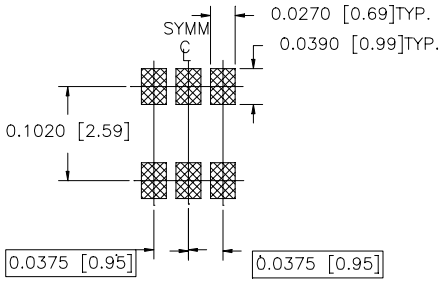



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

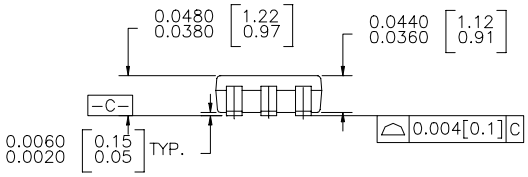
Part Weight per unit (gram): 0.0158

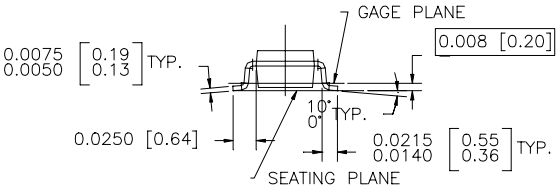



LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS




NOTES : UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH : 150 MICROINCHES 93.81 MICROMETERS)
MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

SUPER SOT 6 LEADS

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SuperSOT™-8
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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