



STD5NM60 STB8NM60 - STP8NM60

N-channel 650 V @Tjmax, 0.9 Ω , 8 A MDmesh™ Power MOSFET
TO-220, TO-220FP, D²PAK, DPAK, IPAK

Features

Type	V _{DSS}	R _{DS(on)}	I _D	P _w
STD5NM60	650 V	< 1 Ω	5 A	96 W
STD5NM60-1	650 V	< 1 Ω	5 A	96 W
STB8NM60	650 V	< 1 Ω	5 A	100 W
STP8NM60	650 V	< 1 Ω	8 A	100 W
STP8NM60FP	650 V	< 1 Ω	8 A ⁽¹⁾	30 W

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the multiple drain process with the company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

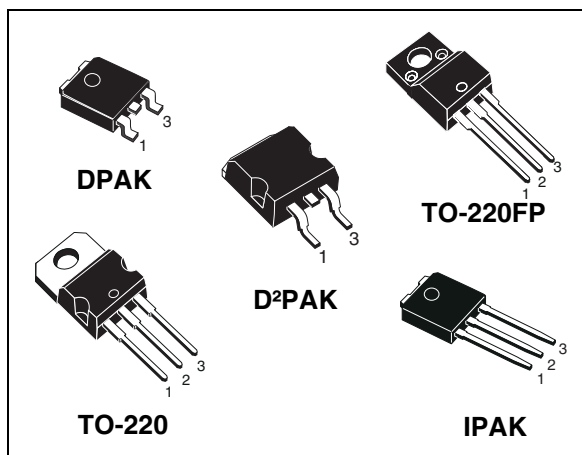


Figure 1. Internal schematic diagram

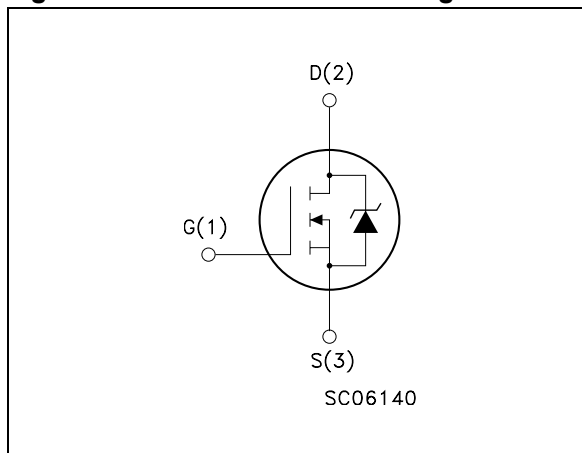


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD5NM60-1	D5NM60	IPAK	Tube
STD5NM60T4	D5NM60	DPAK	Tape & reel
STB8NM60T4	B8NM60	D ² PAK	Tape & reel
STP8NM60	P8NM60	TO-220	Tube
STP8NM60FP	P8NM60FP	TO-220FP	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220 D ² PAK	TO-220FP	IPAK DPAK	
V _{GS}	Gate-source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25 °C	8	8 ⁽¹⁾	5	A
I _D	Drain current (continuous) at T _C = 100 °C	5	5 ⁽¹⁾	3.1 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	32	32 ⁽¹⁾	20 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	100	30	96	W
	Derating factor	0.8	0.24	0.0.4	W/°C
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15			V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)	--	2500	--	V
T _J T _{stg}	Operating junction temperature Storage temperature	-55 to 150			°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. I_{SD} ≤ 5 A, di/dt ≤ 400 A/μs, V_{DD} = 80%V_{(BR)DSS}

Table 2. Thermal resistance

Symbol	Parameter	Value			Unit
		TO-220 D ² PAK	IPAK DPAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	1.25	1.3	4.16	°C/W
R _{thj-a}	Thermal resistance junction-ambient max	62.5			°C/W
T _I	Maximum lead temperature for soldering purpose	300			°C

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J Max)	2.5	A
E _{AS}	Single pulse avalanche energy (starting T _J =25 °C, I _D =I _{AS} , V _{DD} =50 V)	200	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		0.9	1	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$V_{DS} = I_{D(on)} \times R_{DS(on)max}$, $I_D = 2.5\text{ A}$		2.4		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		400 100 10		pF pF pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to } 480\text{ V}$		50		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 12)		13 5 6	18	nC nC nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=300\text{ V}$, $I_D=2.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ (see Figure 17)		14		ns
t_r	Rise time			10		ns
$t_{d(off)}$	Turn-off delay time			23		ns
t_f	Fall time			10		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=480\text{ V}$, $I_D=5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$		7		ns
t_f	Fall time			10		ns
t_c	Cross-over time			17		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=5\text{ A}$, $V_{GS}=0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD}=5\text{ A}$, $V_{DD}=100\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, (see Figure 22)		300		ns
Q_{rr}	Reverse recovery charge			1.95		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$I_{SD}=5\text{ A}$, $V_{DD}=100\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 22)		445		ns
Q_{rr}	Reverse recovery charge			3.00		μC
I_{RRM}	Reverse recovery current			13.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220/D²PAK

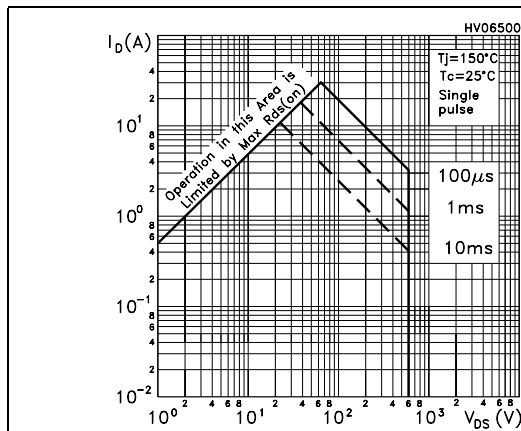


Figure 3. Thermal impedance for TO-220/D²PAK

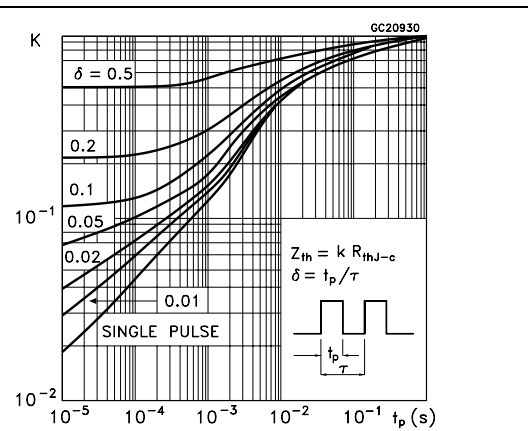


Figure 4. Safe operating area for TO-220FP

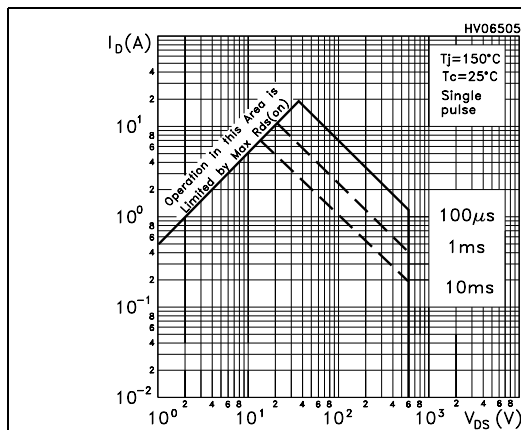


Figure 5. Thermal impedance for TO-220FP

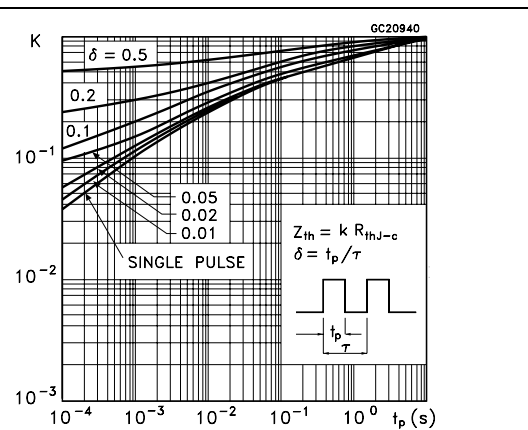


Figure 6. Safe operating area for DPAK/IPAK

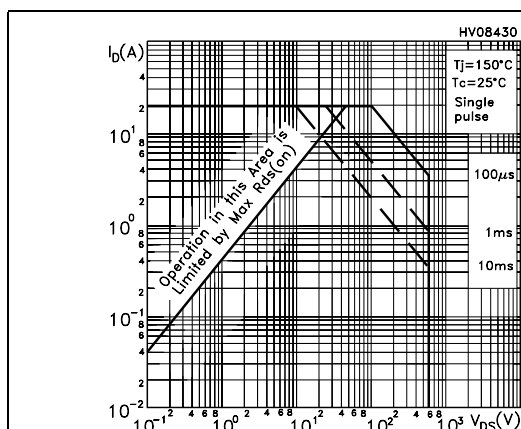


Figure 7. Thermal impedance for DPAK/IPAK

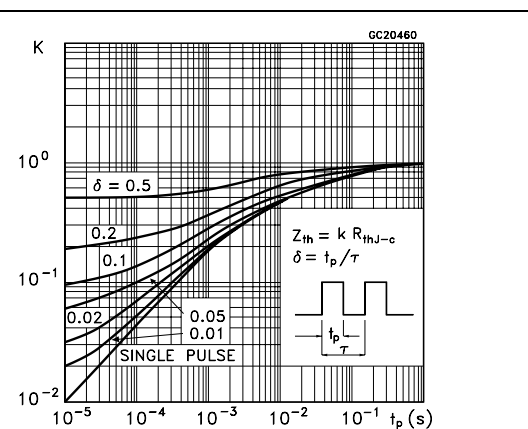


Figure 8. Output characteristics

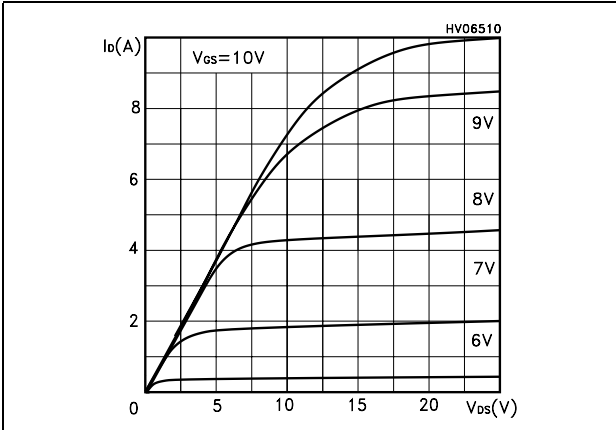


Figure 9. Transfer characteristics

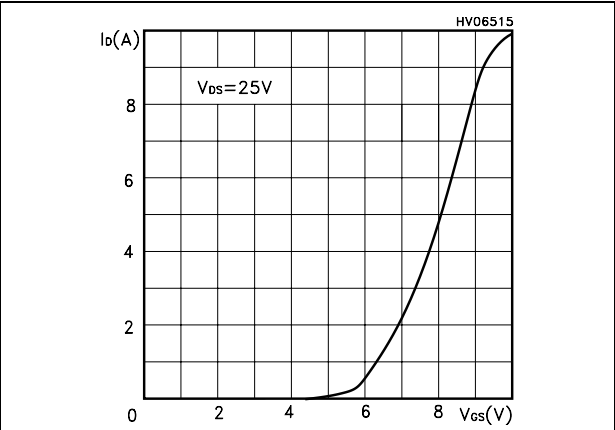


Figure 10. Transconductance

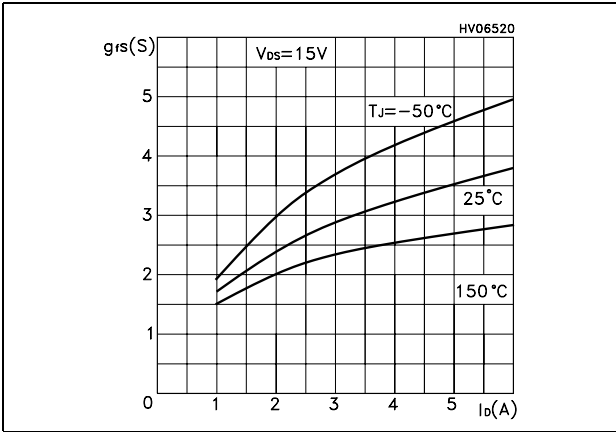


Figure 11. Static drain-source on resistance

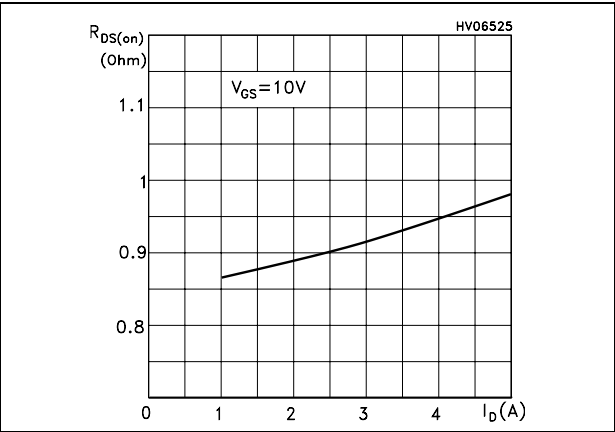


Figure 12. Gate charge vs gate-source voltage

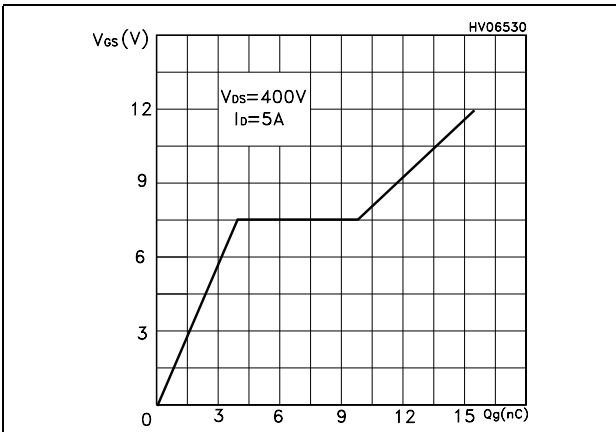


Figure 13. Capacitance variations

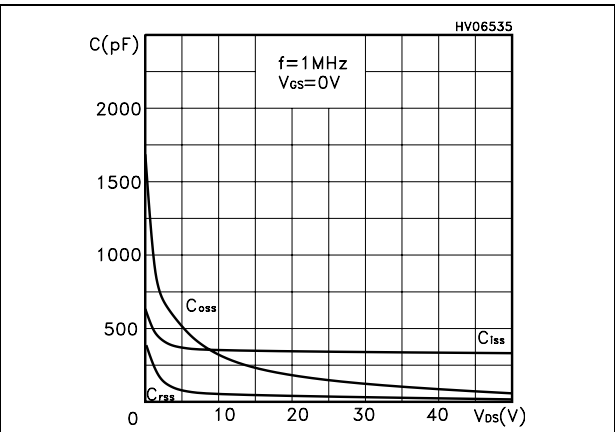


Figure 14. Normalized gate threshold voltage vs temperature

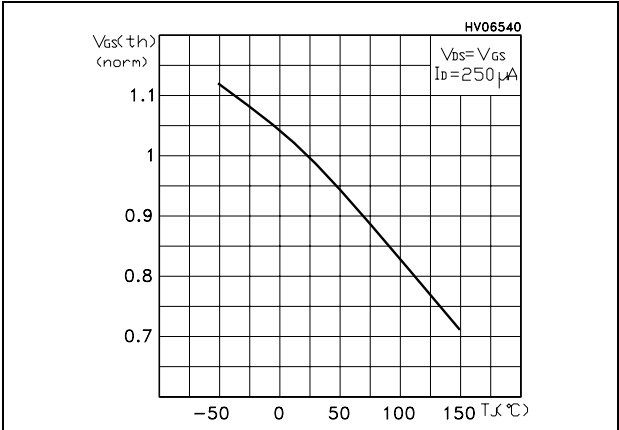


Figure 15. Normalized on resistance vs temperature

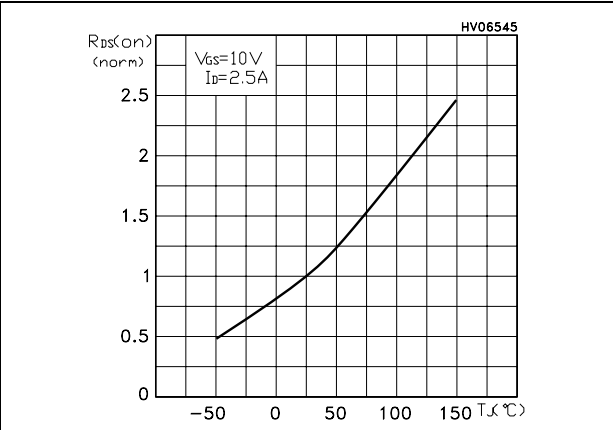
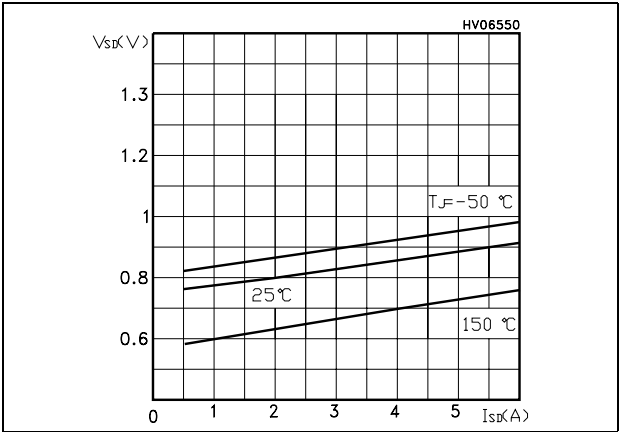


Figure 16. Source-drain diode forward characteristics



3 Test circuit

Figure 17. Switching times test circuit for resistive load

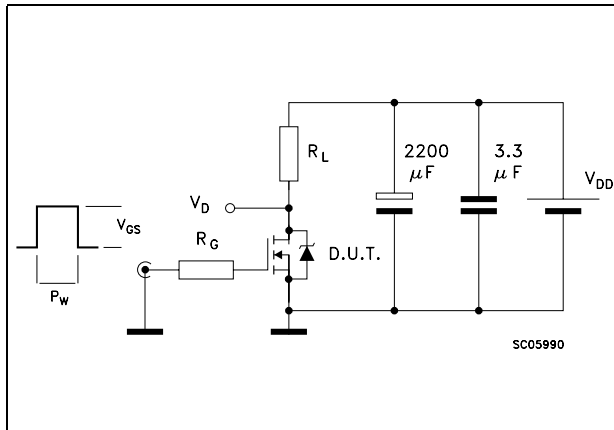


Figure 18. Gate charge test circuit

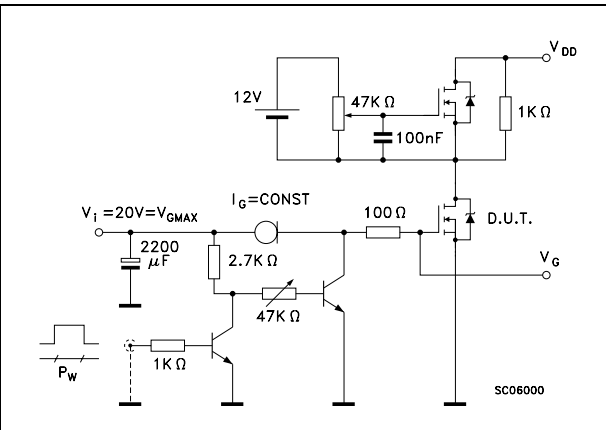


Figure 19. Test circuit for inductive load switching and diode recovery times

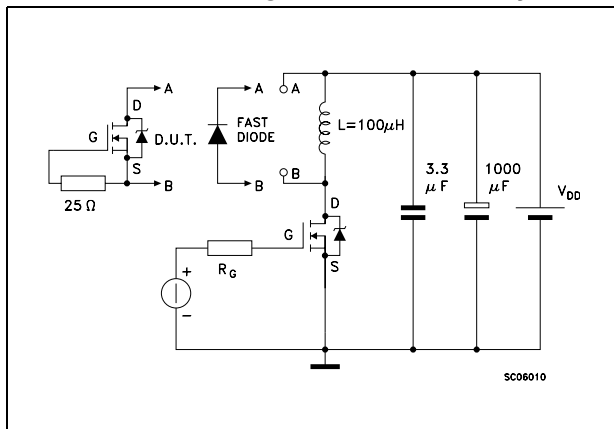


Figure 20. Unclamped inductive load test circuit

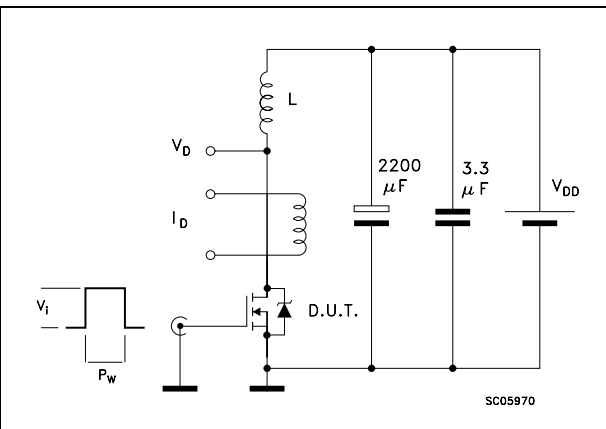


Figure 21. Unclamped inductive waveform

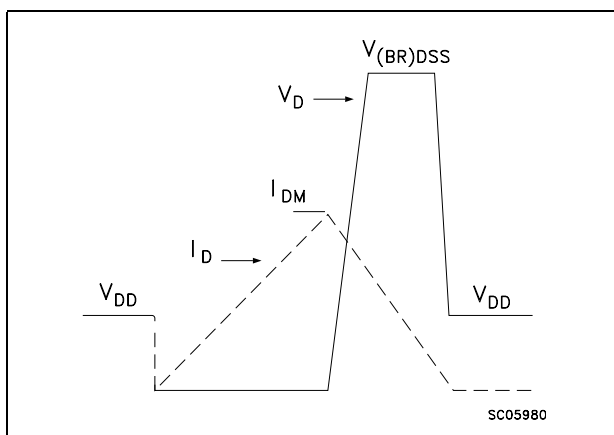
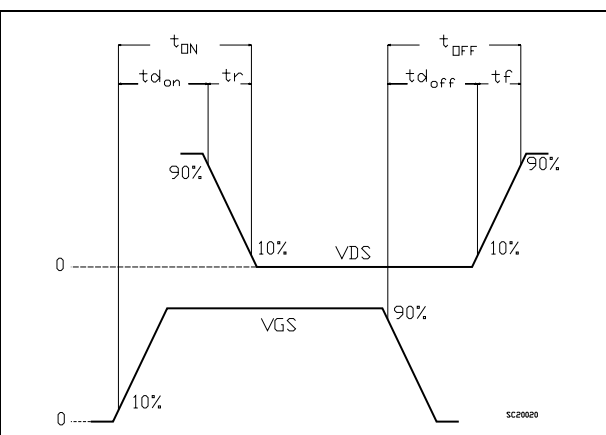


Figure 22. Switching time waveform

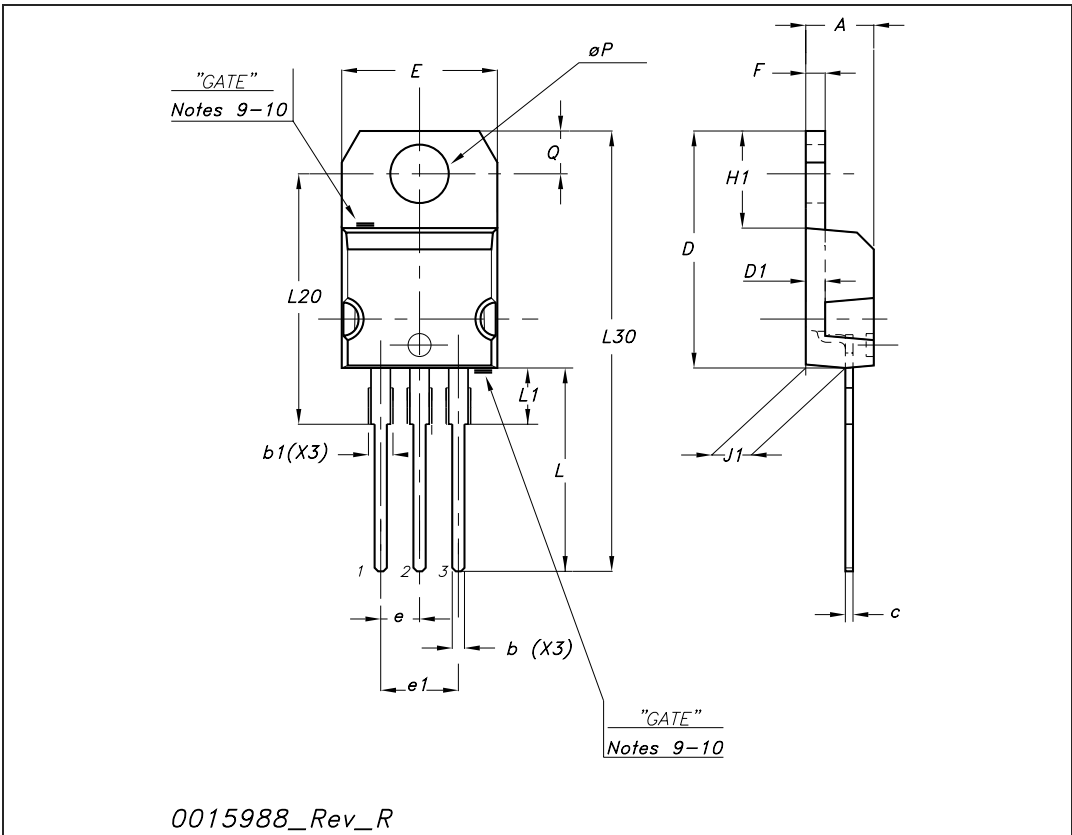


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

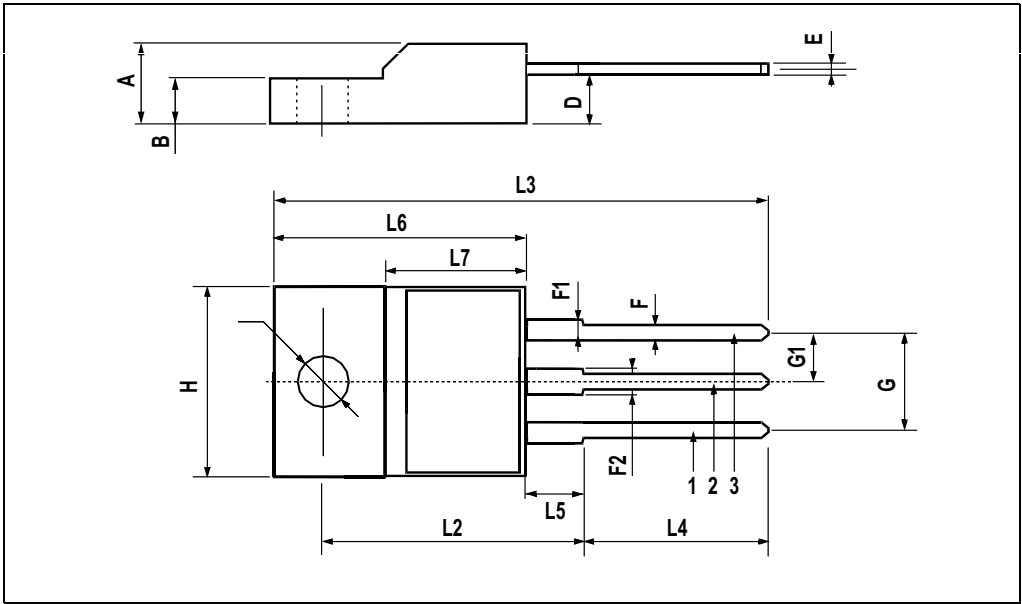
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



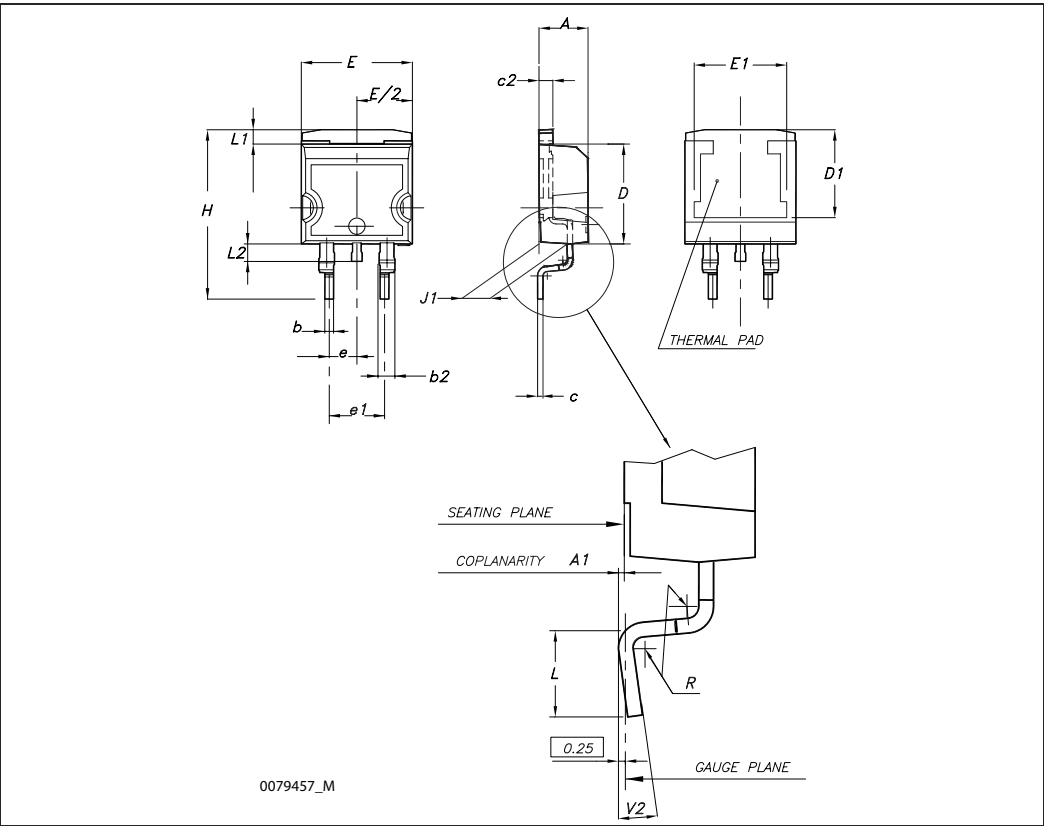
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



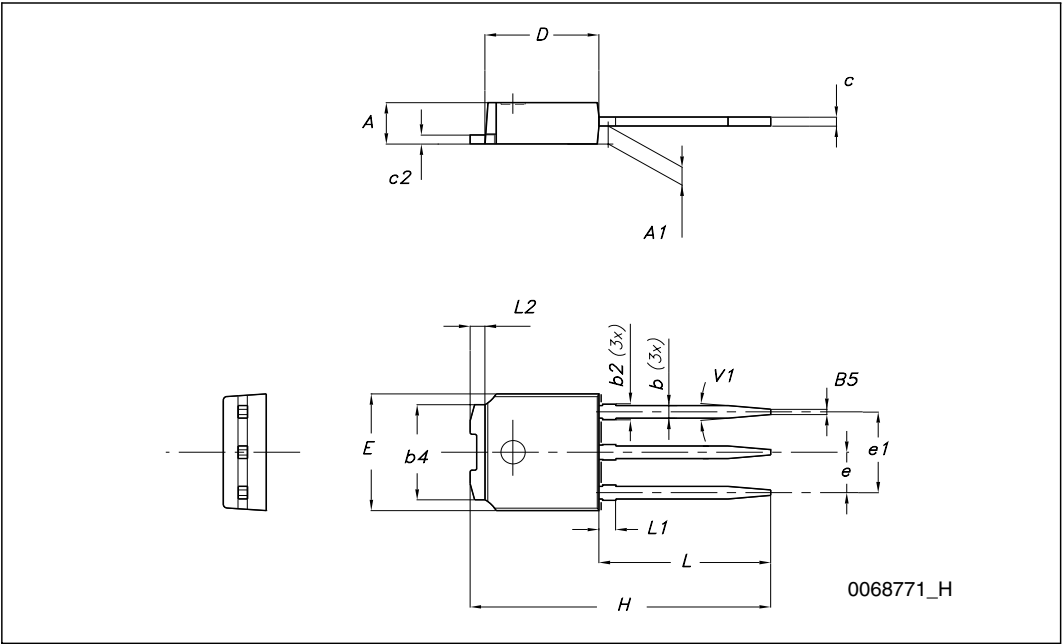
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



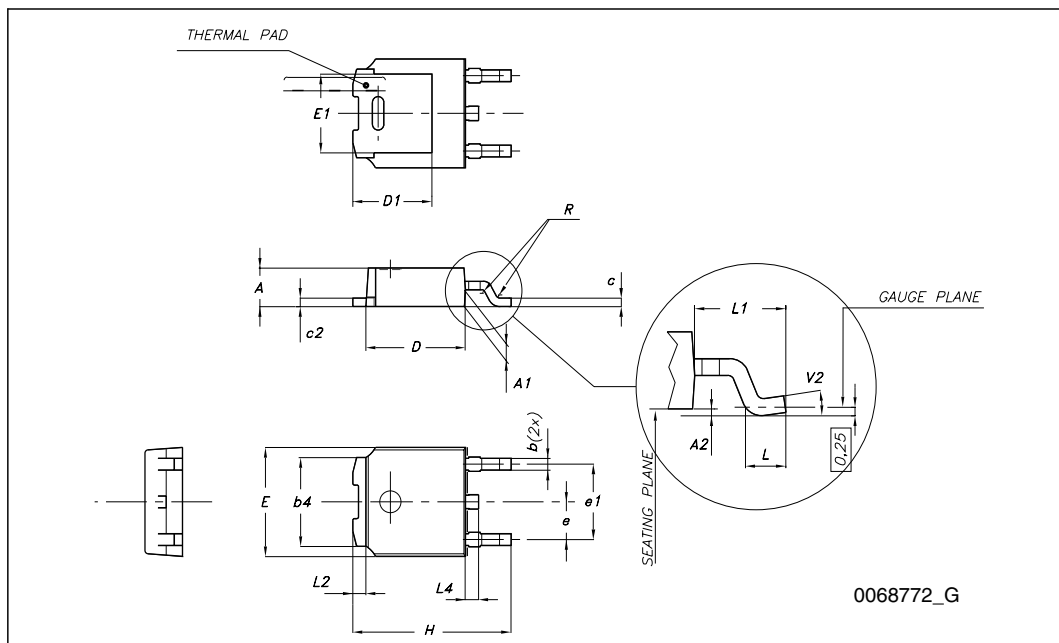
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10°	



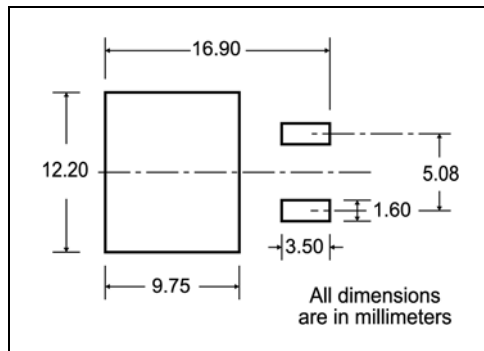
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

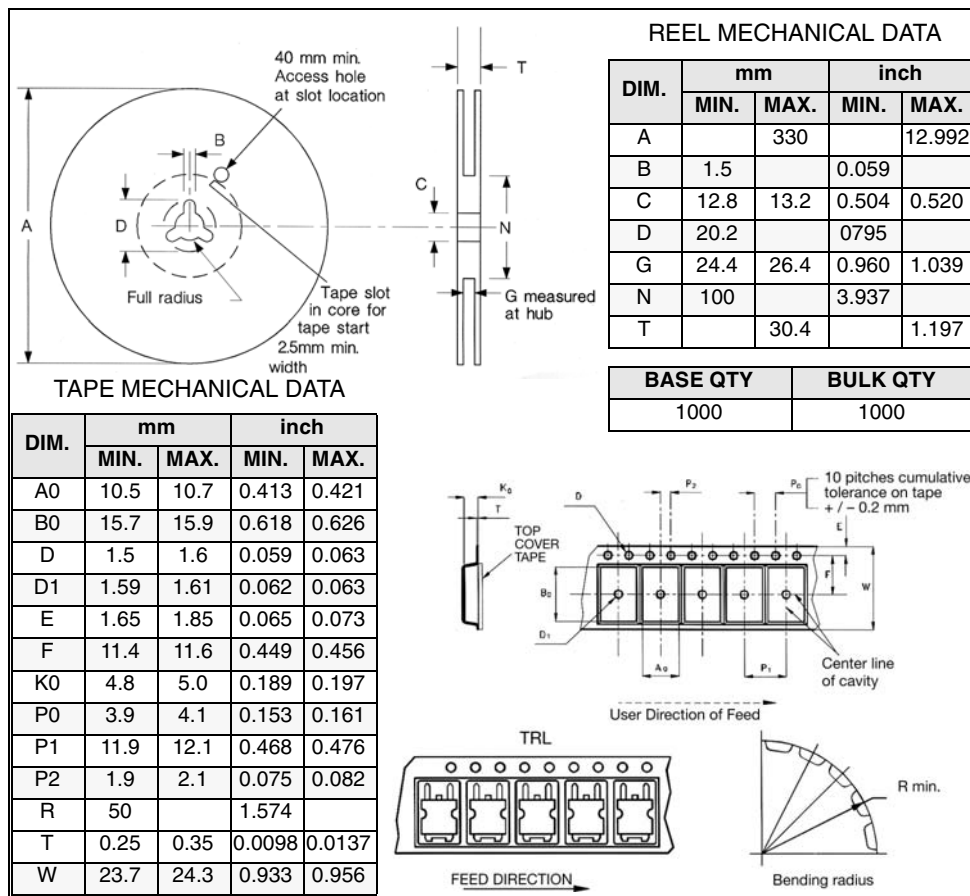


5 Packaging mechanical data

D²PAK FOOTPRINT

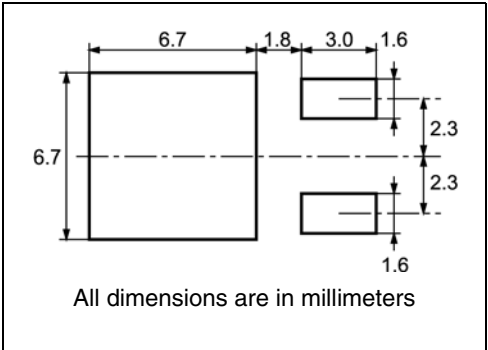


TAPE AND REEL SHIPMENT

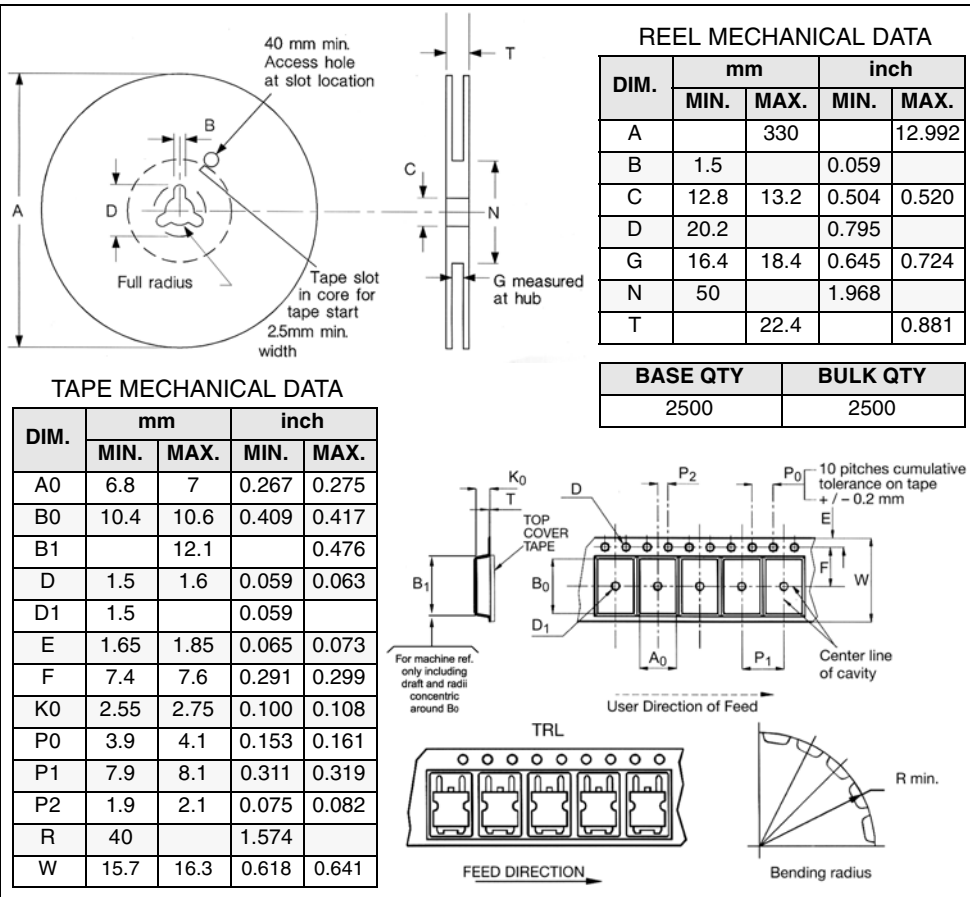


* on sales type

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
14-Apr-2004	11	Title changed
11-Apr-2005	12	Inserted D ² PAK
21-Feb-2006	13	New template
08-Sep-2006	14	Modified order codes
14-Sep-2006	15	Corrected Figure 6.: Safe operating area for DPAK/IPAK
09-Jul-2007	16	Qrr value in Table 7.: Source drain diode has been updated
01-Oct-2008	17	4: Package mechanical data updated

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