偉詮電子股份有限公司
Weltrend Semiconductor, Inc.

WT751002S

PC POWER SUPPLY SUPERVISOR

Data Sheet

REV. 1.00

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GENERAL DESCRIPTION

The WT751002S provides protection circuits, power good output (PGO), fault protection latch (FPOB), and a protection detector function (PSONB) control. It can minimize external components of switching power supply systems in personal computer.

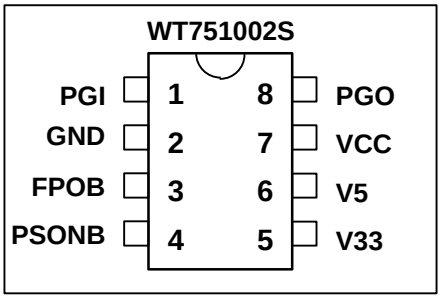
The Over Voltage Detector (OVD) monitors V33, V5 and VCC input voltage level. The Under Voltage Detector (UVD) monitors V33 and V5 input voltage level. When OVD or UVD detect the fault voltage level, the FPOB is latched HIGH and PGO go low. When PGI detect the fault voltage level, the FPOB would be kept LOW and PGO go low. The latch can be reset by PSONB go HIGH. There is 3.5 ms delay time for PSONB turn off FPOB.

When PGI and OVD and UVD detect the right voltage level, the power good output (PGO) will be issue.

FEATURES

- The Over Voltage Detector (OVD) monitors V33, V5 and VCC input voltage.
- The Under Voltage Detector (UVD) monitors V33 and V5 input voltage.
- Both of the power good output (PGO) and fault protection latch (FPOB) are Open Drain Output.
- 75 ms time delay for UVD.
- 300 ms time delay for PGO.
- 38 ms for PSONB input signal De–bounce.
- 73 us for PGI and UVD internal signal De–glitches.
- 55 us for OVD internal signal De–glitches.
- 3.5 ms time delay for PSONB turn-off FPOB.
- The UVD would been disabled when PGI < 0.95V.

PIN ASSIGNMENT AND PACKAGE TYPE



ORDERING INFORMATION

PACKAGE	8–Pin Plastic DIP	8–Pin Plastic SOP	CHIP
	WT751002S–N085	WT751002S–S085	WT751002S-HXXX
Lead–Free（Pb）	WT751002S–N085 Pb	WT751002S–S085 Pb	

※ **The Top-Side Marking would be added a dot（●）in the right side for lead-free package.**

PIN DESCRIPTION

Pin Name	TYPE	Description
PGI	**I**	Power good input signal pin
GND	**P**	Ground
FPOB	**O**	Fault protection output pin, open drain output
PSONB	**I**	On/Off switch input
V33	**I**	3.3V over voltage & under voltage
V5	**I**	5V over voltage & under voltage
VCC	**I**	Power supply
PGO	**O**	Power good output signal pin, open drain output

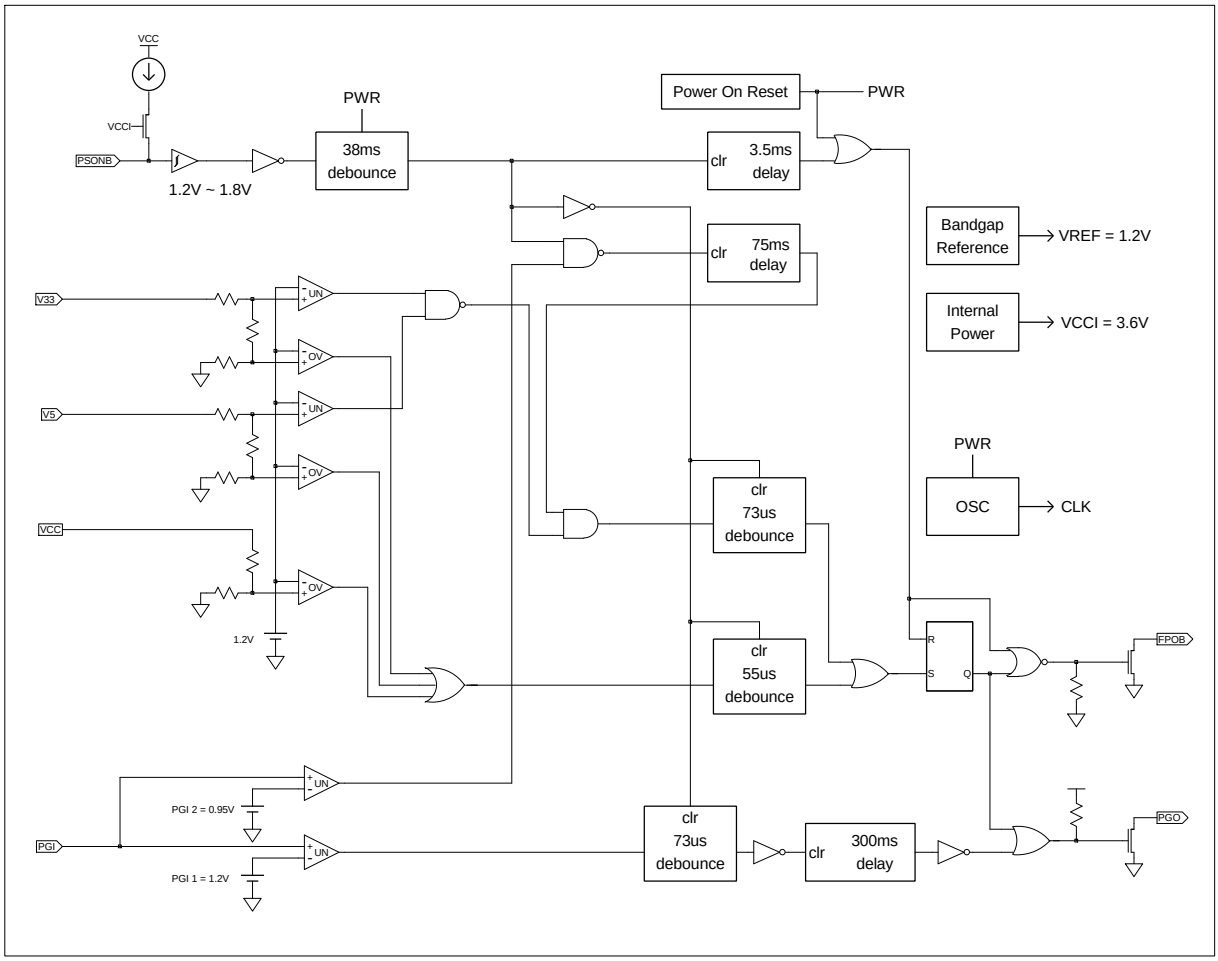
FUNCTION TABLE

PGI	PDON_N	UVD	OVD	FPL_N	PGO
< 0.95V	L	No	No	L	L
< 0.95V	L	No	Yes	H	L
< 0.95V	L	Yes	No	L	L
0.95V < PGI < 1.2V	L	No	No	L	L
0.95V < PGI < 1.2V	L	No	Yes	H	L
0.95V < PGI < 1.2V	L	Yes	No	H	L
PGI > 1.2	L	No	No	L	H
PGI > 1.2	L	No	Yes	H	L
PGI > 1.2	L	Yes	No	H	L
X	H	X	X	H	L

X = don’t care

BLOCK DIAGRAM

WT751002S- 080



ABSOLUTE MAXIMUM RATINGS

Parameter		Min.	Max.	Unit
Supply voltage, VCC		–0.3	16	V
Input voltage	PGI, PSONB, V5, V33	–0.3	VCC + 0.3（Max. 7V）	V
Output voltage	PGO	–0.3	7	V
	FPOB	–0.3	16	V
Operating temperature		-40	125	℃
Storage temperature		-55	150	℃

*Note: Stresses above those listed may cause permanent damage to the devices

RECOMMENDED OPERATING CONDITIONS

Parameter		Conditions	Min.	Typ.	Max.	Unit
Supply voltage, VCC			4	12	15	V
Input voltage	PGI, PSONB, V5, V33				7	V
Output voltage	PGO				7	V
	FPOB				15	V
Output sink current	FPOB	0.3V			10	mA
	PGO	0.3V			10	mA
Supply voltage rising time			1			ms

ELECTRICAL CHARACTERISTICS, at Ta=25°C and V_{CC}=5V.

Over Voltage Detection

Parameter		Condition	Min.	Typ.	Max.	Unit
Over voltage threshold	V33		3.7	3.9	4.1	V
	V5		5.7	6.1	6.2	V
	VCC		12.9	13.4	13.9	V
$I_{LEAKAGE}$ Leakage current (FPOB)		V(FPOB) = 5V		5		uA
V_{OL} Low level output voltage (FPOB)		I_{sink} =10mA			0.3	V

Under Voltage Detection、PGI、PGO

Parameter		Condition	Min.	Typ.	Max.	Unit
Under voltage threshold	V33		2.0	2.2	2.4	V
	V5		3.3	3.5	3.7	V
Input threshold voltage (PGI)		PGI1	1.16	1.20	1.24	V
		PGI2	0.90	0.95	1.00	V
$I_{LEAKAGE}$ Leakage current (PGO)		PGO = 5V		5		uA
V_{OL} Low level output voltage(PGO)		I_{sink} =10mA			0.3	V

PSONB

Parameter	Condition	Min.	Typ.	Max.	Unit
Input pull-up current	PSONB= 0V		150		uA
High-level input voltage		1.8			V
Low-level input voltage				1.2	V

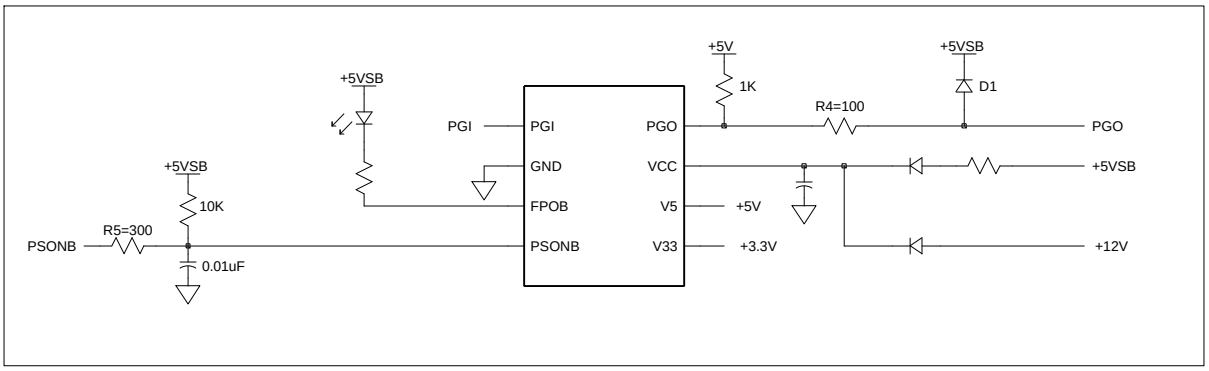
TOTAL DEVICE

Parameter	Condition	Min.	Typ.	Max.	Unit
Icc Supply current	PDON _N= 5V			1	mA
Vcc start-up voltage			3.4		V
Vcc stop voltage after start-up			3.0		V

SWITCHING CHARACTERISTICS, Vcc=5V

Parameter	Condition	Min.	Typ.	Max.	Unit
t_{db1} De-bounce time (PSONB)		24	38	52	mS
t_{delay1} Delay time (PGI to PGO)		200	300	400	mS
t_{db2} De-bounce time (PSONB)		24	38	52	mS
t_{g1} De-glitch time for PGI		47	73	100	uS
t_{g2} De-glitch time for UVD		47	73	100	uS
t_{g3} De-glitch time for OVD		35	55	75	uS
t_{delay2} PSONB to FPOB delay time		t_{db2}+2.0	t_{db2}+3.5	t_{db2}+5.0	mS
t_{delay3} Internal UVD delay time	After FPOB go low or every time PGI > 1.2V	49	75	100	mS

APPLICATION CIRCUIT

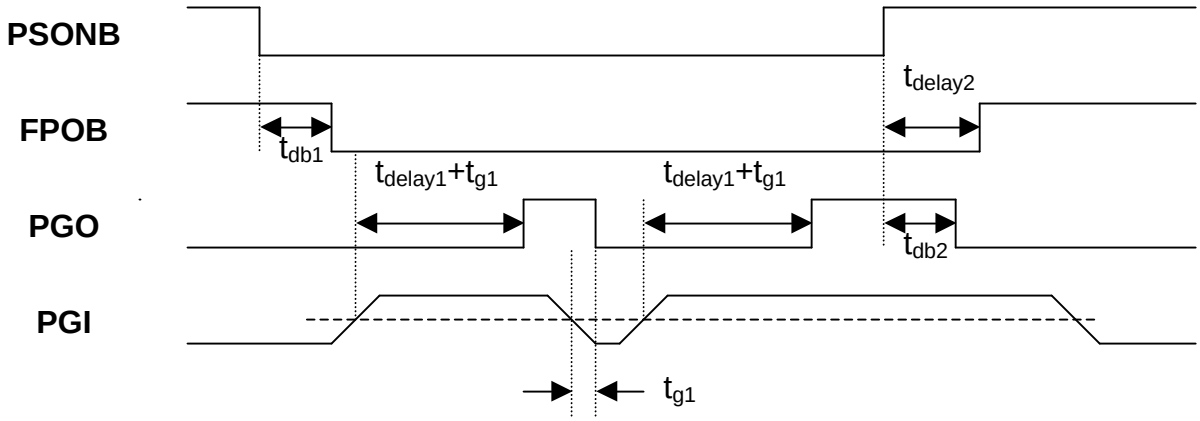


NOTE1：The series resistor R5 at PSONB can not be omitted.（R5 = 300Ω is suggested）

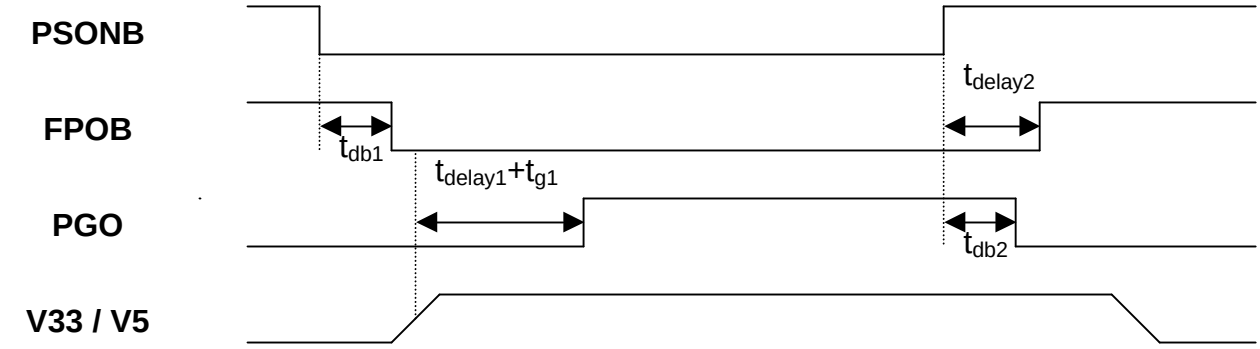
NOTE2：The series resistor R4 = 100Ω and diode D1 at PGO is suggested.

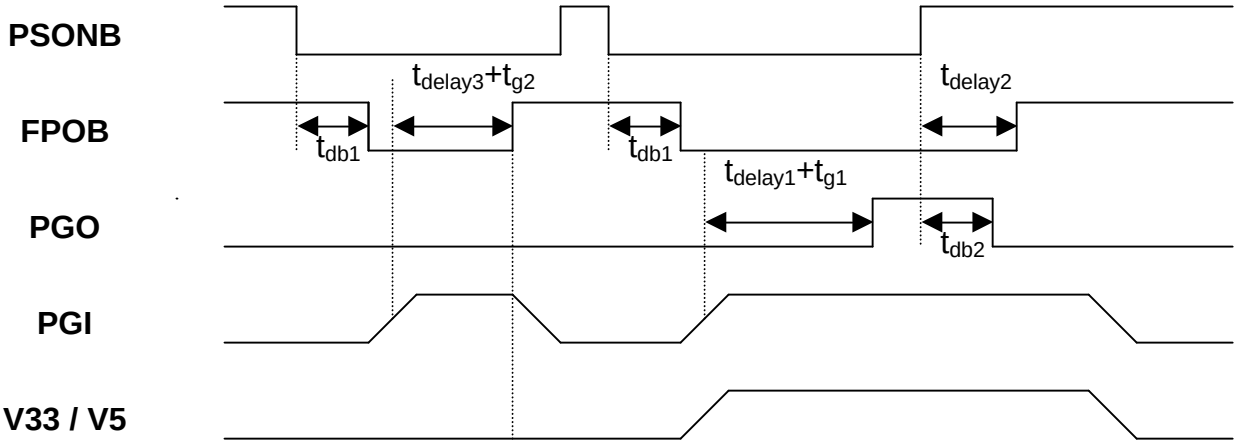
APPLICATION TIMMING

1.) PGI (UNDER_VOLTAGE)：

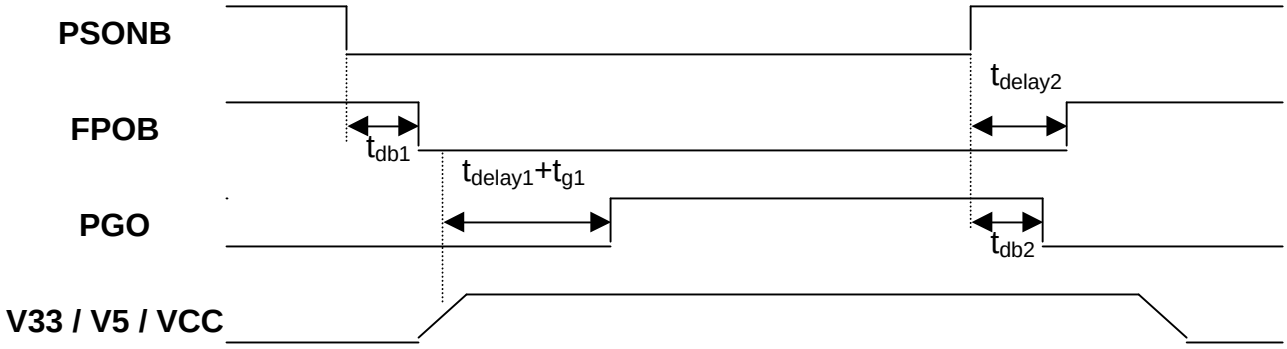


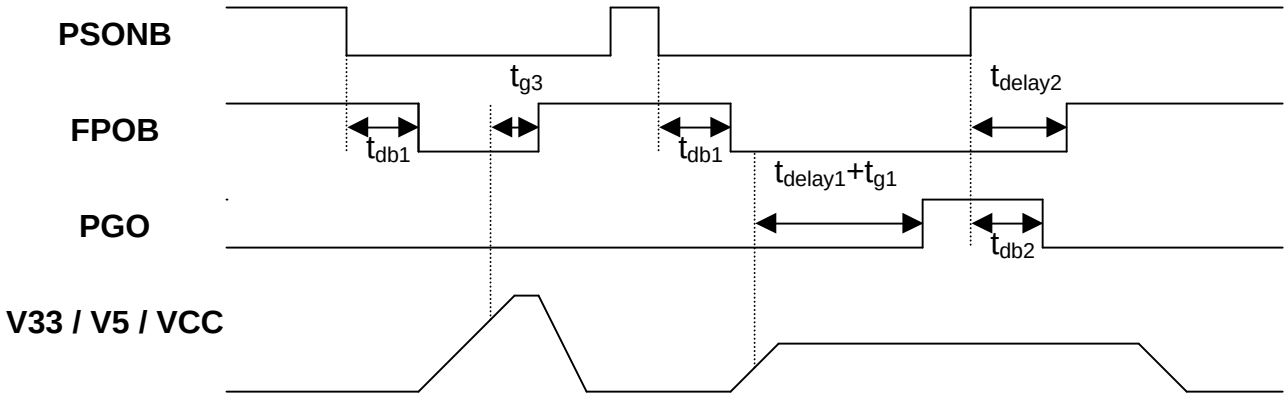
2.) V33 / V5 UVD：


PSONB
FPOB
PGO
V33 / V5
t_{delay2}
t_{db1}
$t_{delay1}+t_{g1}$
t_{db2}


PSONB
FPOB
PGO
PGI
V33 / V5
$t_{delay3}+t_{g2}$
t_{delay2}
t_{db1}
t_{db1}
$t_{delay1}+t_{g1}$
t_{db2}

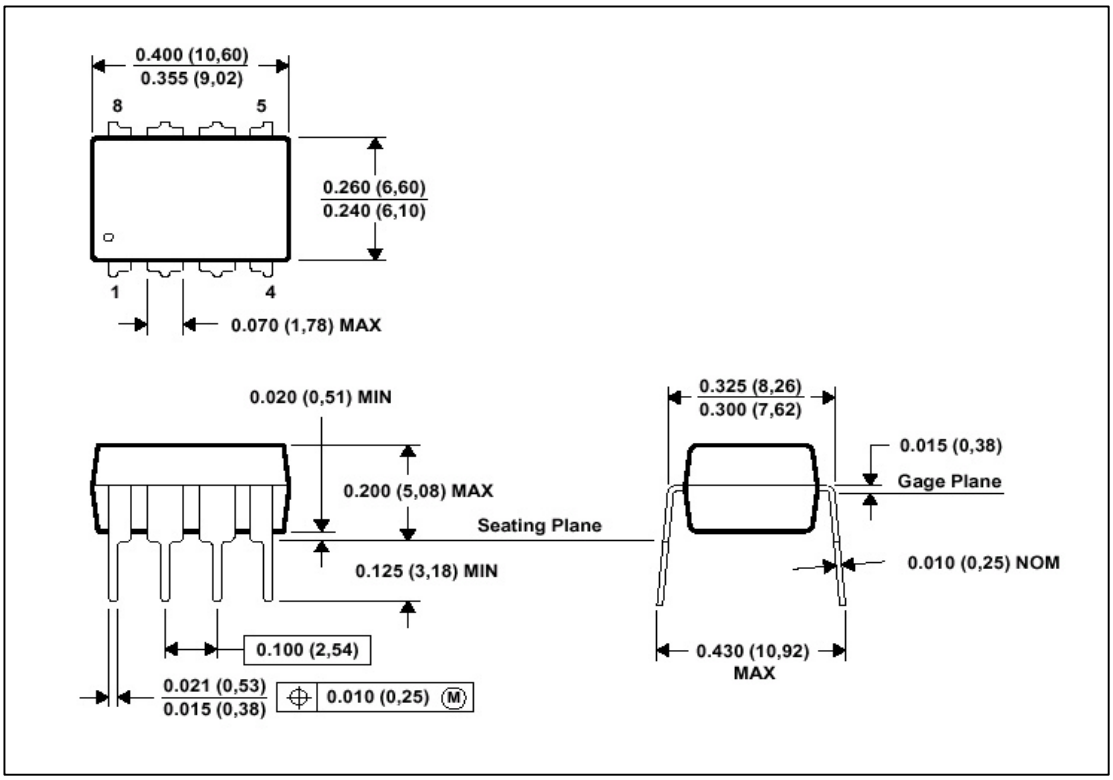
3.) V33 / V5 / VCC OVP：





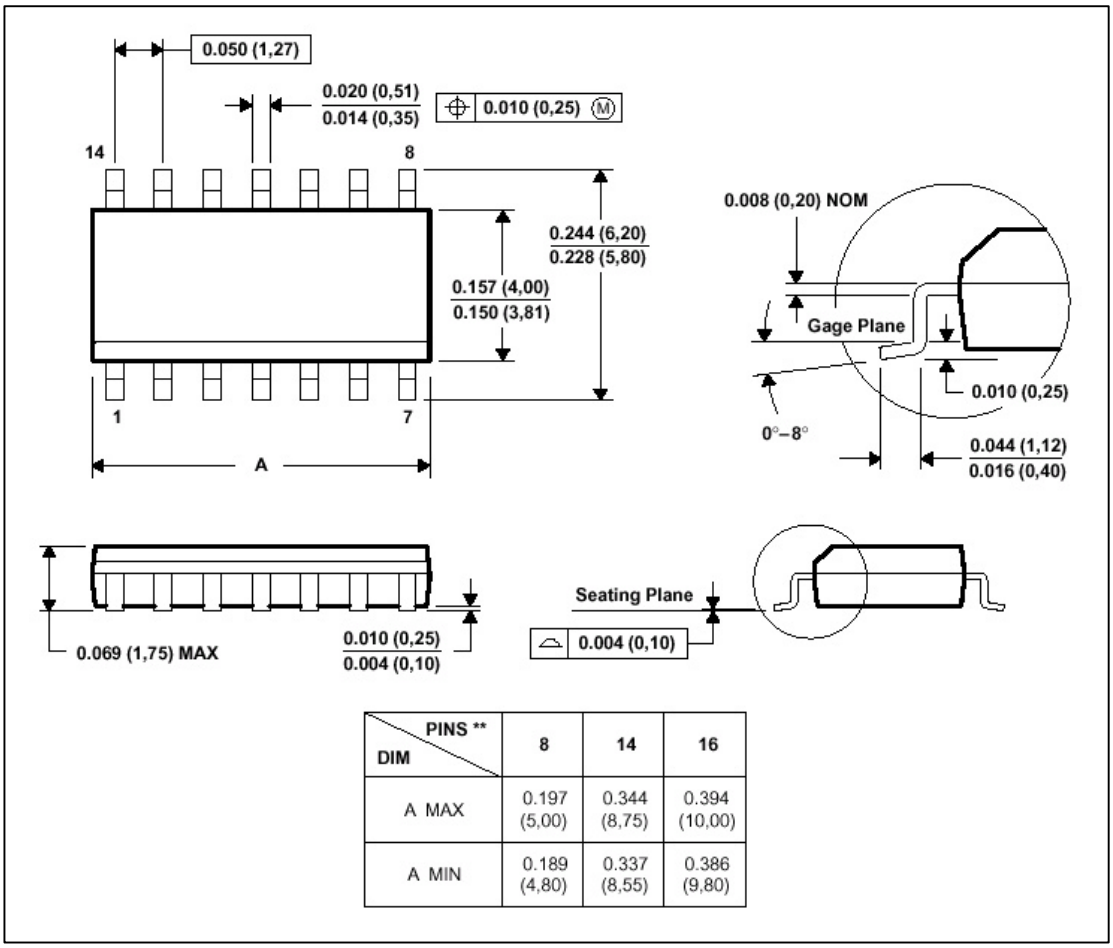
MECHANICAL INFORMATION

PLASTIC DUAL–IN–LINE 8PIN PACKAGE



NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–001

PLASTIC SMALL–OUTLINE 8PIN PACKAGE



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

NOTE 1：All linear dimensions are in inches（millimeters）.
NOTE 2：This drawing is subject to change without notice.
NOTE 3：Falls within JEDEC MS–012