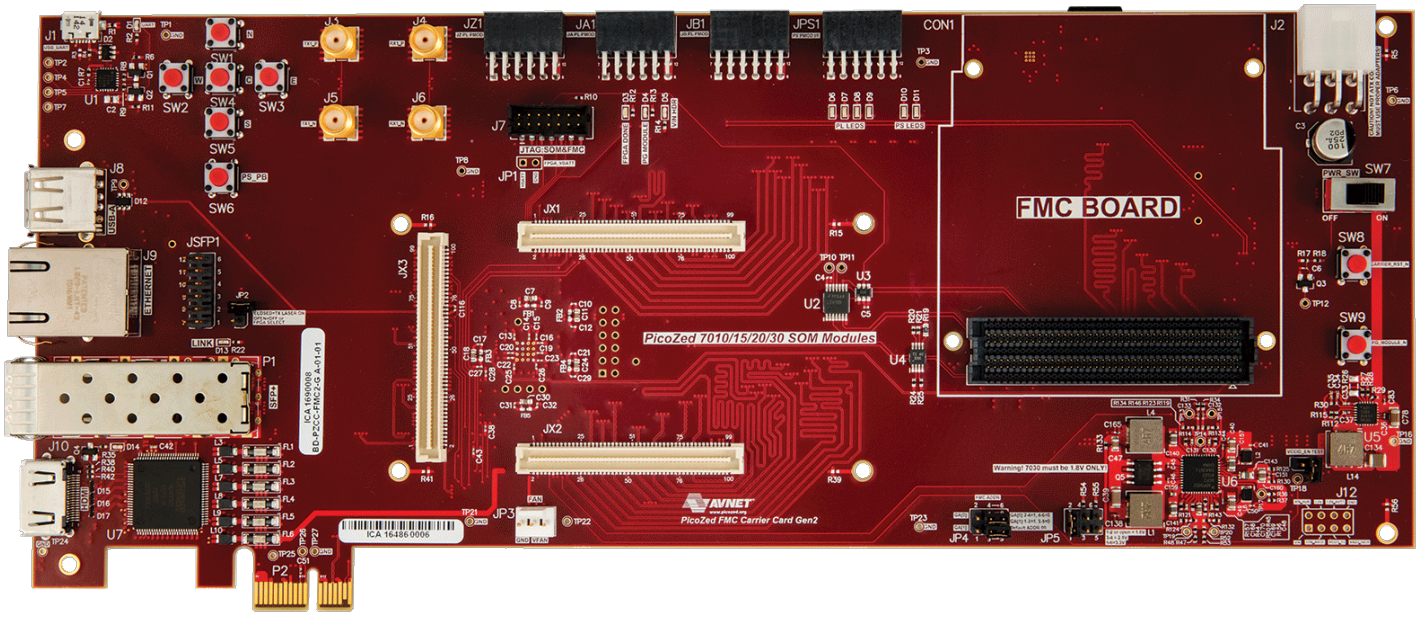
PicoZed FMC Carrier Card V2

PZCC-FMC-V2, Revision 1.1

Hardware User Guide

Version 1.1



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1 Introduction

The PicoZed FMC Carrier Card Version 2 (PZCC-FMC-V2) is a development board designed for customers to easily evaluate the Avnet PicoZed System On Module (SOM) boards. This board provides an I/O breakout platform for the PicoZed SOMs. The PZCC-FMC-V2 provides all necessary SOM power, reset control and SoC I/O pin accessibility through the JX1, JX2, and JX3 MicroHeaders.

This document details the specific features, operation and configuration of the PZCC-FMC-V2 board.

Please visit http://picozed.org/product/picozed-fmc-carrier-card-v2 for the latest product information.

1.1 Glossary

Term	Definition
MIO	Multiplexed Input Output – the dedicated I/O available on the PS
PL	Programmable Logic
POR	Power On Reset
PS	Processing System
SMPS	Switch Mode Power Supply
SOM	System On Module
SoC	System On Chip – Xilinx Zynq®-7000
Pmod	Peripheral Module
FMC	FPGA Mezzanine Card
LPC	Low Pin Count

Table 1 – Glossary of Acronyms

1.2 Additional Documentation

Specific Zynq pin connections are not called out in this document. These are available in either the ***PicoZed FMC Carrier Card V2 Pinout Tables*** or ***Programmable Logic Master User Constraints*** available on the PicoZed FMC Carrier Card V2 documentation page:
http://picozed.org/support/documentation/13076

Avnet PicoZed products information:
Additional information and documentation on Avnet's PicoZed product line can be found at www.picozed.org.

Xilinx Zynq information:
Additional information and documentation on Xilinx's Zynq®-7000 All Programmable SoCs can be found at www.xilinx.com/zynq.

1.3 PZCC-FMC-V2 Features:

- **Interfaces:**
  - FMC LPC (72 differential, 3 single ended)
  - JTAG
    - Single JTAG connector allows accesses to the Zynq and the FMC board through automatic switching circuit.
  - 4 Digilent Pmod™ compatible interfaces:
    - JPS1 connected to PS MIO
    - JA & JB connected to Bank 13 PL (7Z015/20/30 only)
    - JZ connected to Bank 13 PL (7Z015/30 only)
  - Micro SD Card slot
  - Three 100-pin JX MicroHeaders for SOM insertion
  - SFP+ Interface (7Z015/30 only) – control signals connected to JSFP1 to JZ1 PMOD using a jumper cable.
  - HDMI 1080p Output
  - PCIe x 1 Gen 2 Interface pairs
  - SMA connector pairs:
    - SMA-TX P/N
    - SMA-RX P/N
  - 10/100/1000 Mb RJ45 Ethernet connector (connected to PicoZed SOM PHY)
  - Transceivers for 7015/30:
    - SFP+ Interface
    - PCIe x1 Gen 2
    - SMA
    - FMC LPC
  - I2C SW programmable clock synthesizer with I2C configuration EEPROM.
  - I2C Synthesizer Test Header spaced at 0.100”.
  - USB UART - Micro USB connector & transceiver.
  - USB 2.0 OTG – USB Type A connector on the faceplate.
  - MAC ID I2C EEPROM
  - MAC ID UNI/O single wire EEPROM (SFP+ MAC ID – 7015/30 SOM only).
  - I2C Real Time Clock (RTC)
  - CR1025 Battery holder for RTC
  - 1 PS User Push Button
  - 5 PL User Push Buttons
  - 2 Configuration Push Buttons (CARRIER_RST_N, PG_MODULE_N)
  - 4 PL Red User LEDs
  - 2 PS Red User LEDs
  - 3 Status LEDs (VIN_HDR, FPGA DONE & PG_MODULE)
  - 1 100 mil header for FPGA_VBAT_TEST
  - 1 Voltage Monitor pads spaced at 0.100”
  - 1 VADJ User Selectable Header: 1.8V, 2.5V, 3.3V selection; defaults to 1.8V
  - 1 slide switch for main power

- **Power**
  - On Board
    - ADP2384 single channel SMPS IC:
      - Generates the primary board 5V power supply.
        - 5V @ 4 Amp capable.
    - ADP5052 five channel SMPS IC:
      - VADJ: 1.8V, 2.5V, 3.3V up to 4A (user selectable voltage)
      - 3.3V & VCCO_13 up to 4.0A
      - 1.0V_AVCC up to 1.2 A
      - 1.2V_AVTT up to 1.2 A
      - 1.8V LDO@ 200mA
  - Wall Adapter
    - Primary 12V ≥ 5.0A, 2x3 connector
      - NOTE: not an ATX compatible power supply.

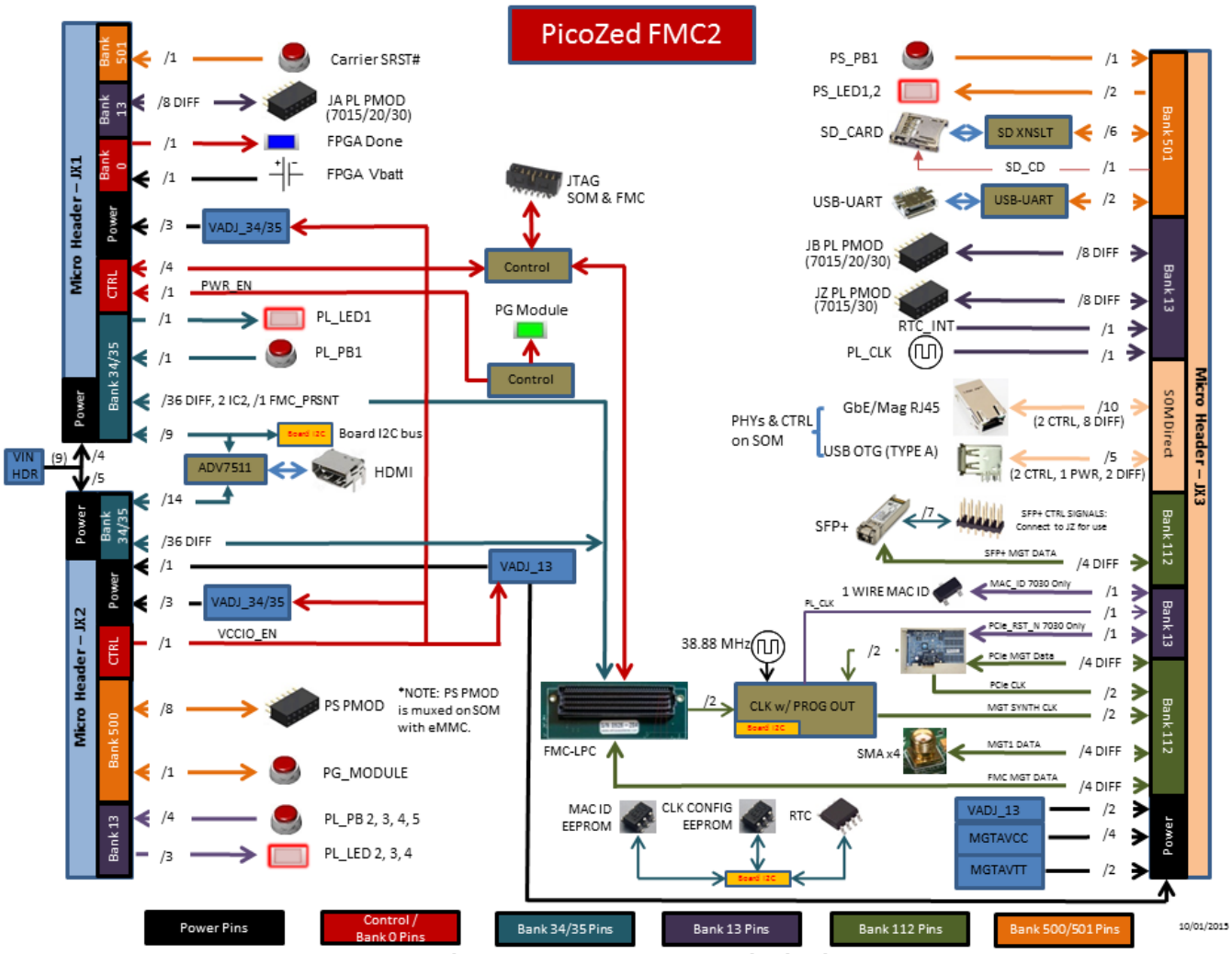

Figure 1 – PZCC-FMC-V2 Block Diagram

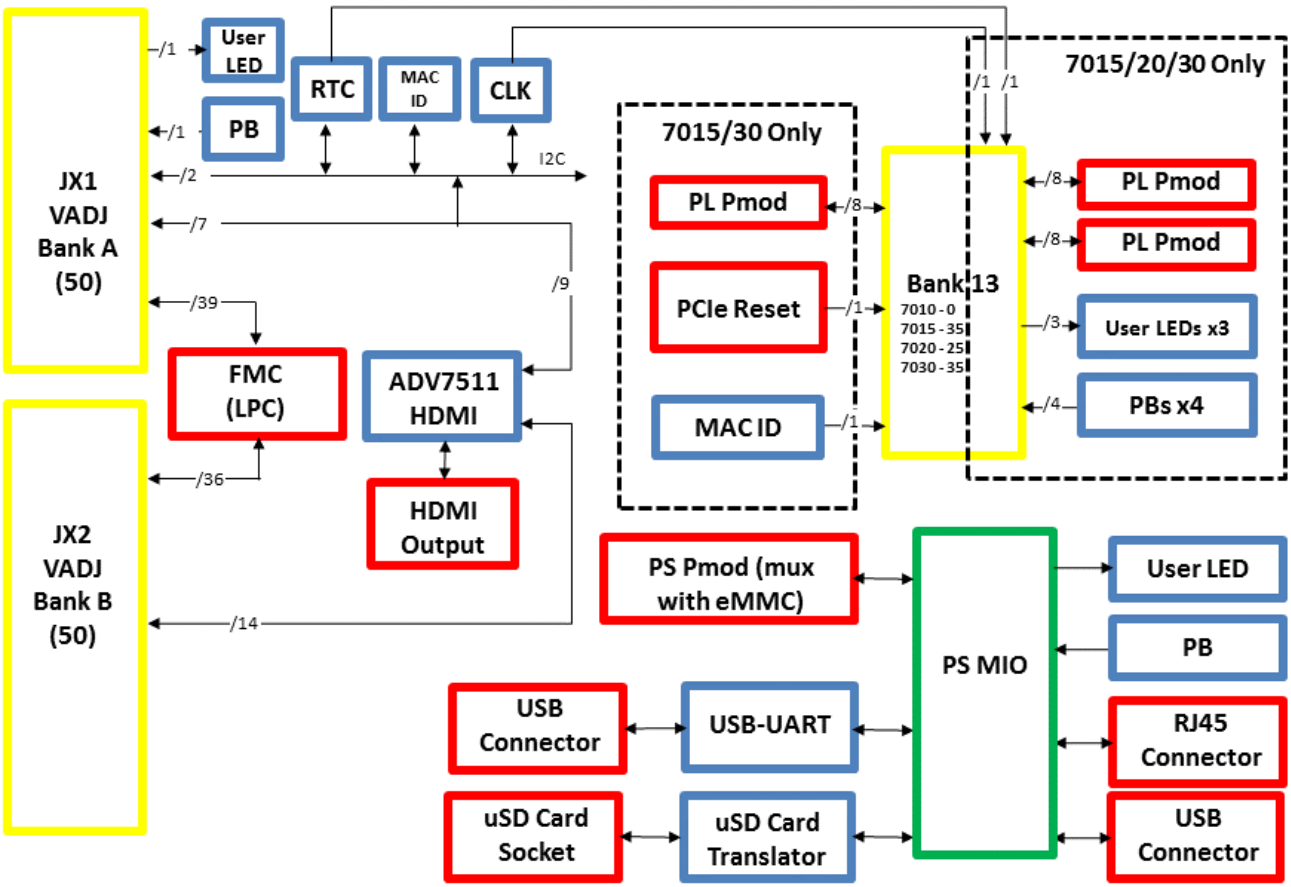

Figure 2 – PZCC-FMC-V2 Functional Block Diagram

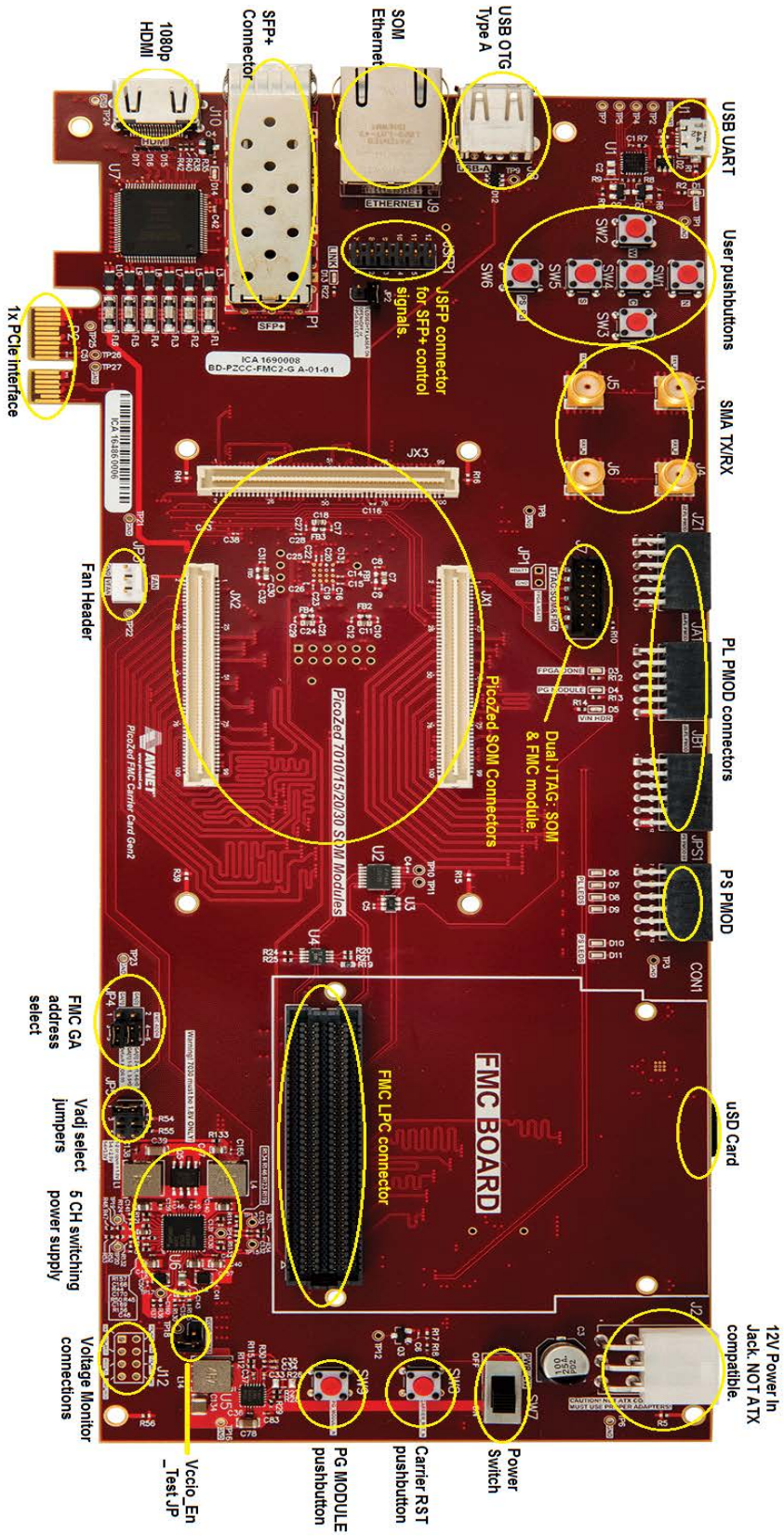

Figure 3 – PZCC-FMC-V2 Component Overview

2 Functional Description

The PZCC-FMC-V2 Carrier is an expansion board for the PicoZed SOMs. The primary I/O interface is via the LPC FMC connector. The board features additional MGT lanes for PCIe and SFP+. The PZCC-FMC-V2 bridges Avnet's PicoZed SOM products to common high speed interfaces.

In addition to the LPC FMC connector, the PZCC-FMC-V2 also has 4 Digilent Pmod™ compatible interfaces, a SFP+ connector, a Micro SD card, Dual function JTAG port (FMC & SOM), an HDMI port, 2 USB ports (UART and OTG TYPE A 2.0), PCIe x1 Gen 2.0 edge connector and a SOM driven Ethernet port.

The board includes user adjustable operational features to aid in product design and development. Such features include software configurable MGT clock synthesizer SMA MGT (TX/RX) data inputs and a user adjustable VADJ power plane.

The board's HDMIO I2C bus, nets labeled: HDMIO_SCL/SDA is the board's primary I2C bus and can be considered the "board I2C bus". More information can be found in section: 2.3.

2.1 Reset sources

2.1.1 System Power Reset: PG_MODULE_N - SW9

The PG_MODULE signal is an active high 2.75V signal. When high, it indicates both the carrier and SOM power supplies are within their regulation tolerance parameters and functional. The signal is held low until the power supplies have completed their successful sequencing routine. Green LED D4 illuminates when this signal is high.

The user can force this pin low by depressing SW9, which will trigger a reboot of the Zynq device. Depressing this button will not cause a hard power cycle, however the PS and PL on the Zynq device will be reset to power on default settings and the selected boot process is initiated based on the boot configuration setting of the SOM.

SOM Net Name:	Carrier Net Name:	JX2 Pin #:
PG_MODULE	PG_MODULE	11

Table 2 – PG_MODULE Connection

2.1.2 Processor Subsystem Reset: CARRIER_SRST_N - SW8

The SYS_RST# button provides an active low signal to net CARRIER_SRST_N which allows the user to reset all of the PL logic on the SOM FPGA without disturbing the debug environment. For example, the previous breakpoints set by the user remain valid after system reset. Due to security concerns, system reset erases all memory content within the PS, including the OCM. The PL is also reset in system reset. Upon de-assertion of this signal, the SoC does not re-sample the boot mode strapping pins.

SOM Net Name:	Carrier Net Name:	JX1 Pin #:
CARRIER_SRST_N	CARRIER_SRST_N	6

Table 3 – CARRIER_SRST_N Connection

2.2 User I/O – Switches and LEDs

2.2.1 User Push Buttons: SW1 – SW6: 7015/20/30 SOM

When a 7015/20/30 SOM is plugged in, the carrier provides 5 PL and 1 PS user GPIO push buttons for the Zynq-7000 AP SoC (blue and green in the table below). When a 7010 SOM is attached, only two switches are available - SW1 (PL_PB1) and SW6 (PS_PB1). These are highlighted in the table as green.

Each signal has a pull down resistor and noise decoupling capacitor to help reduce switch bounce. When depressed the button provides a logic high on the respective net. The switches are placed in a North, South, East, West and Center position. This is to allow the customer to better distinguish which button to press.

Below figure shows the locations of the user switches and the associated labeling. These switches are located in the upper left corner of the PZCC-FMC-V2 board.

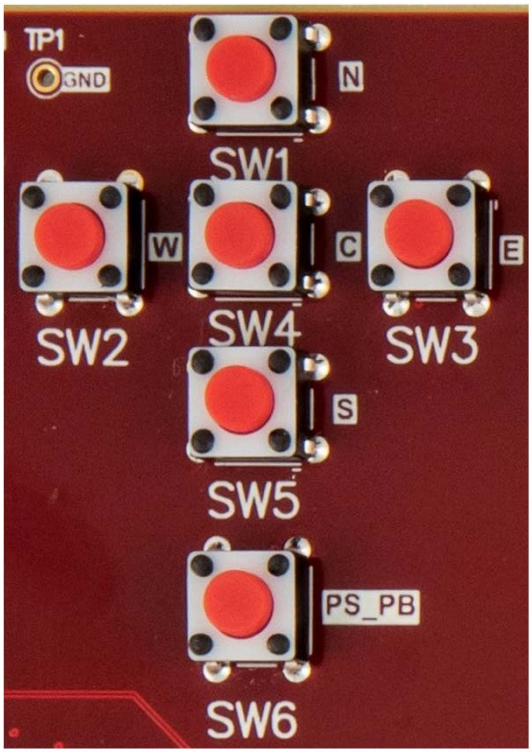

Figure 4 – Push Button Orientation

MIO Number	Carrier Net Name:	Switch Name:	JX MicroHeader Connection:
N/A	PL_PB1	SW1, North	JX1.19
N/A	PL_PB2	SW5, South	JX2.100
N/A	PL_PB3	SW3, East	JX2.95
N/A	PL_PB4	SW2, West	JX2.94
N/A	PL_PB5	SW4, Center	JX2.96
MIO51	PS_PB1	PS_PB	JX3.64

Table 4 – Push Button Connections

2.2.2 User LEDs

The Carrier has 6 SOM driven user LEDs – 4 PL and 2 PS. LEDs listed in green are available to the 7010 SOM. All LEDs (highlighted green and blue) are available to all other SOMs. A logic high from the Zynq-7000 AP SoC I/O turns the LED on. LED's are sourced from the PZCC-FMC-V2's 3.3V rail.

MIO Number	Carrier Net Name:	JX MicroHeader Connection:
N/A	PL_LED1	JX1.17
N/A	PL_LED2	JX2.97
N/A	PL_LED3	JX2.99
N/A	PL_LED4	JX2.93
MIO47	PS_LED1	JX3.40
MIO50	PS_LED2	JX3.66

Table 5 – User LED Connections

2.3 I2C Address space and registers

The FMC-V2 carrier's "board I2C" bus is the board's HDMIO I2C bus. The net names on this bus are HDMIO_SCL and HDMIO_SDA. This bus accesses the following devices at the following I2C addresses:

IDT Config EEPROM Slave Address (EEPROM): 0xA0

| 1 | 0 | 1 | 0 | A2 | A1 | 0 | R/W |

MAC ID Slave Address (EEPROM): 0xA2

| 1 | 0 | 1 | 0 | A2 | A1 | 1 | R/W |

RTC Slave Address: 0xD0

| 1 | 1 | 0 | 1 | 0 | 0 | 0 | R/W |

HDMI Slave Addresses:

0x72 (Main Map slave address)

| 0 | 1 | 1 | 1 | 0 | 0 | 1 | R/W |

0x70 (Packet Memory Map slave address controlled by Main Map Register 0x45)

| 0 | 1 | 1 | 1 | 0 | 0 | 0 | R/W |

0x78 (CEC Map slave address controlled by Main Map Register 0xE1)

| 0 | 1 | 1 | 1 | 1 | 0 | 0 | R/W |

0x7C (Fixed I2C Map slave address controlled by Main Map Register 0xF9)

| 0 | 1 | 1 | 1 | 1 | 0 | 1 | R/W |

0x7E (CEC Map slave address controlled by Main Map Register 0xE1)

| 0 | 1 | 1 | 1 | 1 | 1 | 0 | R/W |

IDT-242 Slave Address:

0xF8 (Default OTP setting when using -006 IDT factory load)

| 1 | 1 | 1 | 1 | 1 | 0 | 0 | R/W |

0xD8 (When configured with Avnet factory default EEPROM config)

| 1 | 1 | 0 | 1 | 1 | 0 | 0 | R/W |

2.4 Clocks

2.4.1 Clock synthesizer IC - U13

IDT-242 I2C ADDR: 0xD8

The FMC2 contains an IDT 8T49N242-006 I2C programmable clock synthesizer to offer maximum clocking flexibility. Upon power up the part is configured via U14, a 24AA025T EEPROM. A 38.888MHz crystal is used for the synthesizer's input for optimum performance and frequency selection. See the below figure for topology. There is also a non-populated header (J14) available on the board. See section 4.2

The synthesizer is wired to provide 2 outputs – Q3 single ended and Q2 differential. Both Q2 and Q3 outputs are synthesized from one of three clock inputs: 38.888MHz, FMC_GBTCLK, or PCIe_CLK. The choice of how U13 handles the input and output clocks is configured in U14.

1) Channel Q3 output – Single ended output from 1 MHz to 200 MHz on SOM Bank 13 MRCC pin (PL_CLK JX3.73).

2) Channel Q3 INV output: tied to test pad TP31.

3) Channel Q2 output is a differential output derived from either the FMC clock or the PCIe clock and drives the SOMs MGT1 bank. The choice of which clock to use is configured in U14, the configuration EEPROM.

4) The PCIe clock input is routed to the synthesizer and the JX3 connector in a multidrop LVDS (M-LVDS) configuration for optimal performance.

- **Synthesizer base default address: 0xD8**
- Base address adjustable via JT1 and JT2.

For more information on the IDT 8T49N242 IC please refer to the IDT datasheet: www.idt.com/>>8T49N242

Figure 5 – Clock Synthesizer topology

SOM Net Name:	Carrier Net Name:	JX3 Pin:
RSVD_PCIE_REFCLK0_P	MGTREFCLK0_P	1
RSVD_PCIE_REFCLK0_N	MGTREFCLK0_N	3
RSVD_MGTREFCLK1_P	MGTREFCLK1_P	2
RSVD_MGTREFCLK1_N	MGTREFCLK1_N	4
BANK13_LVDS_7_P	PL_CLK	73

Table 6 – Clock synthesizer pin table

2.4.2 I2C Clock Configuration EEPROM – U14

EEPROM I2C ADDR: 0xA0

The clock configuration EEPROM is a Microchip 24AA025T-I/OT and is used to configure U13 when powered up.

- **Base default address: 0xA0**
- Base address adjustable set through JT3 and JT4.
- If desired, the user can change the timing of the synthesizer via IDT's Timing Commander Tool via the on board HDMIO I2C bus or by populating J14 and connecting directly to the HDMIO I2C bus.
- For more information on how to custom program the clock, a reference design and tutorials page can be accessed at the following location: http://picozed.org/support/design/13076/106
- For more information on the Timing Commander tool: (http://www.idt.com/products/clocks-timing/timing-commander-software-download-resource-guide)

2.5 PCIe x1 Gen2 Interface

Note: The PCIe data interface is available when using a PicoZed 7015 or 7030 SOM.

- The PCIe x1 interface is **not** required for normal operation. However, it has been provided to assist in the development of PCIe based SOM products if desired. When inserted into a PCIe slot, 12V power from the host PCIe slot can be used for low power applications (10 Watts or less per the PCIe specification Version 1.1). The PCIe interface includes a 12V power circuit, control signals and a single data lane (differential TX and RX) and one differential PCIe clock.

  For PCIe applications needing more than 10 Watts, use the included ATX-to-6P Mini-Fit adapter. Connect the 6P end of the adapter to J2. Connect the 4-pin ATX connector to the ATX power supply. This will provide supplemental 12V power to the PZCC-FMC-V2.

Figure 6 – ATX-to-6P Mini-Fit Adapter for Supplemental 12V PCIe Power

- The PRSNT signals are used to identify the lane width (x1) of the PCIe bus for the host motherboard. The carrier ties the PRSNT1# and PRSNT2# signals together to accomplish this. The host motherboard has pull-up and pull-down resistors on these signals so the carrier does not require any other special configurations to enumerate as a single lane PCIe device when plugged into a host PC.

- The differential PCIe reference clock (PCIe_REFCLK_P/N) is routed directly to the JX3 header for SOM connectivity.

- The PCI Express transmit lanes are AC coupled (DC blocking capacitors are included in the signal path) on the development board as required by the PCI Express specification.

SOM Net Name:	Carrier Net Name:	JX3 Connection:
PCIE_RX0P	PCIE_RX0P	8
PCIE_RX0N	PCIE_RX0N	10
PCIE_TX0P	PCIE_TX0P	13
PCIE_TX0N	PCIE_TX0N	15
PCIE_REFCLK_P	PCIE_REFCLK_P	1
PCIE_REFCLK_N	PCIE_REFCLK_N	3
PCIE_RST_N	PCIE_RST_N	86

Table 7 – GTP Pin Locations for PCI Express

2.6 FMC LPC Connector

A single Low Pin Count (LPC) FMC connector is implemented on the carrier board to support FMC plug-in modules. The block diagram shows the MicroHeader connections to the FMC LPC connectors. See Figure **7 – FMC Connections** for topology overview.

When and FMC board is plugged in, the FMC_PRSNT_N and FMC_PRSNT_VADJ_N signals are driven low per the FMC specification. The FMC_PRSNT_N signal is used to switch the JTAG signals so the FMC card can be accessed through the JTAG interface. When a FMC card is not present, FMC_PRSNT_N is pulled high via R104 and the JTAG interface is isolated to the SOM only. See section 2.20, JTAG Interface.

The FMC_PRSNT_VADJ_N signal can be used as an indicator to the SOM that an FMC device has been attached. This signal is located per the table below:

SOM Net Name:	Carrier Net Name:	JX3 Pin:
JX1_LVDS_2_N	FMC_PRSNT_VADJ_N	25

Table 8 – CP2104 Connections

There are four mounting holes in the FMC card area to facilitate secure FMC module mounting and match the FMC specification. There are also no components directly under the FMC mounting area on the top side of the board per the FMC specification.

The following guidelines have been observed in the layout of the FMC interface:

- **CLK_#_M2C**
  - 50 ohm single-ended impedance
  - Less than 10mil skew in P/N pair
  - Connected to MRCC (Multi-Region)
  - No length matching to any other feature
- **LA bus**
  - 50 ohm single-ended impedance
  - Less than 10mil skew in P/N pair
  - Less than 100mil length skew across all bits in a bus
  - LA Bus 0:16 located in bank 34 (7010/20), Bank 35 (7015/30).
  - LA Bus 17:33 located in bank 35 (7010/20), Bank 34 (7015/30).
  - CC Pairs 0, 17 on MRCC pins
  - CC Pairs 1, 18 on SRCC pins
- To conserve SoC pins, GA[1:0] pins are connected to header J9 – see **Section 4.1** for address selection.

2.6.1 Layout Routing Guidelines

- The signals for each header follow FMC routing tolerances and guidelines. Each of the P/N pairs have 50Ω single-ended impedance (100Ω differential) with less than 10 mil skew between all P/N pairs on each header.

- There is less than 200 mil length skew across all bits in a bus or byte group, including DQ and DQS pins in each bank.

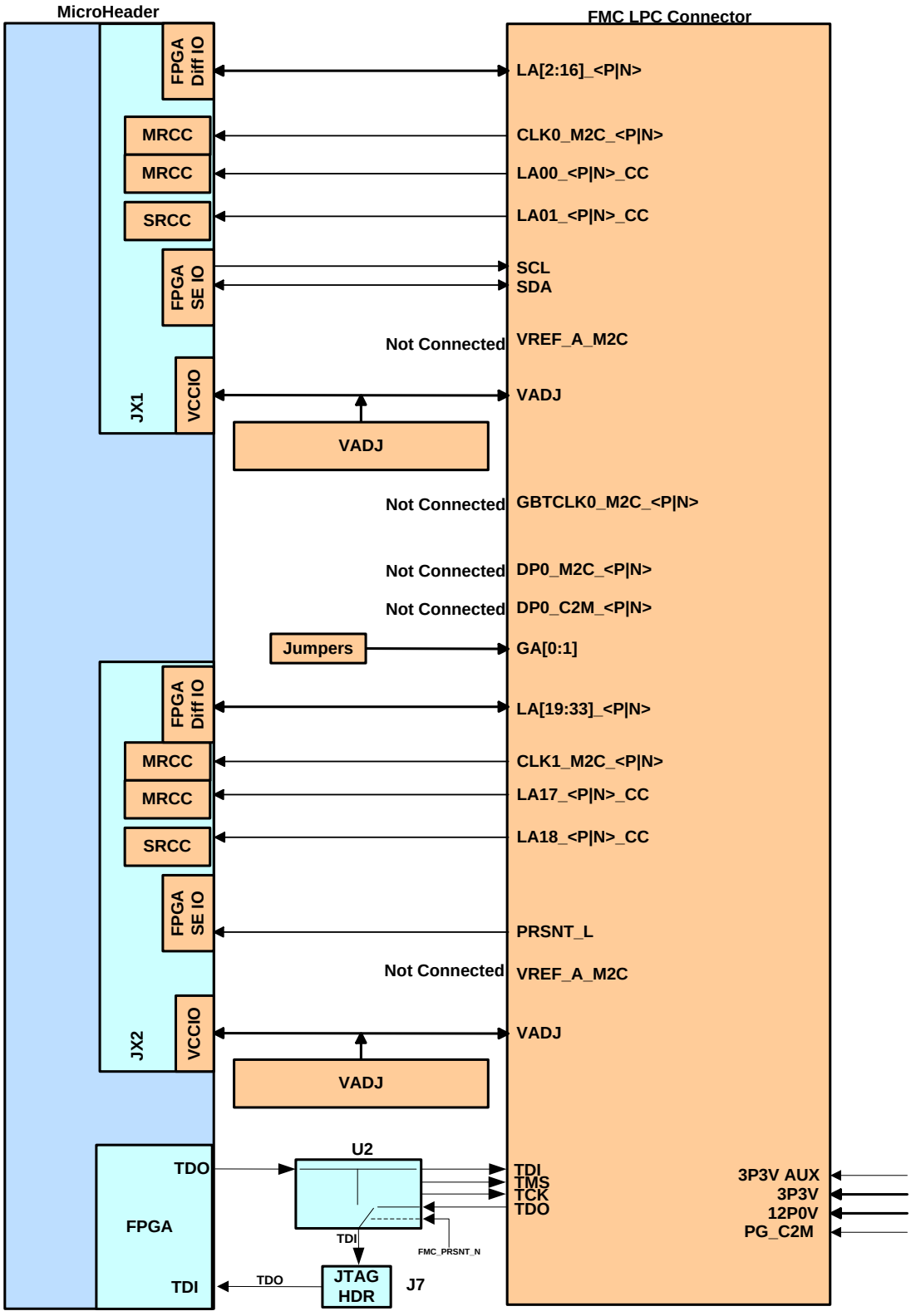

Figure 7 – FMC Connections

Note: The FMC slot SDA, SCL, and FMC_PRSNT signals are 3.3V levels. For this reason, level translation is implemented to follow the VADJ level.

2.7 SFP+ Interface – P1 (7015/30 SOM only)

The SFP+ interface is available to the 7015/30 SOM. The non-transceiver portion of the SFP+ interface is routed out to a vertical 0.1" connector (JSFP1). The SFP+ interface can be used without JSFP1 as long as the SFP+ doesn't require control signals. If the SFP+ does require control signals, a loopback cable must be installed into JSFP1 and attached to the JZ PL PMOD connector. This cable is available from Digilent.
http://store.digilentinc.com/2x6-pin-cable/

- JP2 is used to enable or disable the SFP+ transmit laser. When the jumper is placed, the laser is enabled. When the jumper is removed, the laser is disabled unless a low is written to JSFP1 Pin 2.

- D13 is the LOS (Loss Of Signal) indicator. It is silkscreened as "LINK" on the board. This yellow LED will illuminate when a valid SFP+ link is established and maintained. It will extinguish if there is not a link.

- **NOTE:** The PS_PMOD interface on the PicoZed SOM is, by default, set to eMMC mode. To select between the PS_PMOD interface and the eMMC interface, please see the SOM's User Guide: http://picozed.org/support/documentation/4736

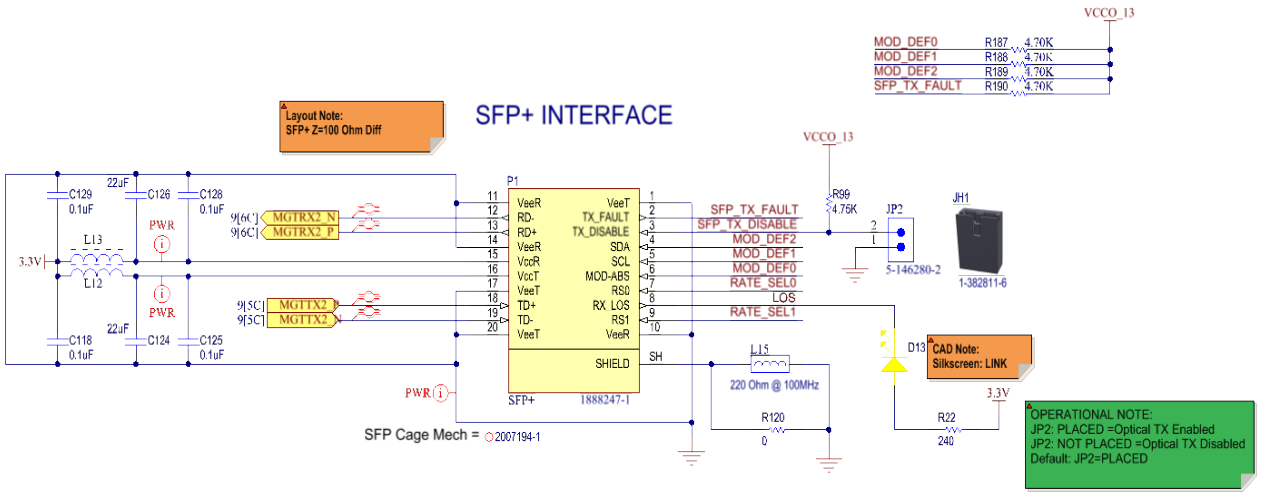

Figure 8 – SFP+ Interface connections

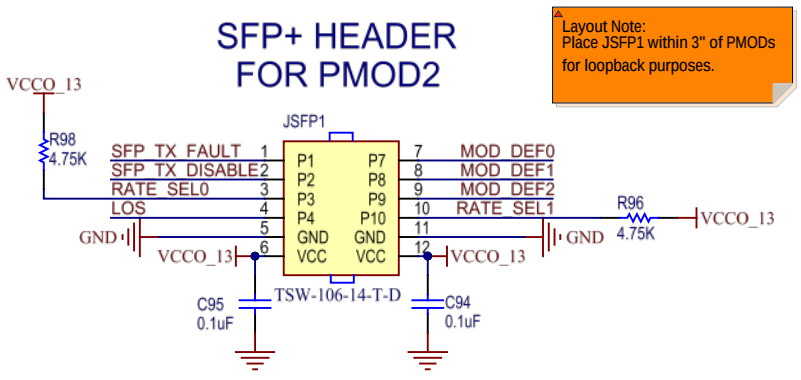

Figure 9 – SFP+ Control connections

2.8 PS/PL PMOD™ Interfaces – JA, JB, JZ & JPS1

The carrier has four Digilent Pmod™ right angle 0.1" female sockets (2x6). Three connectors are for the SoC's PL (JA, JB, JZ) and one for the SoC's PS (JPS1). These connections include eight GPIO. The JA, JB, and JZ PL Pmods are powered via VCCO_13 (3.3V).

- Pmod™ Connections based on board type:
  - PicoZed 7010: JPS1 Pmod only
  - PicoZed 7020: JPS1, JA, JB Pmods
  - PicoZed 7015/30: JPS1, JA, JB, JZ Pmods

- JPS1 - PS Pmod is attached to bank 500 and can be used as a general Pmod interface, Processor (PJTAG) access or other hardened MIO peripherals (SPI, GPIO, CAN, I2C, UART, SD, QSPI, Trace, Watchdog). Note that these Pmod signals are muxed to eMMC on the PicoZed SOM.

- **NOTE:** The PS_PMOD interface on the PicoZed SOM is, by default, disabled as the mux on the SOM is, by default, set to eMMC mode. To select between the PS_PMOD interface and the eMMC interface, please see the SOM's User Guide: http://picozed.org/support/documentation/4736

JA Pmod™	SOM Net Name:	Carrier Net Name:	JX1 Connection:	JA PMOD Pin Number:
JA	BANK13_LVDS_0_P	JA0-1_P	87	1
	BANK13_LVDS_0_N	JA0-1_N	89	2
	BANK13_LVDS_1_P	JA2-3_P	88	3
	BANK13_LVDS_1_N	JA2-3_N	90	4
	BANK13_LVDS_2_P	JA4-5_P	91	7
	BANK13_LVDS_2_N	JA4-5_N	93	8
	BANK13_LVDS_3_P	JA6-7_P	92	9
	BANK13_LVDS_3_N	JA6-7_N	94	10
JB Pmod™	**SOM Net Name:**	**Carrier Net Name:**	**JX3 Connection:**	**JB PMOD Pin Number:**
JB	BANK13_LVDS_8_P	JB0-1_P	74	1
	BANK13_LVDS_8_N	JB0-1_N	76	2
	BANK13_LVDS_9_P	JB2-3_P	79	3
	BANK13_LVDS_9_N	JB2-3_N	81	4
	BANK13_LVDS_10_P	JB4-5_P	80	7
	BANK13_LVDS_10_N	JB4-5_N	82	8
	BANK13_LVDS_11_P	JB6-7_P	85	9
	BANK13_LVDS_11_N	JB6-7_N	87	10
JZ Pmod™	**SOM Net Name:**	**Carrier Net Name:**	**JX3 Connection:**	**JZ PMOD Pin Number:**
JZ	BANK13_LVDS_14_P	JZ0-1_P	92	1
	BANK13_LVDS_14_N	JZ0-1_N	94	2
	BANK13_LVDS_13_P	JZ2-3_P	91	3
	BANK13_LVDS_13_N	JZ2-3_N	93	4
	BANK13_LVDS_16_P	JZ4-5_P	98	7
	BANK13_LVDS_16_N	JZ4-5_N	100	8
	BANK13_LVDS_15_P	JZ6-7_P	97	9
	BANK13_LVDS_15_N	JZ6-7_N	99	10

Table 9 – PL PMOD Pin Assignments

PS Pmod™	SOM Net Name:	Carrier Net Name:	JX2 Connection:	JPS1 PMOD Pin Number:
JPS1	MIO13	PSPMOD_D0	2	1
	MIO10	PSPMOD_D1	1	2
	MIO11	PSPMOD_D2	6	3
	MIO12	PSPMOD_D3	5	4
	MIO0	PSPMOD_D4	7	7
	MIO9	PSPMOD_D5	8	8
	MIO14	PSPMOD_D6	3	9
	MIO15	PSPMOD_D7	4	10

Table 10 – JPS1 PS PMOD Pin Assignments

2.9 JX1, JX2 and JX3 SOM Interface MicroHeaders

The PicoZed Carrier has three 100-pin MicroHeaders (FCI, 61083-101400LF) for connection to the SOM. The stack height is 5mm for each of these connectors.

- The JX1 and JX2 connectors interface power control signals, SOM reset, JTAG, PL (FMC data/control, PB), PS Pmod, Ethernet, and HDMI signals to the SOM target.

- The JX3 connector interfaces SOM Ethernet, PCIe TX/RX/CLKs, microSD Card, 1 Wire MAC ID, RTC interrupt, USB OTG, PL I/O, USB UART, Gigabit transceivers data and clocks (MGT/GTX), and the jumper cabled SFP+ to the JZ PMOD header.

- The connectors are FCI 0.8mm BergStak®, 100 Position, Dual Row, BTB Vertical plugs. These have variable stack heights from 5mm to 16mm, making it easy to connect to a variety of carrier or system boards.

- Each pin can carry 500mA of current. The 5mm stack height is used on the PZCC-FMC-V2, and PicoZed SOMs support I/O speeds up to 8 Gbps as shown in the following FCI customer presentation:

  BergStak® 0.8mm Mezzanine Connectors
  Customer Presentation
  June 2014
  http://portal.fciconnect.com/Comergent/fci/documentation/customerpresentation/bergstak_customerpresentation.pdf

- The fastest supported rate in the PicoZed family exists with the 7030 member, whose Zynq device/package can achieve 6.6 Gbps. This is within the operating rate of the BergStak connectors.

- The carrier card powers the PicoZed PL VCCIO banks. This gives the carrier card the flexibility to control the I/O bank voltages. On the PZCC-FMC-V2, both VCCO_34 and VCCO_35 are powered from a single supply.VCCO_13 is powered from 3.3V.

- One signal in a Bank 34 differential pair (JX1_LVDS_2_P on 7010/20, JX2_LVDS_2_P on 7015/30) is shared with PUDC_B which is pulled down via a 1KΩ resistor to ground.

Table 11 – MicroHeader JX1 and JX2 Overview

MicroHeader #1 (JX1)				MicroHeader #2 (JX2)			
	Signal Name	Source	Pins		Signal Name	Source	Pins
PL	JX1 I/Os, for 7010/20: PUDC on JX1.17 (pulled up to VCCO_34), PL_LED, PL_PB, FMC_PRSNT_N, HDMI (x9), HDMIO I2C, FMC SDA/SCL	Zynq Bank 34 or Zynq Bank 35	50 ##	PL	JX2 I/Os for 7015/30: PUDC is on JX2.23. HDMI (x14), FMC (x36 Diff).	Zynq Bank 35 or Zynq Bank 34	50 ++
	Bank 13 I/Os	Zynq Bank 13	8 **		Bank 13 I/Os: PL_PB (x4), PL_LED (x3)	Zynq Bank 13	7 **
JTAG	TMS_0	Zynq Bank 0	4	PS	PS MIO: PMOD/eMMC (x8), PG_MODULE	Zynq Bank 500	9
	TDI_0	Zynq Bank 0		CTRL	VCCIO_EN	Module/Carrier	1
	TCK_0	Zynq Bank 0			No Connect	No Connect	1
	TDO_0	Zynq Bank 0		PWR	VADJ_34/35	Carrier	3
CTRL	FPGA_DONE	Zynq Bank 0	1		VADJ_13	Carrier	1
	Carrier_SRST#	Carrier. Drives bank 501.	1		VIN_HDR	Carrier	5
	PWR_Enable	Carrier	1		GND	Carrier	23
Power	VIN_HDR	Carrier	4	**Total**			100
	GND	Carrier	23				
	VADJ_34/35	Carrier	3				
	FPGA_VBATT	Carrier	1				
N.C.	No Connects	No Connects	4				
TOTAL			100				

** PicoZed 7015/7020/7030
PicoZed 7010/7020 Bank 34 and PicoZed 7015/7030 Bank 35
++ PicoZed 7010/7020 Bank 35 and PicoZed 7015/7030 Bank 34

Table 12 – MicroHeader JX3 Overview

MicroHeader #3 (JX3)			
Signal Name		**Source**	**Pin Count**
PL	Bank 13 I/Os, PMODs JB & JZ, PL_CLK	Zynq Bank 13	20 **
XCVR	MGTTX I/Os	Zynq Bank 112	20 ##
	MGTRX I/Os	Zynq Bank 112	
	MGTREFCLK I/Os	Zynq Bank 112	
PS	SD_CARD	Zynq Bank 501	7
	USB_UART	Zynq Bank 501	2
	PS_PB1, PS_LED1, PS_LED2	Zynq Bank 501	3
SOM	Gigabit Ethernet	SOM PHY	10
	USB OTG – TYPE A (Data & Ctrl). VBUS listed below.	SOM PHY	4
Power	USB_VBUS_OTG	Carrier	1
	VADJ_13	Carrier	2
	MGTAVCC	Carrier	4
	MGTAVTT	Carrier	2
	GND	Carrier	25
TOTAL			100

** PicoZed 7020 has 10 I/O and PicoZed 7015/7030 adds 20 I/O
PicoZed 7015/7030 only

2.10 Multi-Gigabit Transceivers (MGTs)

Four MGT interfaces are available with the 7015/30 SOMs:

1) LPC FMC – see section: **2.6**
2) PCIe x1 – see section: **2.5**
3) SFP+ - see section: **2.7**
4) 4 SMAs – see section: **2.10.1**

- The PicoZed 7015 and 7030 SOMs have four multi-gigabit full-duplex transceiver lanes that reside on Bank 112 of the Zynq device. These high speed transceivers are used to interface to multiple high speed standard interfaces such as PCI Express and FMC. In addition to the PCIe and FMC interface, they can interface the remaining available MGT pins to other high speed interfaces such as Ethernet, Serial ATA, etc....

- The PicoZed 7015 is fitted with the XC7Z015-1CLG485 and is enabled with GTP transceivers which are capable of a transceiver data rate up to 3.75Gb/s. Speed grade devices of -2 or -3 are capable of data transceiver rates up to 6.25Gb/s.

- The PicoZed 7030 is fitted with the XC7Z030-1SBG485 and is enabled with GTX transceivers which are capable of a transceiver data rate up to 6.6Gb/s. Speed grade devices of -2 or -3 are also capable of data transceiver rates up to 6.6Gb/s in the SBG package.

Two differential MGT reference clock inputs are available for use with the GTP/GTX lanes. Either clock input can be used as the clock reference for any one or more of the GT lanes in bank 112. This allows the user to implement various protocols requiring different line rates.

Gigabit transceiver lanes and their associated reference clocks are connected to the carrier board via the JX3 MicroHeader. The table below shows the MGT connections between the Zynq device and the JX MicroHeader.

GTP/GTX Name:	SOM Net Name:	Carrier Net Name:	JX3 Pin:
MGT0	PCIE_TX0_P	PCIE-TX0_P	13
	PCIE_TX0_N	PCIE-TX0_N	15
	PCIE_RX0_P	PCIE-RX0_P	8
	PCIE_RX0_N	PCIE-RX0_N	10
MGT1	MGTTX1_P	MGTTX1_P	19
	MGTTX1_N	MGTTX1_N	21
	MGTRX1_P	MGTRX1_P	14
	MGTRX1_N	MGTRX1_N	16
MGT2	MGTTX2_P	MGTTX2_P	25
	MGTTX2_N	MGTTX2_N	27
	MGTRX2_P	MGTRX2_P	20
	MGTRX2_N	MGTRX2_N	22
MGT3	FMC_MGT_TX_P	FMC_MGT_TX_P	31
	FMC_MGT_TX_N	FMC_MGT_TX_N	33
	FMC_MGT_RX_P	FMC_MGT_RX_P	26
	FMC_MGT_RX_N	FMC_MGT_RX_N	28
MGT_REFCLK0	RSVD_PCIE_REFCLK0_P	MGTREFCLK0_P	1
	RSVD_PCIE_REFCLK0_N	MGTREFCLK0_N	3
MGT_REFCLK1	RSVD_MGTREFCLK_P	MGTREFCLK1_P	2
	RSVD_MGTREFCLK_N	MGTREFCLK1_N	4

Table 13 – MGT Pin Assignments

2.10.1 SMA Data TX/RX_P/N pairs

The PZCC-FMC-V2 has four MGT Data SMA Female connectors for differential TX_P/N and RX_P/N data connections. These I/O's are not DC blocked on the carrier. If DC blocking is required for your application, Avnet recommends using an inline capacitor, such as the Fairview part:
http://www.fairviewmicrowave.com/inner-dc-block-5-mhz-18-ghz-sma-connectors-sd3241-p.aspx

The data connections are listed in **Table 13 – MGT Pin Assignments**.

2.11 USB UART – J1

The PZCC-FMC-V2 implements a USB-to-UART bridge connected to a PS UART peripheral. U1 is a Silicon Labs CP2104 USB-to-UART Bridge device and allows connection to a host computer via USB. The CP2104 connects to the USB Micro AB connector, J1. Basic TXD/RXD connection is implemented. When the port is not in suspend mode, LED D1 illuminates.

The USB UART interface is designed to operate in bus powered mode. In this mode the UART is powered solely from the host PC's USB connection. This mode does not require the carrier to be turned on. Once enumeration is complete, the communication port with the PC will remain persistent as long as the USB cable is plugged in. The carrier may be power cycled or reset without loss of the port connection which is useful in the event a user wants to monitor the UART outputs on a terminal window.

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers which permit the CP210x USB-to-UART bridge to appear as a COM port to host computer communications application software (for example, HyperTerminal or Tera Term). Please refer to the *Silicon Labs CP210x USB-to-UART Setup Guide* available at www.picozed.org. Note that each CP2104 ships with a unique ID and appears as a unique device when connected to a PC. Windows will enumerate multiple PicoZed FMC Carrier boards with a unique COM port for each one. This means that multiple PicoZed FMC Carriers can be connected to a single PC without issue.

The uart1 Zynq PS peripheral is accessed through MIO Bank 1/501 (1.8V). 3.3V to 1.8V level translators are placed on the data lines to allow this data connection.

SOM Net Name:	Carrier Net Name:	JX3 Pin:
USB_UART_RXD	USB_UART_RXD	42
USB_UART_TXD	USB_UART_TXD	44

Table 14 – CP2104 Connections

2.11.1 USB circuit protection

USB data lines, D+/-, are ESD protected with Bourns ESD diode array, CDSOT23-SR208.

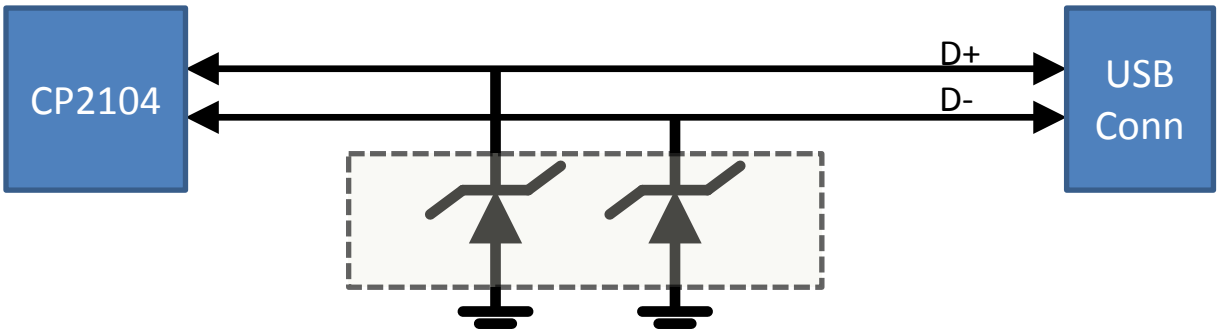

Figure 10 – ESD Protection

2.12 USB OTG Interface – J8

A USB Type A connector is routed to the SOM via header JX3 pins 63, 67, 69 and 70. In USB OTG Host mode (default), this interface sources VIN_HDR (+5.0V) power onto the USB_VBUS rail via power switch (U10) when an active high control signal is present on USB_OTG_CPEN (JX3.70).

This signal is level translated from SOM 3.3V to VIN_HDR via Q14 as shown below. The USB_OTG_ID signal is brought out to JX3.63 via R23 to allow Host or Device selection. When grounded the interface is initially set to host mode, when floating the interface is in device mode. Once connected, the roles can change via the Host Negotiation Protocol (HNP).

- By default, the PZCC-FMC-V2 ships in USB Host Mode, with capacitors C76/C79 placed and R87 set to 10KΩ.
- To change the mode from Host to OTG, change R87 from 10KΩ to 1KΩ, and remove capacitors C76/C79.
- To change the mode from Host to Device, leave R87 at 10KΩ, and remove capacitors C76/C79.

2.12.1 USB Interface protection

The 2.0 OTG data lines (D+/-) are ESD protected using a Bourns diode array (D12), PN: CDSOT23-SR208 as shown below.

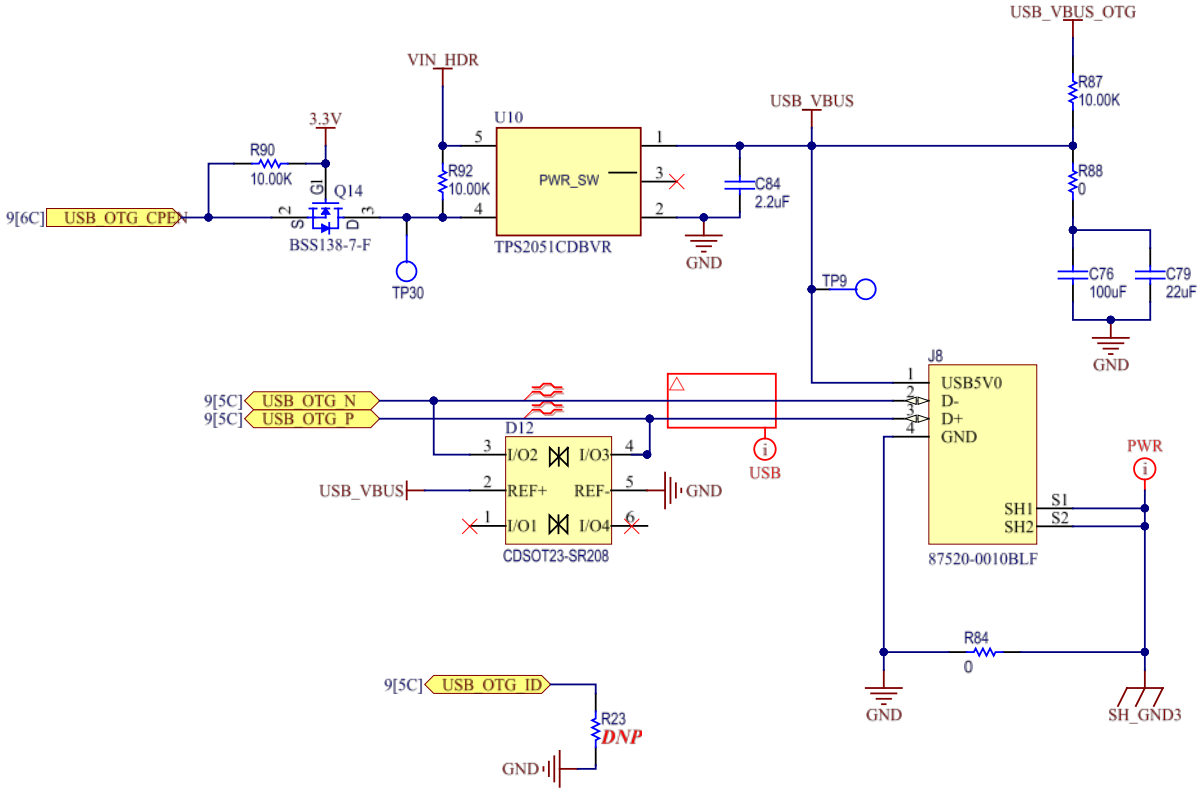

Figure 11 – USB OTG Interface

SOM Net Name:	Carrier Net Name:	JX3 Pin:
USB_OTG_ID	USB_OTG_ID	63
USB_OTG_P	USB_OTG_P	67
USB_VBUS_OTG	**USB_VBUS_OTG**	68
USB_OTG_N	USB_OTG_N	69
USB_OTG_CPE_N	USB_OTG_CPEN	70

Table 15 – USB OTG pin connections

2.13 SOM 10/100/1000 Ethernet RJ45 – J9

J9 is a SOM direct connect Ethernet port. The connector is a MagJack L829-1J1T-43 and contains integrated magnetics and two LEDs for connection indication. The left side LED[1] is green and indicates link status while the right side LED[0] is amber and indicates link activity.

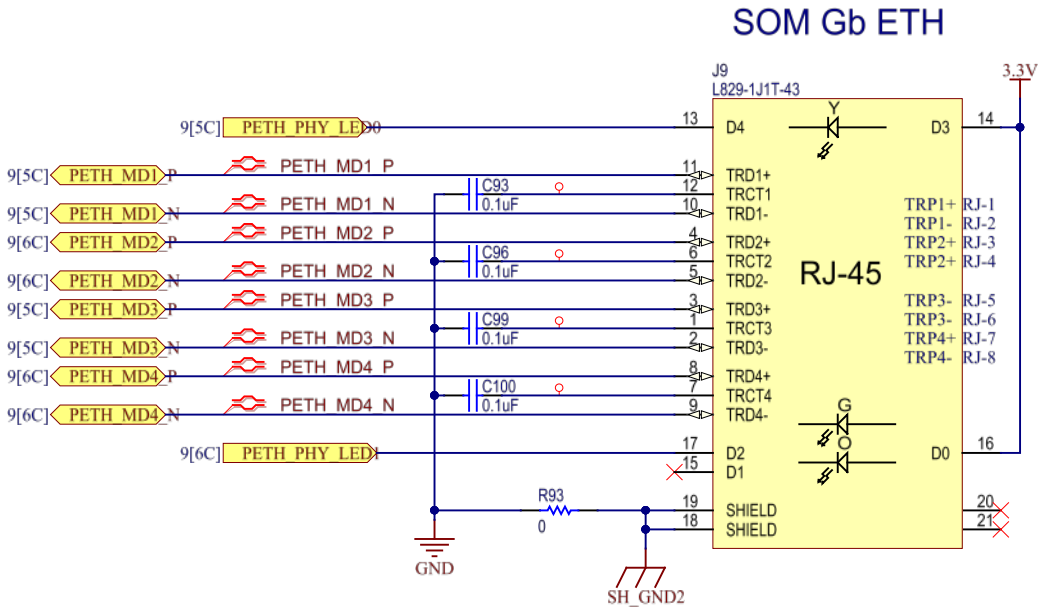

Figure 12 – RJ45 connection

The SOM's PHY is routed through JX3 directly to J1. For this reason, the PHY is configured via the SOM. The PZCC-FMC-V2 net names for this connector interface begin with PETH and are listed below.

SOM Net Name:	Carrier Net Name:	JX3 Pin:
PETH_PHY_LED0	PETH_PHY_LED0	47
PETH_PHY_LED1	PETH_PHY_LED1	48
PETH_MD1_P	PETH_MD1_P	51
PETH_MD2_P	PETH_MD2_P	52
PETH_MD1_N	PETH_MD1_N	53
PETH_MD2_N	PETH_MD2_N	54
PETH_MD3_P	PETH_MD3_P	57
PETH_MD4_P	PETH_MD4_P	58
PETH_MD3_N	PETH_MD3_N	59
PETH_MD4_N	PETH_MD4_N	60

Table 16 – Ethernet JX3 connections

2.14 MAC ID – EEPROM

MAC ID I2C ADDR: 0xA2

The SOM does not contain a MAC ID EEPROM so the carrier has one placed for design flexibility. A 2Kb MAC ID EEPROM with EUI-48 Node Identity (Microchip PN: 24AA025E48) is used to store the MAC ID for the SOM's Ethernet PHY. The device allows a user ID to be written at location 0x00 to 0x79. The devices' remaining memory is programmed at the factory with a globally unique node address stored in the upper half of the array. This address (0x80 to 0xFF) is permanently write protected. The I2C address is configured via JT5 and JT6. The default address is 0xA2.

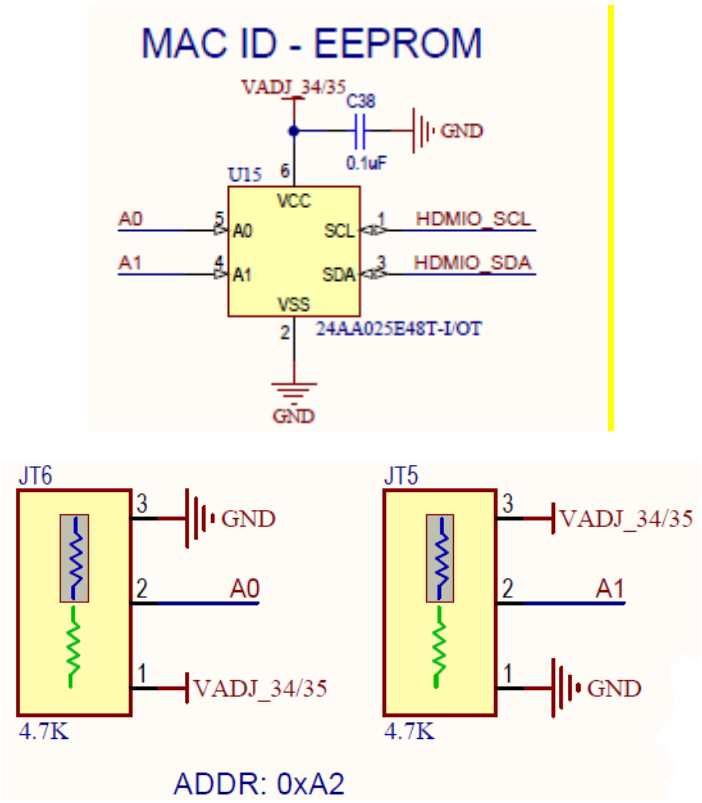

Figure 13 – MAC ID – I2C EEPROM

2.15 MAC ID – UNI/O EEPROM (7Z015/30 only)

In addition to the MAC ID EEPROM, a second 2Kb MAC ID UNI/O® EEPROM with EUI-48 Node Identity (Microchip PN: 11AA02E48) is used to store a MAC address for a SFP+ Ethernet module. This device is only accessible with a 7015/30 SOM. The device allows a user ID to be written at location 0x00 to 0xC0. The devices' remaining memory is programmed at the factory with a globally unique node address stored in the upper half of the array. This address (0xC0 to 0xFF) is permanently write protected.

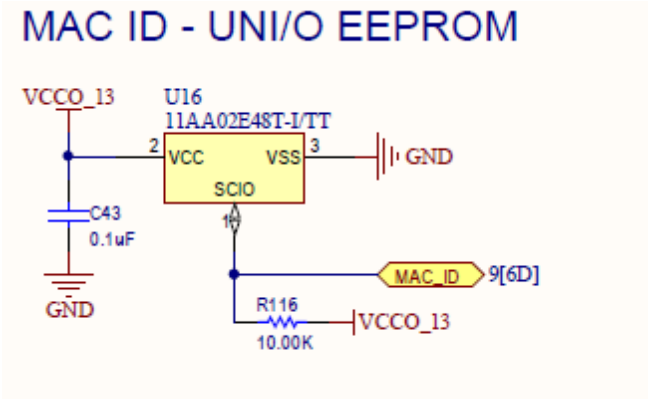

Figure 14 – MAC UNI/O EEPROM

2.16 Real Time Clock – Maxim DS3231MZ

RTC I2C ADDR: 0xD0

A Maxim DS3231 I2C RTC IC at address 0xD0 has been placed on the board to allow for clock and calendar functions. The RTC has a built in oscillator so an external device is not required. The interface is level translated using U11, a TCA9517 IC and attached to the HDMIO I2C bus. The RTC has a battery backup using a BHX1-1025 battery holder.

The RTC also has an open-drain, active-low interrupt or 1Hz square-wave output multifunction pin connected to RTC_INT. The interrupt function can be programmed to trigger upon a match between the timekeeping registers and either of the alarms. Refer to JX3 pin table for the pin assignments.

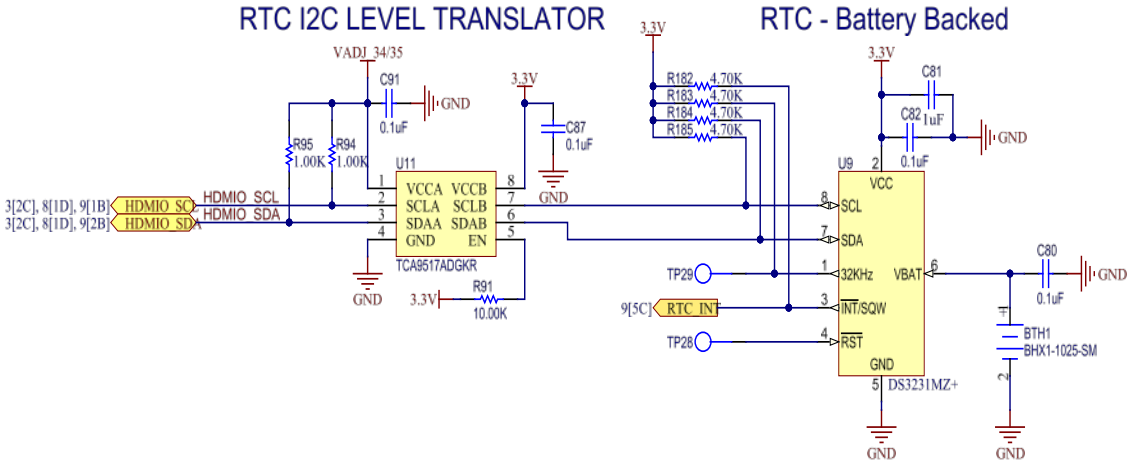

Figure 15 – RTC connections

RTC Battery installation instructions:
The CR1025 battery is required to be installed in a sleeve, part number BHX1-1025 (included in PZCC-FMC-V2 KIT) and firmly inserted into the carrier's socket. The coin cell's positive terminal is placed into the opening of the sleeve facing up. Please see figures below:

Figure 16 – CR1025 battery placed in BHX1025 sleeve

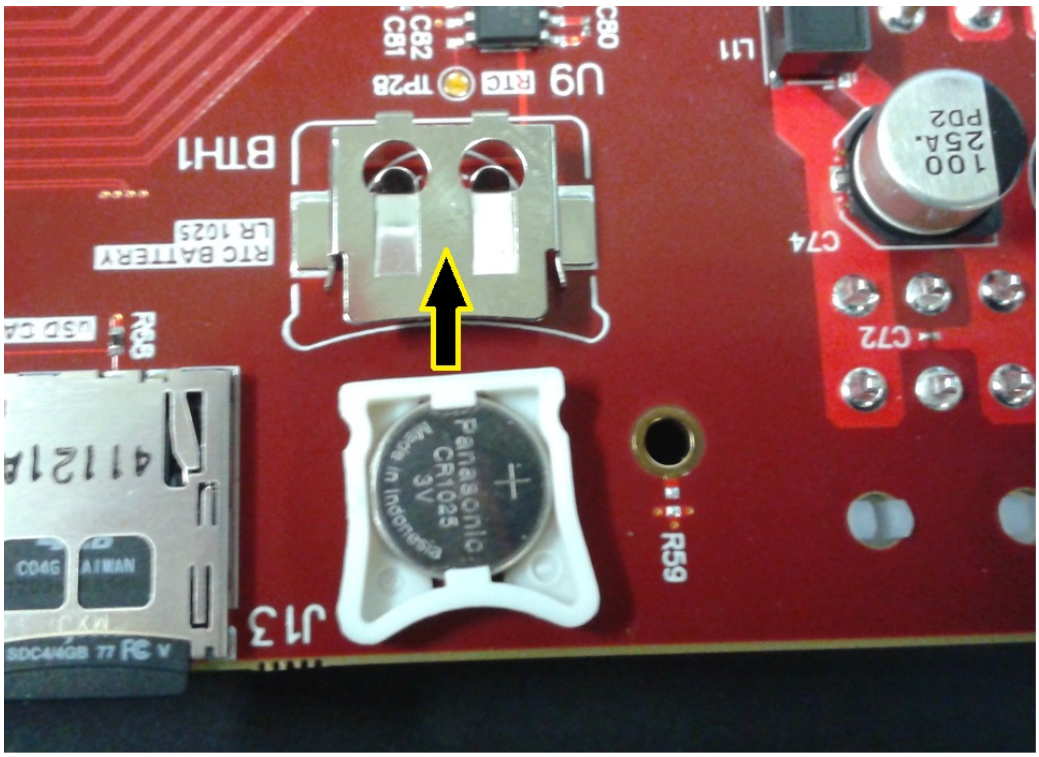

Figure 17 – Battery & sleeve orientation prior to insertion

2.17 HDMI Interface – J10

The PZCC-FMC-V2 has a HDMI V1.4 and DVI V1.0 video output port, J10. The data is configured for the YCbCr 4:2:2 format. This port is based on the Analog Devices ADV7511 225MHz HDMI transmitter IC, capable of transmitting up to 1080p resolution video. The port is a 16 bit interface, using data signals ADV7511 D20 to D35 and is split across the JX1 and JX2 interfaces. Refer to **Table 17** for the pin assignments.

The IC is configured via the I2C interface at address 0x72, based on the PD pin being pulled low. The user can assert this signal high to change the address to 0x7A.

LED D14 is used to indicate a Hot Plug Detect signal when a valid HDMI connection is made. D14 will turn on when this occurs.

To ensure low EMI emissions all power pins are triple filtered to this device using ferrite beads, inductors and capacitors. Additionally, the data signals to J10 are ESD protected using ESD protection diodes. If necessary, a 0603 varistor may be placed at location R155 to protect the CEC signal. By default this component is not placed.

SOM Net Name:	Carrier Net Name:	JX1 Pin:
JX_SE_0	HDMIO_SCL	9
JX1_SE_1	HDMIO_SDA	10
JX1_LVDS_0_P	HDMIO_CBCR5_D33	11
JX1_LVDS_1_P	HDMIO_CBCR7_D35	12
JX1_LVDS_0_N	HDMIO_CBCR4_D32	13
JX1_LVDS_1_N	HDMIO_CBCR6_D34	14
JX1_LVDS_3_N	HDMIO_SPDIF	20
JX1_LVDS_4_P	HDMIO_HPD	23
JX1_LVDS_4_N	HDMIO_PD	25
SOM Net Name:	**Carrier Net Name:**	**JX2 Pin:**
JX2_SE_0	HDMIO_CBCR0_D28	13
JX2_SE_1	HDMIO_CBCR1_D29	14
JX2_LVDS_0_P	HDMIO_CBCR3_D31	17
JX1_LVDS_0_N	HDMIO_CBCR2_D30	19
JX1_LVDS_2_P	HDMIO_INT	23
JX1_LVDS_10_P	HDMIO_Y1_D21	47
JX1_LVDS_10_N	HDMIO_Y0_D20	49
JX1_LVDS_16_P	HDMIO_Y3_D23	67
JX1_LVDS_16_N	HDMIO_Y2_D22	69
JX1_LVDS_22_P	HDMIO_Y5_D25	87
JX1_LVDS_23_P	HDMIO_Y7_D27	88
JX1_LVDS_22_N	HDMIO_Y4_D24	89
JX1_LVDS_23_N	HDMIO_Y6_D26	90

Table 17 – HDMI Pin Mapping table

Please refer to Analog Devices ADV7511 datasheet, Hardware User's Guide and Programming guide at www.analog.com for detailed information. The ADI EngineerZone is also a very useful source of information -- https://ez.analog.com/welcome. Additionally, more detailed information on the ADV7511, including a hardware user guide and example schematics/layout, can be found on the Analog Devices EngineerZone: http://ez.analog.com/docs/DOC-1740

2.18 microSD Card Interface

The Zynq PS SD/SDIO peripheral controls communication with the FMC-V2 carrier's microSD Card. The microSD card can be used for non-volatile external memory storage as well as booting the Zynq-7000 AP SoC. PS peripheral sd0 is connected through Bank 1/501 MIO[40-46], including Card Detect.

The microSD Card is a 3.3V interface is connected through MIO Bank 1/501 which is set to 1.8V. To interface to the SD card, the carrier card uses a Texas Instrument TXS02612RTWR voltage level translator IC. This part includes a 6-channel SPDT switch with voltage-level translation capability.

The TXS02612 has three separate supply rails that operate over the full range of 1.1 V to 3.6 V. This allows the Zynq MIO and SDIO peripherals to operate at different supply voltages.

The microSD Card is connected through an 8-pin micro SD card connector, J13, Molex 502570-0893. Note that this connector's supported temperature range is -25° to 85° C. A Class 4 card or better is recommended. Up to 32 GB is supported. If a user intends to use the microSD card interface at industrial temperatures, an industrial temperature microSD card is required. Please request more information on this from your local Avnet representative. Alternatively, the customer can load their image on the eMMC memory on the SOM.

SOM Net Name:	Carrier Net Name:	JX3 Pin #	J13 SD Card Pin:
PS_MIO41	SD_CMD	34	P3
PS_MIO43	SD_D1	36	P8
PS_MIO42	SD_D0	37	P7
PS_MIO45	SD_D3	38	P2
PS_MIO44	SD_D2	39	P1
PS_MIO46	SD_CD	41	G4
PS_MIO40	SD_CLK	43	P5

Table 18 – microSD Card Pin assignments

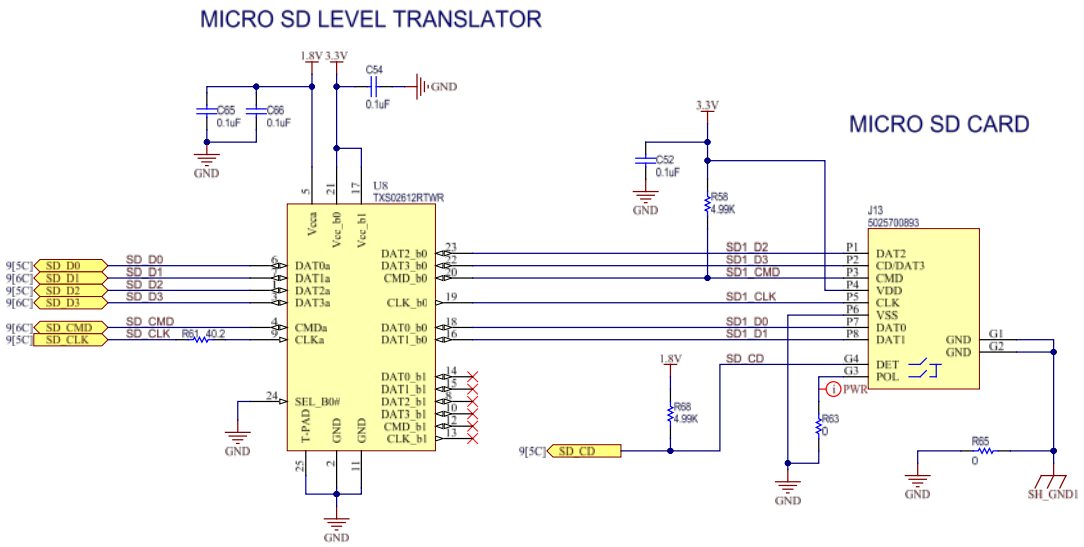

Figure 18 – microSD card interface

2.19 Fan Header – JP3

JP3, a three pin 0.85” pitch fan header has been placed to allow the customer to use a fan for SOM cooling if needed. By default the header is connected to the VIN_SW which is +12V via R161. If a 5V fan is desired, remove R161 and populate R162 with a 0402 zero ohm resistor.

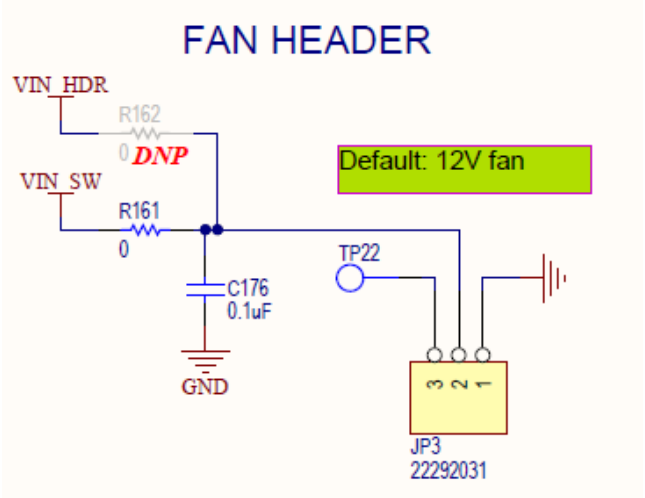

Figure 19 – Fan Header connections

2.20 JTAG Configuration – J7

An auto switching JTAG interface port is provided on the PZCC-FMC-V2 through J7, a PC4 compliant connection. The port defaults to SOM JTAG operation unless an FMC board is placed. Upon insertion of a FMC board, the interface will switch the FMC into the JTAG chain via U3.

A Xilinx JTAG platform cable (HW-USB-II-G) or a Digilent JTAG HS2 or HS3 programming cable should be used when programming via these ports. Diode D18 on the VREF pin is used to prevent the JTAG cable from back feeding into the PZCC-FMC-V2 3.3V power supply.

Pullup resistors R191, R192, R193 are not populated by default as the FMC module should have the pullup resistors in place. However, if the FMC module does not have the pullups, this resistor pack can be placed.

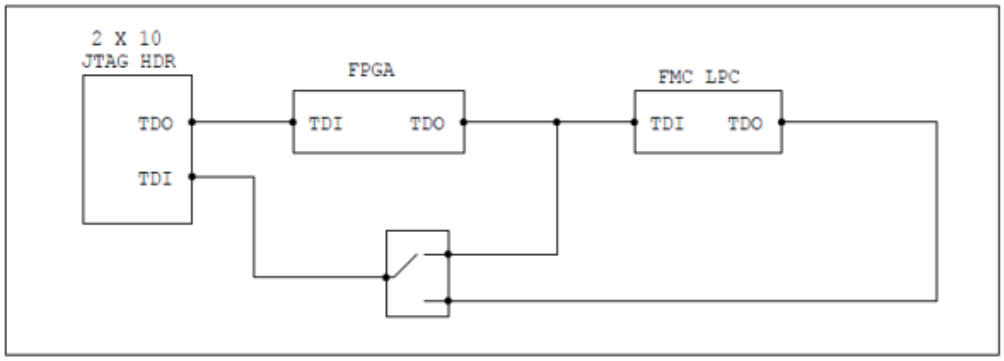

Figure 20 – SOM & FMC JTAG Topology

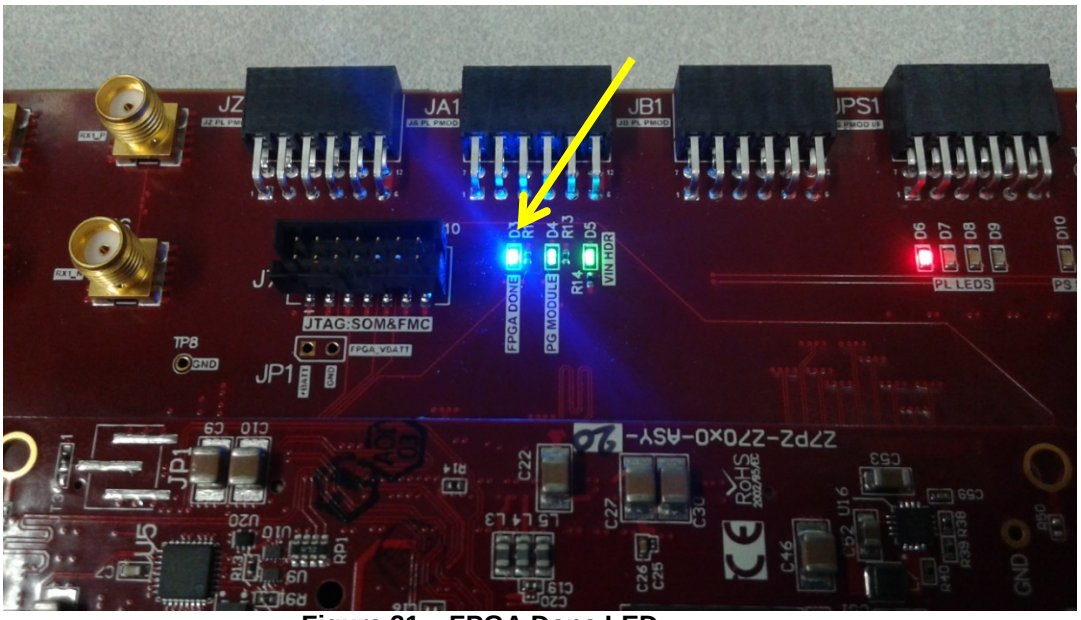

Figure 21 – FPGA Done LED

A blue DONE LED (D3) is connected to the Zynq SOM via JX1.8, net name FPGA_DONE and is located on Bank 0, R11 of the FPGA. When the SOM's PL is properly configured this pin is driven high by the FPGA which turns the DONE LED on.

3 Power

3.1 Power Input – J2/SW7

The board is powered through J2 and SW7 power switch. Slide SW7 to the left to turn on the board. Sliding SW7 to the right turns off the board. J2 is a 12V 2x3 6 pin connector which is NOT ATX compatible. While the board can accommodate up to 15VDC in, to maintain FMC compliance the maximum input voltage should not exceed 12.8V, (12V +/- 5%) to minimize component stress thereby increasing the products operational life.

- D19 and D20 are used for power steering in the event the user wants to insert the board into a PCIe x1 slot for development purposes. **Please Note:** While the PCIe slot can source 10 watts of power (up to 25W via PC configuration) it is recommended the carrier card be plugged in via J2 to eliminate potential under-power scenarios.

- The maximum input current from J2 is limited by filter L11, which has a rating of 5.0 Amps. Any current exceeding this value will damage the filter network. The power supply shipped from Avnet is Avnet part number AES-SLP-12V5A-G and is rated at 12V, 5.0 Amps and is recommended for use with the PZCC-FMC-V2 board.

3.2 Molex to Non-ATX connection

If you choose to power the PZCC-FMC-V2 carrier in an enclosed PC chassis and do not want to attach the external power adapter, an adapter ships with the kit. See Section 2.5 for details.

3.3 Power Rails

The table below lists the voltage rails, currents, and tolerances. 0.1% resistor values were used on the 1.0V_AVCC and 1.2V_AVTT rails to improve the full load accuracy. C74, a bulk 12Vin cap is placed to minimize ripple on the 12V power in rail. This component is placed on the bottom side of the board due to top side space limitations. If this placement is undesirable, the capacitor may be removed by the customer after power testing has been performed with it removed. Avnet has not tested power performance with this component removed.

Voltage (V)	Tolerance	IC	Max DC current	Functional area
12V Input	5%	Wall adapter, NOT ATX compatible	5.0A	All power
PCIe 12V Input	10%	N/A, PCIe x1 card edge	10W = 833 mA, 25W = 2083 mA.	All power
5V	5%	U5, ADP2384ACP	3.0A	SOM VIN Header
VADJ - 1.8V, 2.5V or 3.3V For SOM VCCIO 13, 34, 35 **NOTE: For 7030 SOMs VADJ MUST be set to 1.8V ONLY!**	5%	U6, ADP50502, CH1	4.0A	PZCC-FMC-V2 & SOM VCCIO banks: 34, 35.
3.3V & VCCO_13	5%	U6, ADP50502, CH2	4.0A	PZCC-FMC-V2 logic, Pmod, Ethernet, Vcco_13, LEDs
1.0V_AVCC	3%	U6, ADP50502, CH3	1.2A	SOM MGT Core
1.2V_AVTT	3%	U6, ADP50502, CH4	1.2A	SOM MGT
1.8V	5%	U6, ADP50502, CH5	200mA	microSD level translator, HDMI

Table 19 – Voltage Rails w/ Current Estimates

3.4 2.5V LDO – U12

The clock synthesizer U13 requires a VCCO of 2.5V. U12, an ADI LDO (ADP121-AUJZ25R7) provides 2.5V at 150mA. This IC is always enabled by being pulled up to 3.3V.

3.5 JP1 – FPGA VBAT (VCCBATT)

JP1 is a non-populated 100 mil dual pin connector. Use this connection to provide battery backup power for the FGPA's internal volatile memory that stores the key for the AES decryptor. If using this connection, the SOM will require a resistor to be removed. Please see the appropriate SOMs User Guide (choose the latest revision):
http://picozed.org/support/documentation/4736

NOTE: The voltage input to this connector MUST NOT EXCEED 2.0V or FPGA damage may result. This connection should be to a power supply or 1.5V battery. The positive voltage is attached to pin 1, labeled "+BAT". Ground is attached to pin 2, labeled "GND". See below figure.

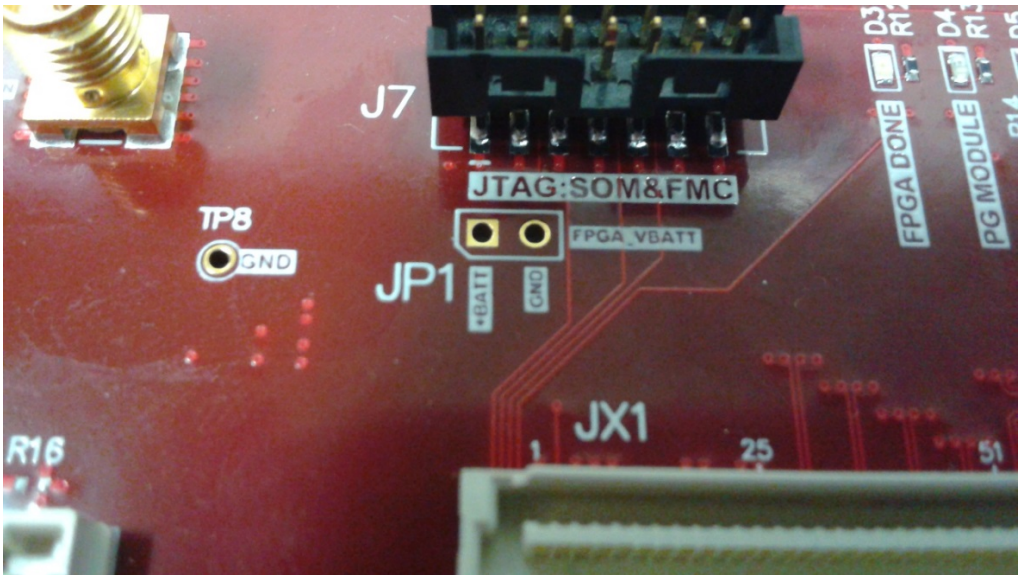

Figure 22 – JP1 VBAT connector

3.6 VADJ selection - JP5

VADJ rail is configurable via JP5. VADJ is an independent rail supplying power to the Zynq PL I/O banks and connected Pmods. VADJ drives banks 34 and 35**.**

WARNING: When using a 7030 SOM, VADJ MUST remain at the 1.8V setting otherwise the SOM will be damaged!

Use the table below for Vadj selection.
NOTE: if JP5 is left open, the board defaults to +1.8V VADJ rail setting.

JP5 Jumper Position (pins)	VADJ
1-2 or Open	1.8V
3-4	2.5V
5-6	3.3V

Table 20 – VADJ Selection Table JP5

3.7 Sequencing

- PWR_EN signal, active high, JX1.5, allows the carrier to turn on or off the PicoZed power supplies. R18 and C6 have been placed to adjust the timing of this signal during power off conditions. This signal should not be de-asserted until VCCIO_EN is de-asserted. In the carrier off condition (power plug removed or power switch turned off), this signal is driven low.

- VCCIO_EN signal, active high, JX2.10, originates on the SOM and is the output of the 1.8V regulator, PG_1V8. This signal enables the carrier's 3.3V supply, which in turn enables the VADJ regulator. When the carrier is turned off (power switch turned off or power plug removed) or the PicoZed's PG_1V8 signal is de-asserted VCCI_EN is driven low, which turns off the FMC-CC supplies. 5V will continue to be supplied unless the power switch SW7 is set to OFF.

- PG_CARRIER signal, active high, JX2.11, is pulled up by PicoZed's +3.3V PG_MODULE signal. This signal can be pulled low by the carrier board (SW4), the FMC board or the PicoZed when the board's power circuitry is not 'Good' yet.

- The following diagram illustrates the power supply sequencing on power up. Note Vin and PWR_Enable can come up simultaneously, but shown staggered as PWR_Enable can come up later.

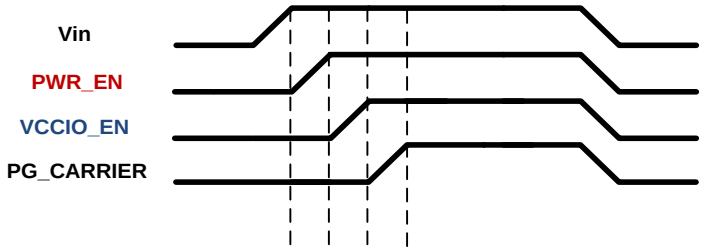

Figure 23 – Power Sequencing

The PG_CARRIER (on PZCC-FMC-V2) and PG_MODULE (on PicoZed) signals are wired OR and tied to the Zynq Power On Reset signal. When the power supplies are valid on both the SOM and carrier, the PG signal de-asserts the Zynq POR signal.

3.8 Bypassing/Decoupling/Filtering

The PZCC-FMC-V2 follows the recommended decoupling and layout techniques per each manufacturer's datasheet.

3.9 PG Module Power Good LED

A green status LED, D4, illuminates when PG_CARRIER signal is high (good).

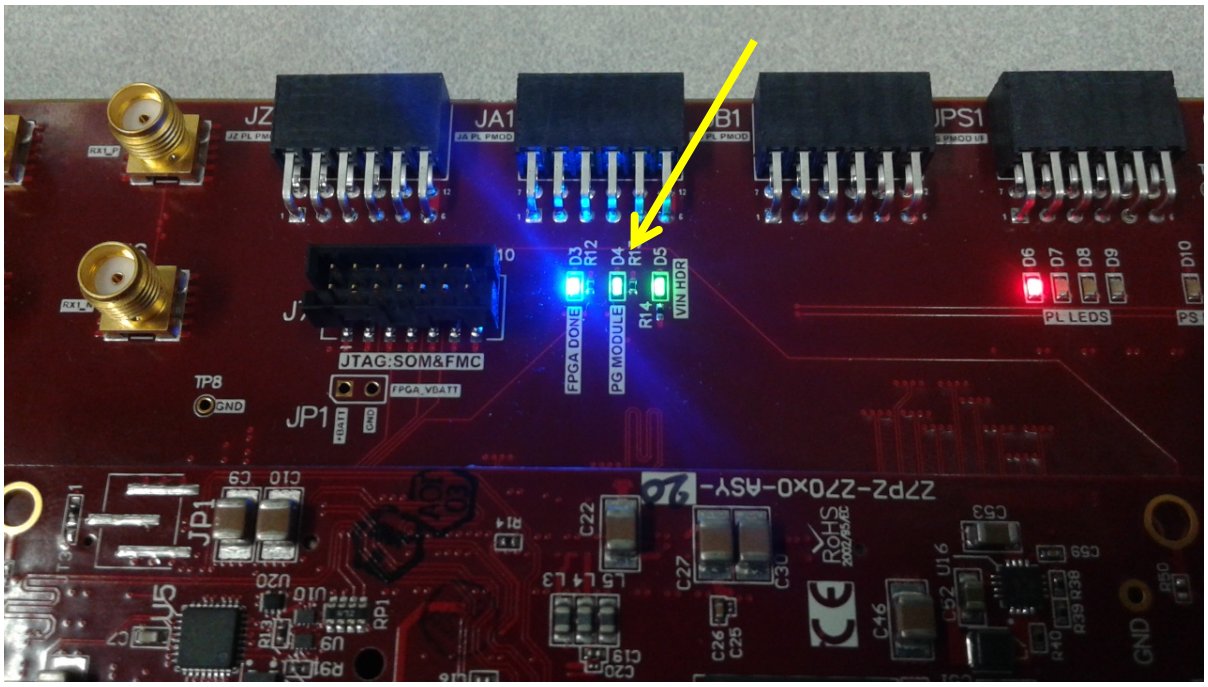

Figure 24 – PG_MODULE LED

4 Jumpers, configuration and test points:

The below table is a quick reference to all of the jumpers, configuration settings and test points on the FMC. For detailed information, refer to the appropriate sections in this document.

Reference Designator	Name	Default	Notes:
JP1	FPGA_VBAT_TEST	Open	Attach a 1.5V battery to this connection to maintain FPGA configuration when board is unpowered.
JP2	SFP+ Laser Enable	Placed	Placed turns on the SFP+ TX laser, not placed keeps it off.
JP3	Fan Header	Placed	Used to power a SOM fan. Default is 12V.
JP4	FMC GA [1:0]	Set to 00	FMC address select. Use jumper headers for selection.
JP5	VADJ	Open or 1-2: 1.8V 3-4: 2.5V 5-6: 3.3V	Used to select 1.8V, 2.5V or 3.3V VADJ level for the SOM VCCIO Banks 34 and 35 as well as the FMC connector. **NOTE: 7030 SOMs MUST be set to 1.8V only!**
JT1/JT2	CLK ADDR	Populated	Use to select Clock IC I2C address. Defaults to 0xD8
JT3/JT4	CLK EEPROM	Populated	Use to select clock I2C EEPROM address. Defaults to 0xA0
JT5/JT6	MAC ID EEPROM	Populated	Use to select MAD ID EEPROM. Defaults to 0xA2
JA1	JA PL PMOD	Populated	7015/20/30 PMOD interface.
JB1	JB PL PMOD	Populated	7015/20/30 PMOD interface.
JZ1	JZ PL PMOD	Populated	7015/30 PMOD interface.
JPS1	PS PMOD	Populated	All SOMs have access to this PMOD interface. Shared with SOMs eMMC.
JSFP1	JSFP1	Populated	SFP+ interface signals breakout to this for connection.
J1	USB UART	Populated	Micro USB UART connection.
J2	+12Vin	N/A	+12V input
J3, J5	MGTX1_P/N	Populated	MGT SMA TX DATA
J4, J6	MGTRX1_P/N	Populated	MGT SMA RX DATA
J7	JTAG	Populated	SOM & FMC peripheral JTAG interface.
J8	USB OTG	Populated	USB 2.0 OTG Type A header.
J9	ETHERNET	Populated	SOM driven Gb Ethernet connector.
J10	HDMI	Populated	HDMI header attached to AD7511 HDMI transmitter.
J11	VCCIO_EN	Not Populated	Short to test the PZCC-FMC-V2 power supplies while SOM not installed. Normal operation leave this open.
J12	VOLTAGE MON	Not Populated	Use the 0.1” holes to measure the voltage of each rail.
J13	Micro SD Card Cage	Populated	MicroSD Card socket
SW1-SW6	USER PB	Populated	User pushbuttons. See section: 2.2.1
SW7	PWR SWITCH	Off	Use to turn on board. Left = on, right = off.
SW8	CARRIER SRST N	Populated	Assert a carrier board reset. See section 2.
SW9	PG MODULE N	Populated	Assert a PG MODULE reset. See section 2.
P1	SFP+	Populated	SFP+ interface.
CON1	FMC	Populated	Low Pin Count FMC Interface.
TP9	USB_VBUS	Populated	5.0V = USB connected or USB OTG Enabled.
TP12	PWR_ENABLE	Populated	+V = PWR_ENABLE from SOM.
TP14	PG_MODULE	Populated	High when 5052 switcher is within regulation.
TP18	VCCIO_EN	Populated	5.0V = VCCIO_EN measurement.
TP22	FAN HEADER	Populated	Spare pin on fan header.
TP25/27	PCIe 12V	Populated	12V PCIe voltage pads
TP26	PCIe_WAKE_N	Populated	PCIe Wake signal pad.
TP30	USB OTG ON	Populated	3.3V = OTG ON. 0V = OTG OFF.

Table 21 – Switch/Jumper/Connector Settings

4.1 FMC GA [1:0] jumper header

The carrier allows the user to select the FMC board address via JP4 and 2 jumper headers. The address range is from 0 to 3 via jumper headers. The jumpers force a high or a low on address bits 1 or 0. Default FMC address is 00 where the jumpers are placed at location 3-5 and 4-6.

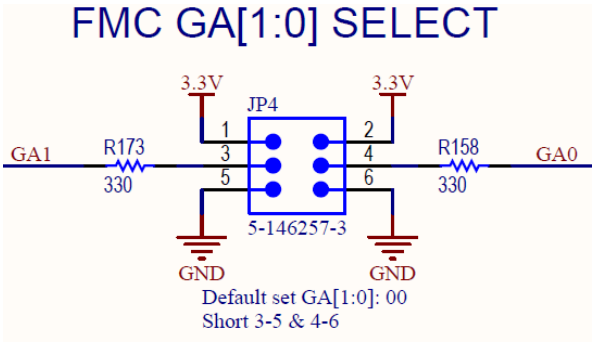

Figure 25 – FMC Address select

Carrier Net Name	FMC LPC CON2E connection
GA0	C34
GA1	D35

Table 22 – FMC GA [1:0] address select

4.2 Clock Synthesizer test header

The clock synthesizer has a test header which is not populated by default. Users can monitor the synthesizer GPIO, power, I2C interface and interrupt. See below figure.

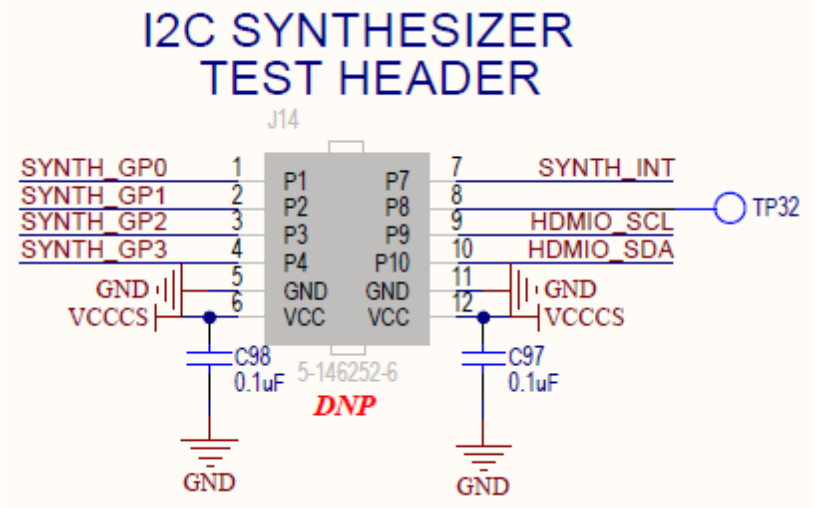

Figure 26 – Clock synthesizer test header

4.3 Power Supply monitor header – J12

The PZCC-FMC-V2 has a power supply monitor connection. While this is primarily for testing, it can be accessed by the user to monitor the voltages on the carrier card. The below figure shows the available voltage monitor points.

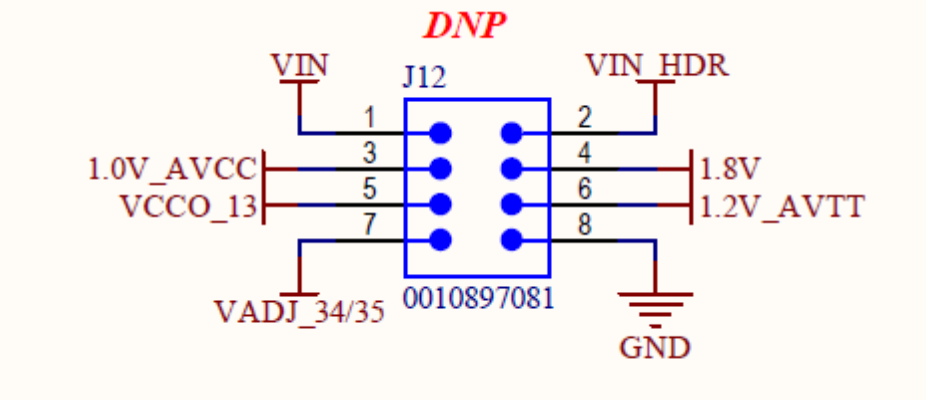

Figure 27 – Voltage Monitor Connections

5 Mechanical

5.1 Diagram and Model

A mechanical diagram and a 3D Model for the PZCC-FMC-V2 are available for download at **www.picozed.org → Product → PicoZed FMC Carrier Card V2 → Documentation** under the ***Mechanical Drawings*** heading.
http://picozed.org/support/documentation/13076

5.2 Weight

The weight of the PZCC-FMC-V2 with rubber feet, SD card, and jumpers populated and without the faceplate or SOM attached is 155 grams (5.47 ounces).

6 Revision History

Version date	Ver #	Reason for change
26 Apr 2016	1.0	Initial release

Table 23 – Revision History

Appendix A – additional information/test results

This section is used to list additional items that may be of interest to readers. This information may change over time and the reader is encouraged to visit the website for the latest data.
http://picozed.org/product/picozed-fmc-carrier-card-v2

I. Functional Transceiver testing:

The PicoZed 7030 SOM contains a Xilinx Zynq 7030 chip in a SBG485 package. Although this SOM is capable of operating at **up to** 6.6Gbps, tuning may be required to achieve this rate. The following link provides tuning guidance: http://picozed.org/support/trainings-and-videos.

Tech Tip - Transceiver Tools 101: Intro to IBERT
Tech Tip - Transceiver Tools 102: We have an IBERT bit stream, now what?
Tech Tip - Transceiver Tools 103: Now that we are running, what are all these adjustments?
Tech Tip - Transceiver Tools 104: Getting More Margin

When the PicoZed 7030 is used it is also recommended a full transceiver to transceiver signal integrity check is performed. Items between the transceivers, such as board to board connectors, interface connections, ESD parts, cables, carrier layout practices, etc. must be carefully evaluated to ensure they can support the intended data rates without performance degradation.

For NON-Standard protocols, Avnet recommends using 5.0Gbps as a max data rate, as this is the most stable link with greatest margin across the largest set of bit streams. More performance may be obtained by adjusting the speed up or down as necessary. If your protocol is a standard protocol, such as what is in the table below, it is possible to reach speeds greater than 5.0Gbps as there tends to be more margin while using these protocols.

Protocol	Data rate (in Gbps)	Encoding
Gb Ethernet	1.25	8B/10B
PCIe Gen 1 / Gen 2	2.5 / 5.0	8B/10B
XAUI	3.125	8B/10B
SATA / SATA2 / SATA3	1.5 / 3.0 / 6.0	8B/10B
SRIO Gen1 / Gen 2	3.125 / 6.25	8B/10B
DisplayPort	1.62 / 2.7 / 5.4	8B/10B
Fibre Channel	1.0625 / 2.125 / 4.25	8B/10B
Aurora	3.75	8B/10B

Note, RED is 7030 only
Note list is not all inclusive and there COULD be exceptions NOT noted

II. Operating Temperature Range:

The PZCC-FMC-V2 Carrier Card has been designed and tested to operate at the commercial operating temperature range of 0C to +70C. The temperature range is limited due to the temperature grade of many of the components on the board.

Note: Thermal testing has been successfully performed on a similar carrier card with all industrial variants of PicoZed SOMs at the industrial temperature range (-40C to +85C). This testing was performed to validate the SOMs operating range and not the carrier's, therefore the carrier is not guaranteed to operate at this range yet Avnet has not had a failure in doing so.

III. EMI Compliance:

There is no requirement for the PZCC-FMC-V2 to be tested to meet emissions compliance. However there is a requirement for the PicoZed SOMs to meet emissions testing in which case the carrier card may be used as the platform for testing. The test results may be posted on the www.picozed.org website or contact your local FAE for the latest data. The PZCC-FMC version 1 has been used in testing and can be referenced for expected emissions.