64Mbit SDRAM

1M x 16Bit x 4 Banks
Synchronous DRAM
LVTTL

Revision 0.1

Sept. 2001

Revision History

Revision 0.0 (June, 2001)

Revision 0.1 (Sep., 2001)

- Changed the Notes in Operating AC Parameter.
  < Before >
    5. For 1H/1L, tRDL=1CLK and tDAL=1CLK+tRP is also supported .
       SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.
  < After >
    5.In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported.
       SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

1M x 16Bit x 4 Banks Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
    - -. CAS latency (2 & 3)
    - -. Burst length (1, 2, 4, 8 & Full page)
    - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Burst read single-bit write operation
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

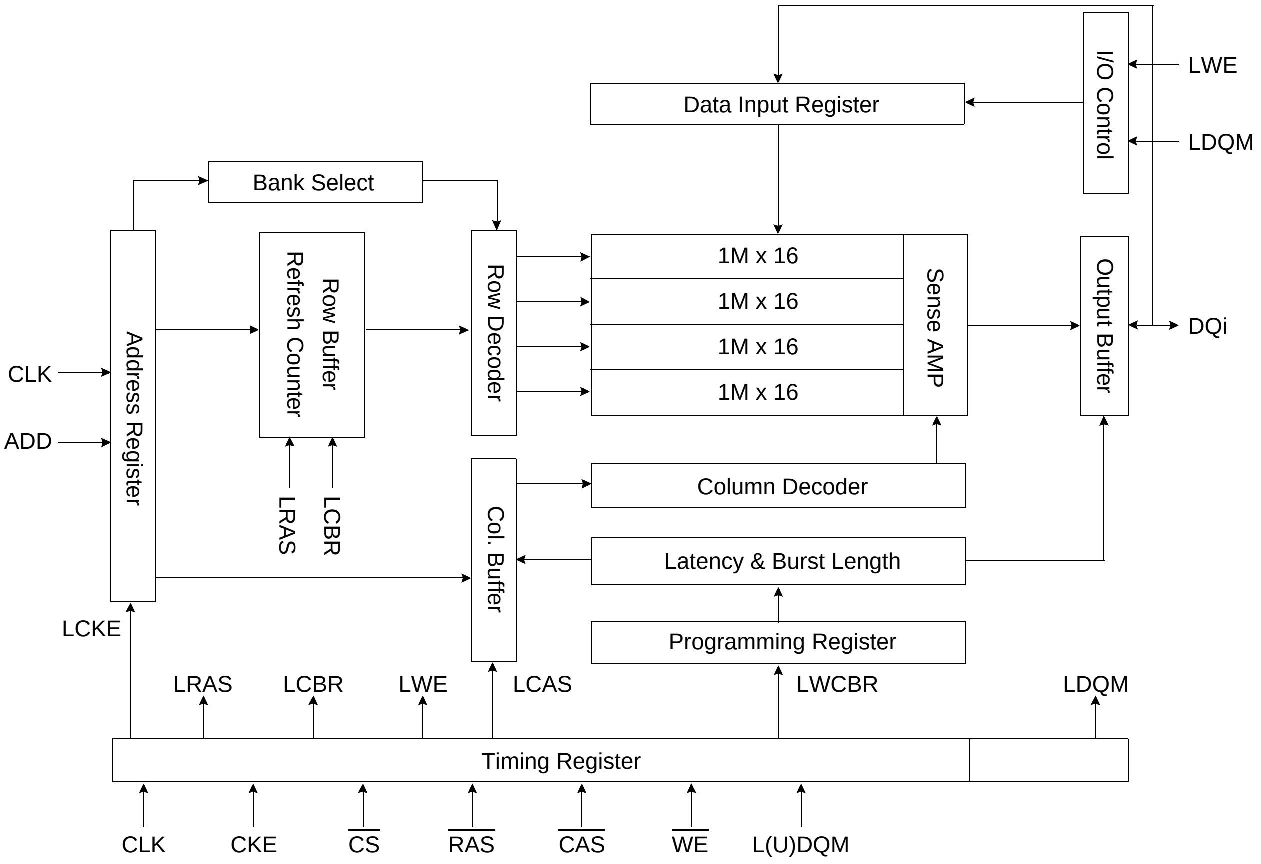
GENERAL DESCRIPTION

The K4S641632F is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

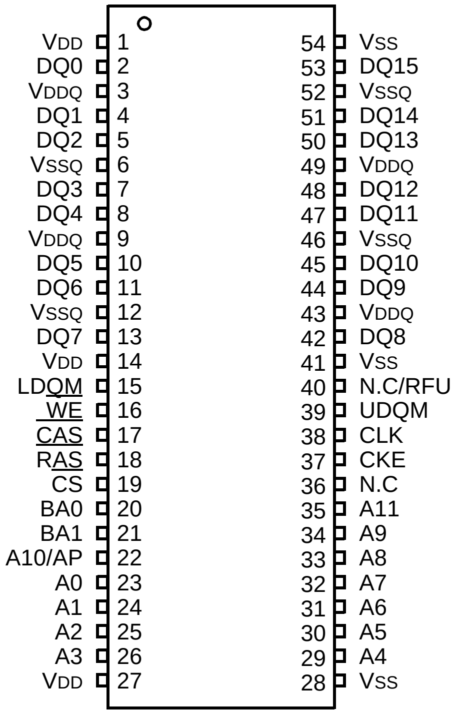
ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package
K4S641632F-TC50/TL50	200MHz(CL=3)	LVTTL	54 TSOP(II)
K4S641632F-TC55/TL55	183MHz(CL=3)		
K4S641632F-TC60/TL60	166MHz(CL=3)		
K4S641632F-TC70/TL70	143MHz(CL=3)		
K4S641632F-TC75/TL75	133MHz(CL=3)		
K4S641632F-TC1H/TL1H	100MHz(CL=2)		
K4S641632F-TC1L/TL1L	100MHz(CL=3)		

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top view)



54Pin TSOP (II)
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{\text{CS}}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A_0 ~ A_{11}	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA_0 ~ RA_{11}, Column address : CA_0 ~ CA_7
BA_0 ~ BA_1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{\text{RAS}}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
L(U)DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ_0 ~ $_{15}$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.
V_{DDQ}/V_{SSQ}	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection* */reserved for future use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	1	W
Short circuit current	IOS	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	VIH	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output logic low voltage	VOL	-	-	0.4	V	IOL = 2mA
Input leakage current	ILI	-10	-	10	uA	3

Notes :
1. VIH (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. The VDD condition of K4S641632F-55/60 is 3.135V~3.6V.

CAPACITANCE (VDD = 3.3V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit	Note
Clock	CCLK	2.5	4.0	pF	1
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, DQM	CIN	2.5	5.0	pF	2
Address	CADD	2.5	5.0	pF	2
DQ_0 ~ DQ_{15}	COUT	4.0	6.5	pF	3

Notes :
1. -75 only specify a maximum value of 3.5pF
2. -75 only specify a maximum value of 3.8pF
3. -75 only specify a maximum value of 6.0pF

DC CHARACTERISTICS

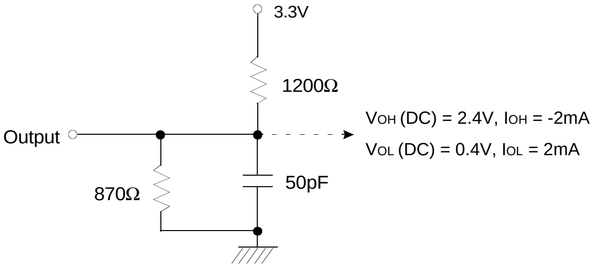
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version							Unit	Note
			- 50	- 55	-60	- 70	- 75	-1H	-1L		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	160	150	140	115	110	100	100	mA	1
Precharge standby current in power-down mode	I_{CC2}P	CKE $\leq V_{IL}$(max), t_{CC} = 10ns	1							mA	
	I_{CC2}PS	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$	1								
Precharge standby current in non power-down mode	I_{CC2}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns	15							mA	
	I_{CC2}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable	6								
Active standby current in power-down mode	I_{CC3}P	CKE $\leq V_{IL}$(max), t_{CC} = 10ns	3							mA	
	I_{CC3}PS	CKE & CLK $\leq V_{IL}$(max), $t_{CC} = \infty$	3								
Active standby current in non power-down mode (One bank active)	I_{CC3}N	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns	30							mA	
	I_{CC3}NS	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable	25								
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	180	170	160	140	135	110	110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	180	170	160	140	135	125	125	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V C	1							mA	3
		L	400							uA	4

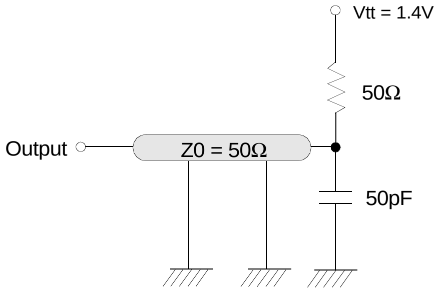
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S641632F-TC**
4. K4S641632F-TL**
5. Unless otherwise noted, input swing level is CMOS($V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ}$)

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Notes : 1. The DC/AC Test Output Load of K4S641632F-50/55/60 is 30pF.
2. The VDD condition of K4S641632F-50/55/60 is 3.135V~3.6V.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version							Unit	Note
		-50	-55	-60	-70	-75	-1H	-1L		
Row active to row active delay	tRRD(min)	10	11	12	14	15	20	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	tRCD(min)	15	16.5	18	20	20	20	20	ns	1
Row precharge time	tRP(min)	15	16.5	18	20	20	20	20	ns	1
Row active time	tRAS(min)	40	38.5	42	49	45	50	50	ns	1
	tRAS(max)	100							us	
Row cycle time	tRC(min)	55	55	60	68	65	70	70	ns	1
Last data in to row precharge	tRDL(min)	2							CLK	2,5
Last data in to active delay	tDAL(min)	2CLK +15ns	2CLK +16.5ns	2CLK +18ns	2CLK +20ns	2CLK +20ns	2CLK +20ns	2CLK +20ns	-	5
Last data in to new col. address Delay	tCDL(min)	1							CLK	2
Last data in to burst stop	tBDL(min)	1							CLK	2
Col. address to col. address delay	tCCD(min)	1							CLK	3
Number of valid output data	CAS latency=3	2							ea	4
	CAS latency=2	-				1				

Notes :
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	- 50		- 55		- 60		- 70		- 75		- 1H		- 1L		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	5	1000	5.5	1000	6	1000	7	1000	7.5	1000	10	1000	10	1000	ns	1
	CAS latency=2		-		-		-		-		10		10		12			
CLK to valid output delay	CAS latency=3	t_{SAC}		4.5		5		5		6		5.4		6		6	ns	1,2
	CAS latency=2			-		-		-		-		6		6		7		
Output data hold time	CAS latency=3	t_{OH}	2		2		2.5		3		3		3		3		ns	2
	CAS latency=2		-		-		-		-		3		3		3			
CLK high pulse width		t_{CH}	2		2		2.5		3		2.5		3		3		ns	3
CLK low pulse width		t_{CL}	2		2		2.5		3		2.5		3		3		ns	3
Input setup time		t_{SS}	1.5		1.5		1.5		2		1.5		2		2		ns	3
Input hold time		t_{SH}	1		1		1		1		0.8		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	1		1		1		1		1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		4.5		5		5		6		5.4		6		6	ns	
	CAS latency=2			-		-		-		-		6		6		7		

Notes : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

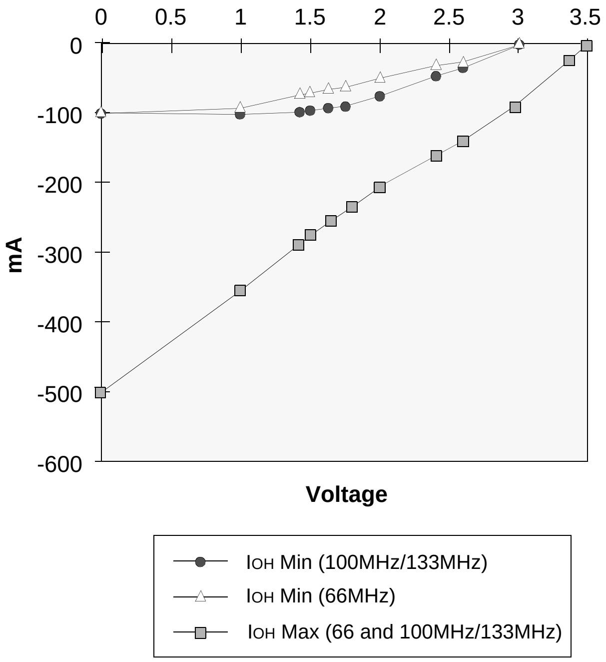
Notes : 1. Rise time specification based on 0pF + 50 Ω to V_{SS}, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to V_{DD}, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to V_{SS}.

IBIS SPECIFICATION

I_{OH} Characteristics (Pull-up)

Voltage	100MHz 133MHz Min	100MHz 133MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
3.45		-2.4	
3.3		-27.3	
3.0	0.0	-74.1	-0.7
2.6	-21.1	-129.2	-7.5
2.4	-34.1	-153.3	-13.3
2.0	-58.7	-197.0	-27.5
1.8	-67.3	-226.2	-35.5
1.65	-73.0	-248.0	-41.1
1.5	-77.9	-269.7	-47.9
1.4	-80.8	-284.3	-52.4
1.0	-88.6	-344.5	-72.5
0.0	-93.0	-502.4	-93.0

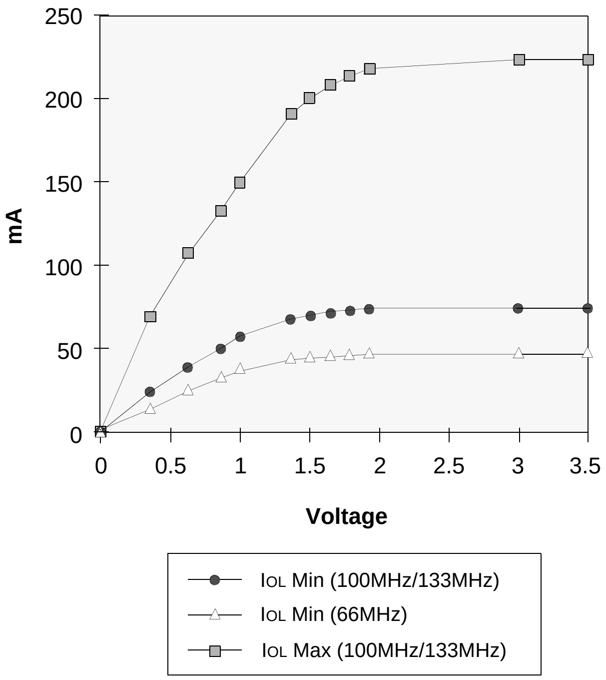
66MHz and 100MHz/133MHz Pull-up



I_{OL} Characteristics (Pull-down)

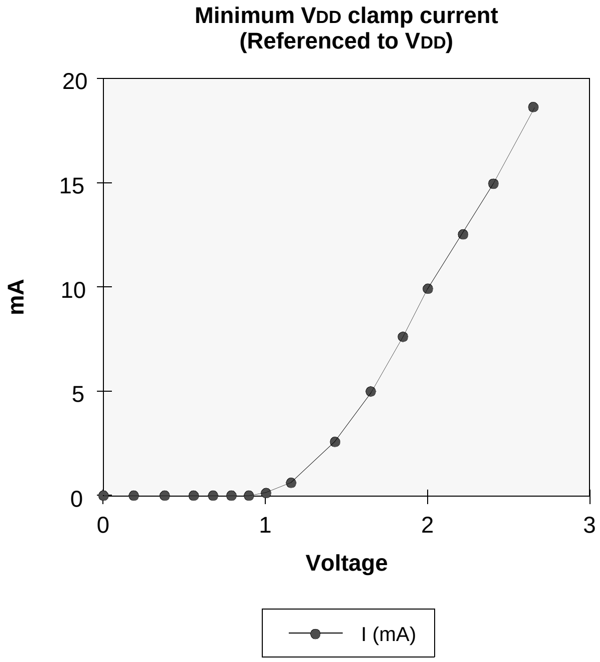
Voltage	100MHz 133MHz Min	100MHz 133MHz Max	66MHz Min
(V)	I (mA)	I (mA)	I (mA)
0.0	0.0	0.0	0.0
0.4	27.5	70.2	17.7
0.65	41.8	107.5	26.9
0.85	51.6	133.8	33.3
1.0	58.0	151.2	37.6
1.4	70.7	187.7	46.6
1.5	72.9	194.4	48.0
1.65	75.4	202.5	49.5
1.8	77.0	208.6	50.7
1.95	77.6	212.0	51.5
3.0	80.3	219.6	54.2
3.45	81.4	222.6	54.9

66MHz and 100MHz/133MHz Pull-down



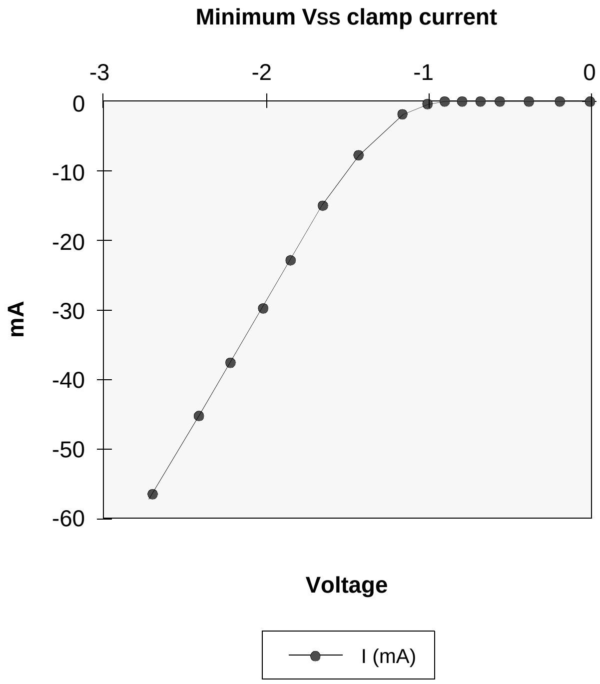
VDD Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

VDD (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31



Vss Clamp @ CLK, CKE, $\overline{\text{CS}}$, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0



SIMPLIFIED TRUTH TABLE

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, $A_9 \sim A_0$	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address ($A_0 \sim A_7$)	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don′t care, H=Logic high, L=Logic low)

Notes : 1. OP Code : Operand code
$A_0 \sim A_{11}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge command is meant by "Auto".
Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank B is selected.
If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank C is selected.
If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)