

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

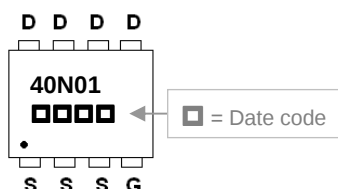
DESCRIPTION

The SPR40N01 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

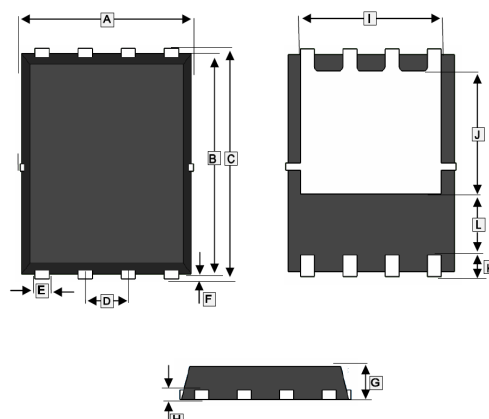
FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

MARKING



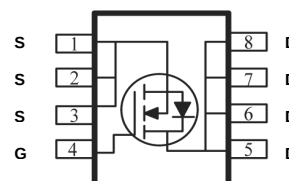
PR-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	

PACKAGE INFORMATION

Package	MPQ	Leader Size
PR-8PP	3K	13 inch



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ @ $V_{GS}=10\text{V}$	$T_C=25^\circ\text{C}$ ³	100	A
	$T_C=70^\circ\text{C}$ ³	100	
	$T_A=25^\circ\text{C}$	31	
	$T_A=70^\circ\text{C}$	25	
Pulsed Drain Current ¹	I_{DM}	400	A
Single Pulse Avalanche Energy, $L=15\text{mH}$	EAS	201	mJ
Avalanche Current, $L=15\text{mH}$	I_{AS}	63.5	A
Total Power Dissipation	$T_C=25^\circ\text{C}$	83	W
	$T_A=25^\circ\text{C}$	3.6	
Operating Junction & Storage Temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Rating			
Thermal Resistance Junction-Ambient ² (Max).	$R_{\theta JA}$	35	$^\circ\text{C} / \text{W}$
Thermal Resistance Junction-Case ² (Max).	$R_{\theta JC}$	1.5	$^\circ\text{C} / \text{W}$

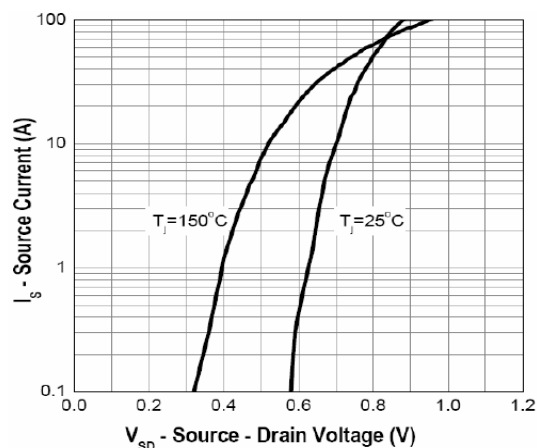
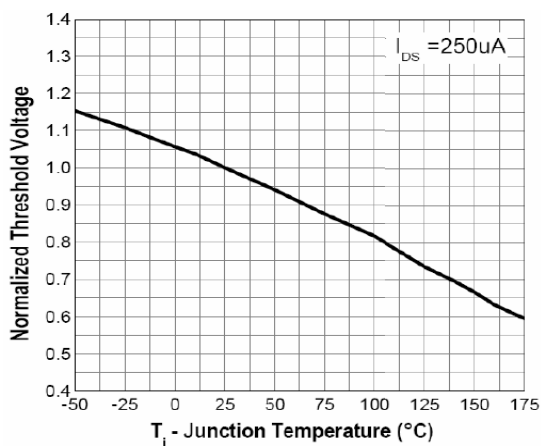
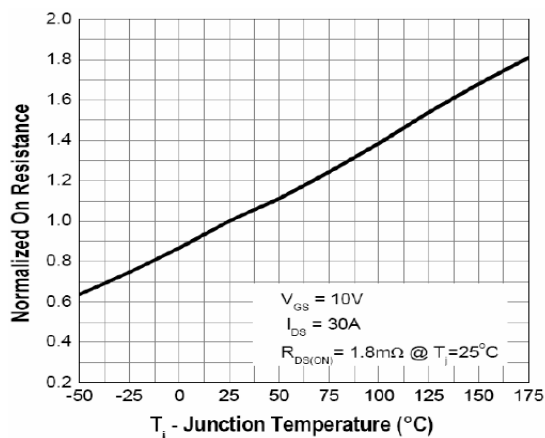
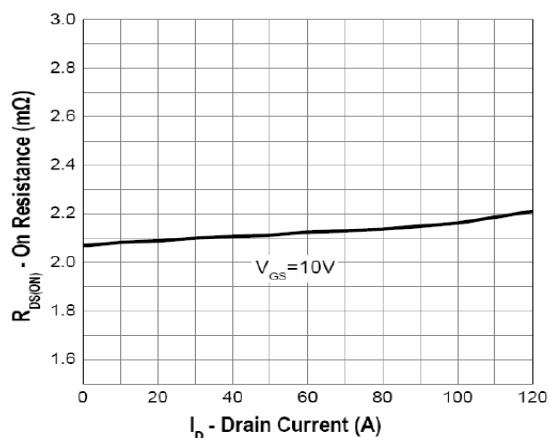
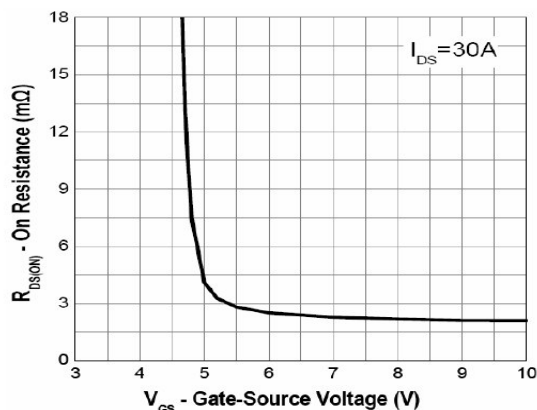
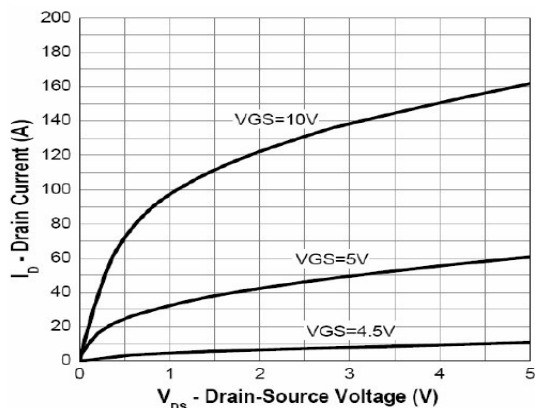
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	-	V	$V_{GS}=0, I_D=250\mu A$
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}= \pm 20V$
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	$V_{DS}=32V, V_{GS}=0, T_J=25^{\circ}C$
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	1.8	2.3	m Ω	$V_{GS}=10V, I_D=30A$
Total Gate Charge	Q_g	-	78	-	nC	$I_D=30A$ $V_{DS}=20V$ $V_{GS}=10V$
Gate-Source Charge	Q_{gs}	-	22	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	4.7	-		
Turn-on Delay Time	$T_{d(on)}$	-	21	-	nS	$V_{DS}=20V$ $I_D=30A$ $V_{GS}=10V$ $R_G=3\Omega$
Rise Time	T_r	-	6	-		
Turn-off Delay Time	$T_{d(off)}$	-	98	-		
Fall Time	T_f	-	17	-		
Input Capacitance	C_{iss}	-	4222	-	pF	$V_{GS}=0$ $V_{DS}=20V$ $f=1.0MHz$
Output Capacitance	C_{oss}	-	889	-		
Reverse Transfer Capacitance	C_{rss}	-	398	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy ⁴	EAS	110	-	-	mJ	$V_{DD}=20V, L=0.1mH, I_{AS}=47A$
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	-	-	1.3	V	$I_S=30A, V_{GS}=0V$
Reverse Recovery Time	t_{rr}	-	32	-	nS	$I_F=30A, dI/dt=100A/\mu s,$ $T_J=25^{\circ}C$
Reverse Recovery Charge	Q_{rr}	-	120	-	nC	

Note:

1. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.
3. Package Limitation current is 100A.
4. The Min. value is 100% EAS tested guarantee.

CHARACTERISTIC CURVES



CHARACTERISTIC CURVES

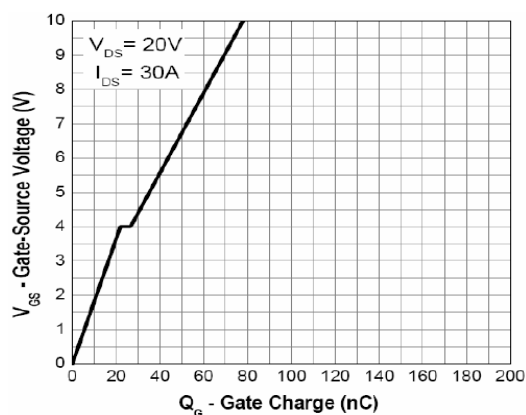


Fig.7 Gate Charge Characteristics

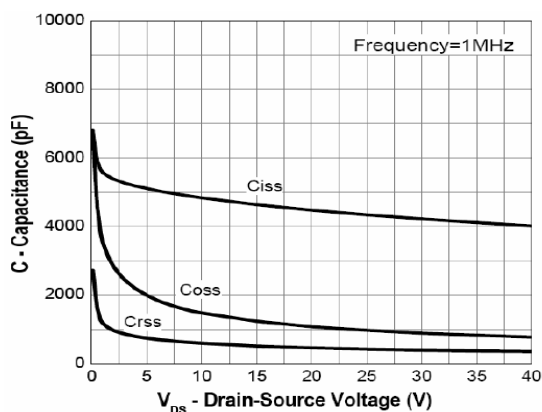


Fig.8 Capacitance Characteristic

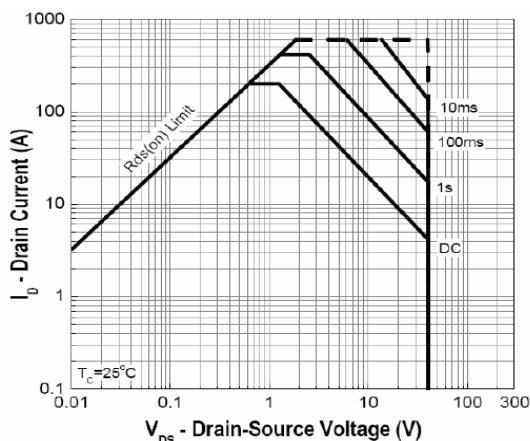


Fig.9 Safe Operating Area

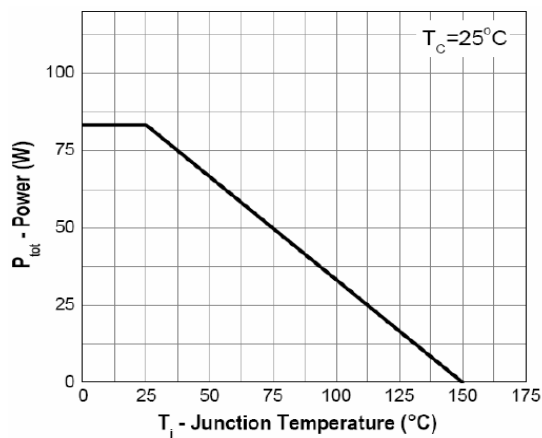


Fig.10 Power Dissipation

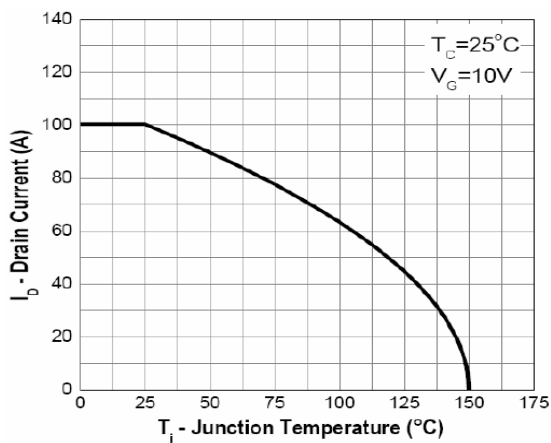


Fig.11 Drain Current vs. T_j

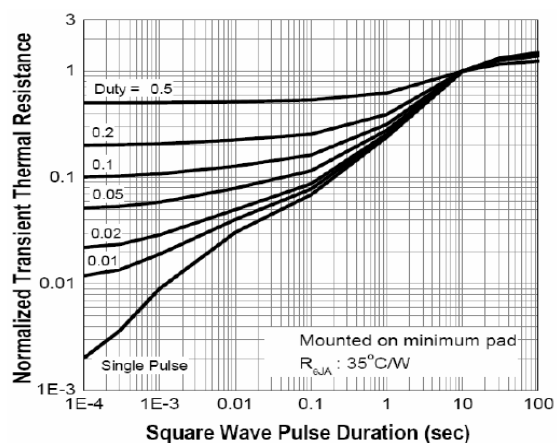


Fig.12 Transient Thermal Impedance