Triple-Supply Power Management IC for Powering FPGAs and DSPs

FEATURES

- **Two Buck Controllers Providing up to 3A and One 300mA LDO for Powering 3 Supplies**
- **Tested and Endorsed by Xilinx for Powering the Spartan™-3 and Spartan-3L FPGAs**
- **Adjustable (1.2V to 6.5V for Bucks, 0.9V to 6.5V for LDO) Output Voltages on All Channels**
- **Independent Soft-Start for Each Supply**
- **Independent Enable for Each Supply**
- **LDO Stable with Small 2.2µF Ceramic Output Cap**
- **Input Voltage Range: 2.2V to 6.5V**
- **Small, Low-Profile 4.5mm x 3.5mm x 0.9mm QFN Package**

APPLICATIONS

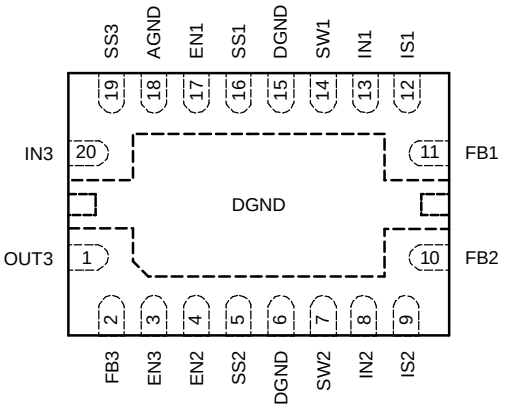
- **FPGA Supplies**
- **DSP/ASIC Supplies**
- **Split Supply Applications**

DESCRIPTION

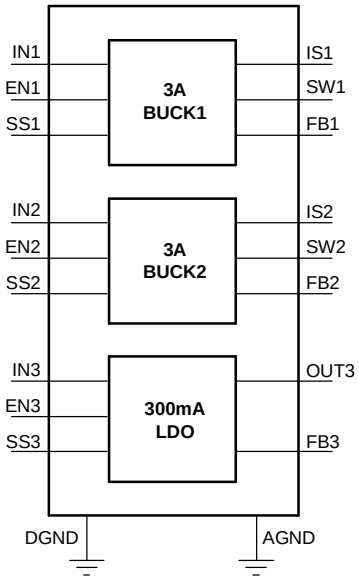
The TPS75003 is a complete power management solution for FPGA, DSP and other multi-supply applications. The device has been tested with and meets all of the Xilinx Spartan-3 and Spartan-3L start-up profile requirements, including monotonic voltage ramp and minimum voltage rail rise time. Independent Enables for each output allow sequencing to minimize demand on the power supply at start-up. Soft-start on each supply limits inrush current during start-up. Two integrated buck controllers allow efficient, cost-effective voltage conversion for both low and high current supplies such as core and I/O. A 300mA LDO is integrated to provide an auxiliary rail such as V_{CCAUX} on the Xilinx Spartan-3 FPGA. All three supply voltages are offered in user-programmable options for maximum flexibility.

The TPS75003 is fully specified from -40°C to +85°C and is offered in a QFN package, yielding a highly compact total solution size with high power dissipation capability.

PRODUCT PREVIEW



TPS75003



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	V_{OUT}	PACKAGE-LEAD DESIGNATOR	SPECIFIED TEMPERATURE RANGE, T_A	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS75003	Buck1: Adjustable Buck2: Adjustable LDO: Adjustable	4.5x3.5 QFN-20 (RHL)	-40°C to +85°C	TPS75003RHLR	Tape and Reel, 3000

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS75003	UNIT
V_{INX} range (IN1, IN2, IN3)	-0.3 to +7.0	V
V_{ENX} range (EN1, EN2, EN3)	-0.3 to V_{INX} +0.3	V
V_{SWX} range (SW1, SW2, SW3)	-0.3 to V_{INX} +0.3	V
V_{ISX} range (IS1, IS2, IS3)	-0.3 to V_{INX} +0.3	V
V_{OUT3} range	-0.3 to +7.0	V
V_{SSX} range (SS1, SS2, SS3)	-0.3 to V_{INX} +0.3	V
V_{FBX} range (FB1, FB2, FB3)	-0.3 to +3.3	V
Peak LDO output current (I_{OUT3})	Internally limited	—
Continuous total power dissipation	See Dissipation Ratings Table	—
Junction temperature range, T_J	-55 to +150	°C
Storage temperature range	-65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

BOARD	$R_{\Theta JC}$	$R_{\Theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \leq 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Reference Layout(1)	—	—	—	—	—	—

(1) Refer to *PCB Layout* section. Internal power dissipation limits are determined by LDO operation: $P_{DISS} = (V_{IN3} - V_{OUT3}) \times I_{OUT3}$.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = V_{IN3} = 3.0V$, $V_{OUT1} = V_{OUT2} = V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = 25°C$.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply and Logic						
V_{INX}	Input Voltage Range (IN1, IN2, IN3)(1)		2.2		6.5	V
I_Q	Quiescent Current, $I_Q = I_{DGND} + I_{AGND}$	$I_{OUT1} = I_{OUT2} = 0mA$, $I_{OUT3} = 1mA$		100	150	µA
I_{SHDN}	Shutdown Supply Current	$V_{EN1} = V_{EN2} = V_{EN3} = 0V$		0.3	3.0	µA
V_{IHX}	Enable High, enabled (EN1, EN2, EN3)		1.3		V_{INX}	V
V_{ILX}	Enable Low, shutdown (EN1, EN2, EN3)		0		0.3	V
I_{ENX}	Enable pin current (EN1, EN2, EN3)			0.01	0.5	µA
Buck Controllers 1 and 2						
$V_{OUT1,2}$	Adjustable Output Voltage Range(2)		V_{FBX}		V_{INX}	V
$V_{FB1,2}$	Feedback Voltage (FB1, FB2)			1.2		V
	Feedback Voltage Accuracy(1) (FB1, FB2)	$2.8V \le V_{IN1,2} \le 6.5V$	-4		+4	%
$I_{FB1,2}$	Current into FB1, FB2 pins			0.01	0.5	µA
$V_{IS1,2}$	Reference Voltage for Current Sense		90	105	120	mV
$I_{IS1,2}$	Current into IS1, IS2 Pins			0.01	0.5	µA
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation(1)	Measured with the circuit in Figure 1, $V_{OUT} + 0.5V \le V_{IN} \le 6.5V$		0.6		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	Measured with the circuit in Figure 1, $1mA \le I_{OUT} \le 2A$		0.6		% / A
$n_{1,2}$	Efficiency(3)	Measured with the circuit in Figure 1, $I_{OUT} = 1A$		94		%
$t_{STR1,2}$	Startup Time(3)	Measured with the circuit in Figure 1, $R_L = 6\Omega$, $C_{OUT} = 100\mu F$, $C_{SS} = 2.2nF$		5		ms
$R_{DS,ON1,2}$	Gate Driver P-Channel MOSFET On-Resistance	$V_{IN1,2} > 2.5V$		4		Ω
		$V_{IN1,2} = 2.2V$		6		
$R_{DS,ON1,2}$	Gate Driver N-Channel MOSFET On-Resistance	$V_{IN1,2} > 2.5V$		4		Ω
		$V_{IN1,2} = 2.2V$		6		
$I_{SW1,2}$	Minimum Gate Drive Current			***TBD***		mA
t_{ON}	Minimum On Time		1.36	1.6	1.84	µs
t_{OFF}	Minimum Off Time		0.44	0.55	0.86	µs
LDO						
V_{OUT3}	Output Voltage Range		1.0		6.5 - V_{DO}	V
V_{FB3}	Feedback Pin Voltage			0.507		V
	Feedback Pin Voltage Accuracy(1)	$2.85V \le V_{IN3} \le 6.5V$, $1mA \le I_{OUT3} \le 300mA$	-4.0		+4.0	%
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation(1)	$V_{OUT3} + 0.5V \le V_{IN3} \le 6.5V$		0.75		% / V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	$10mA \le I_{OUT3} \le 300mA$		0.01		% / mA

(1) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2V, whichever is greater.
(2) Maximum V_{OUT} is dependent on external components and will be less than V_{IN}.
(3) Depends on external components.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = V_{IN3} = 3.0V$, $V_{OUT1} = V_{OUT2} = V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = 25°C$.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
LDO, *continued*						
V_{DO}	Dropout Voltage ($V_{IN} = V_{OUT(NOM)} - 0.1$)(4)	I_{OUT3} = 300mA, 2.2V ≤ V_{IN3} < 6.5		175	300	mV
I_{CL3}	Current Limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$	375	625	1000	mA
I_{FB3}	Current into FB3 pin			0.01	0.1	µA
V_n	Output Noise	BW = 100Hz - 100kHz, I_{OUT3} = 300mA		400		μV_{RMS}
PSRR	Power-Supply Rejection Ratio	f = 1kHz		***TBD***		dB
		f = 10kHz		***TBD***		
t_{SD}	Thermal Shutdown Temperature for LDO	Shutdown, Temp Increasing		175		°C
		Reset, Temp Decreasing		160		

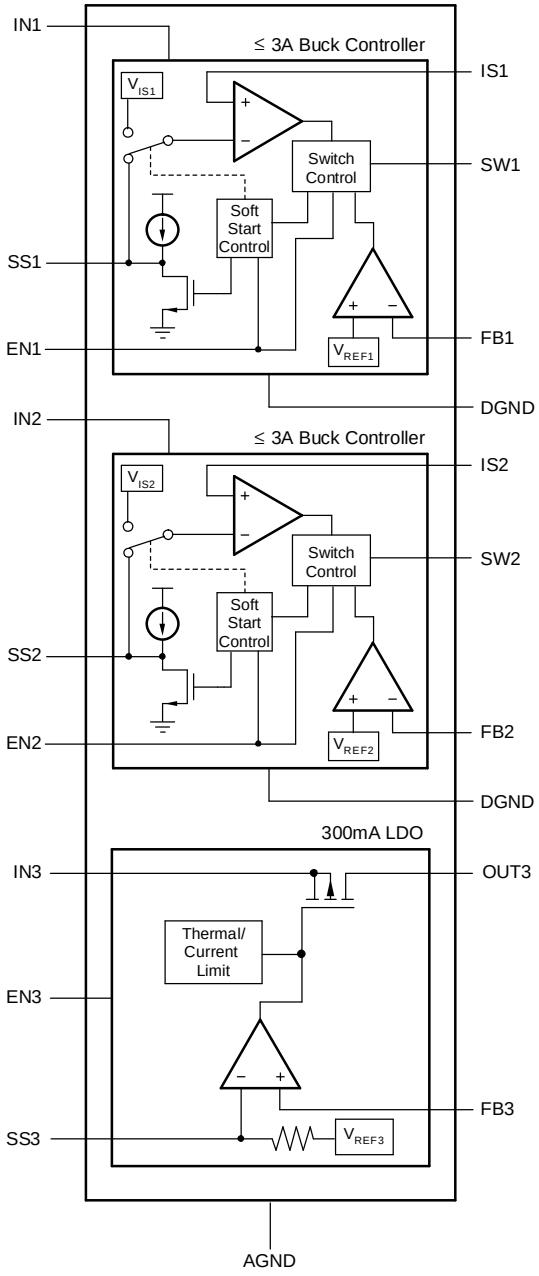
(4) V_{DO} does not apply when $V_{OUT} + V_{DO} < 2.2V$.

PRODUCT PREVIEW

DEVICE INFORMATION

Functional Block Diagram

TPS75003



PRODUCT PREVIEW

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	RHL	
DGND	6, 15, PAD	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the *PCB Layout* section of this data sheet.
AGND	18	Ground connection for LDO.
IN1	13	Input supply to BUCK1.
IN2	8	Input supply to BUCK2.
IN3	20	Input supply to LDO.
EN1	17	Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.
EN2	4	Same as EN1 but for BUCK2 controller.
EN3	3	Same as EN1 but for LDO.
SS1	16	Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important. See *Applications* and *PCB Layout* sections for details.
SS2	5	Same as SS1 but for BUCK2 regulator.
SS3	19	Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, therby slowing output voltage ramp-up. See *Applications* section for details.
IS1	12	Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required. See *Applications* section for details.
IS2	9	Same as IS1 but compared to IN2 and used for BUCK2 controller.
SW1	14	Gate drive pin for external BUCK1 P-channel MOSFET.
SW2	7	Same as SW1 but for BUCK2 controller.
FB1	11	Feedback pin. Used to set the output voltage of BUCK1 regulator.
FB2	10	Same as FB1 but for BUCK2 controller.
FB3	2	Same as FB1 but for LDO.
OUT3	1	Regulated LDO output. A small ceramic capacitor (≥ 2.2μF) is needed from this pin to ground to ensure stability.

PRODUCT PREVIEW

Typical Application Circuit for Powering the Xilinx Spartan-3 FPGA

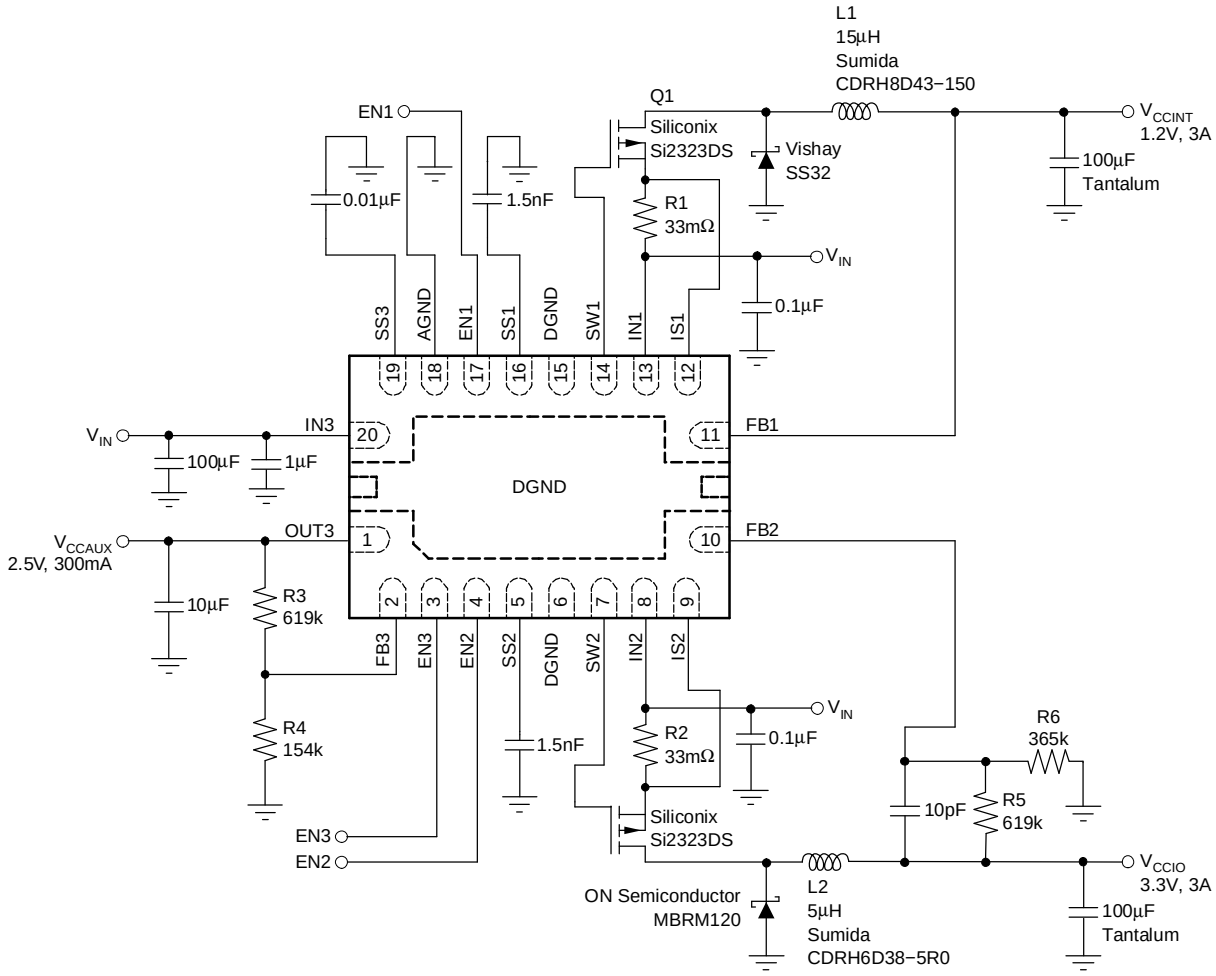


Figure 1.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

Measured using circuit in Figure 1

Buck Converter

BUCK LOAD REGULATION

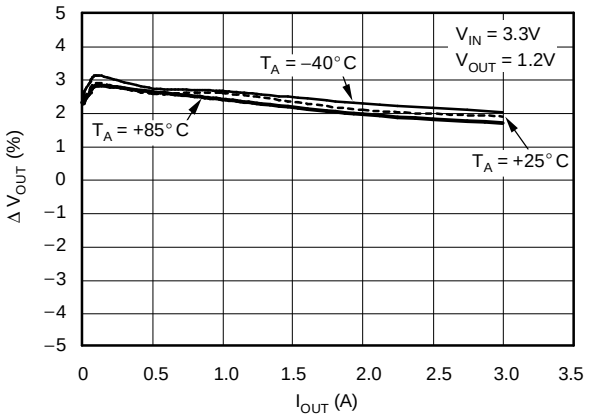


Figure 2.

BUCK LOAD REGULATION

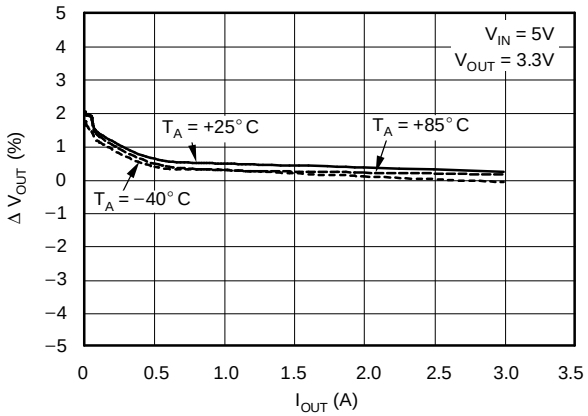


Figure 3.

BUCK LINE REGULATION

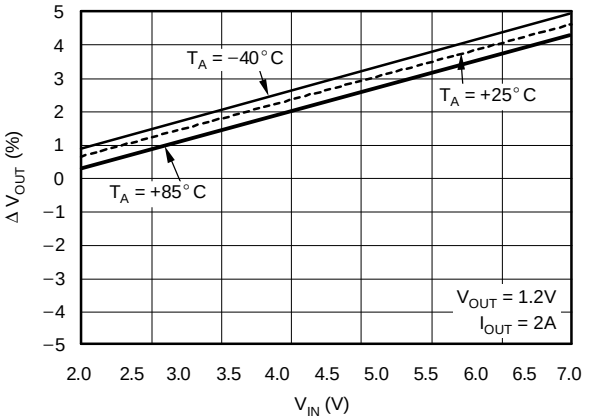


Figure 4.

BUCK LINE REGULATION

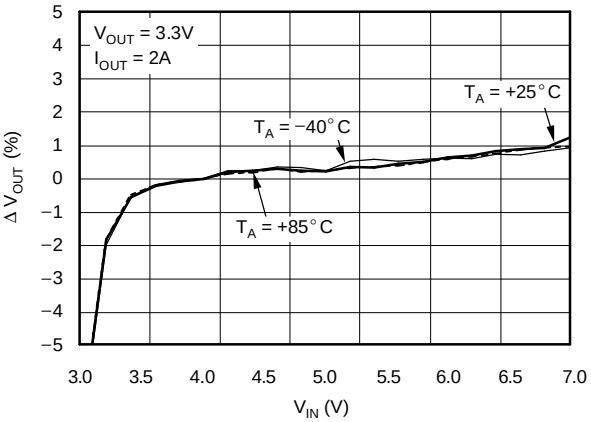


Figure 5.

BUCK SWITCHING FREQUENCY vs I_{OUT}, T_A

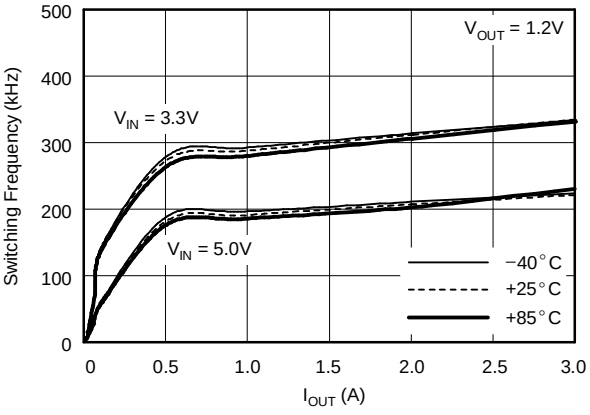


Figure 6.

BUCK SWITCHING FREQUENCY vs I_{OUT}

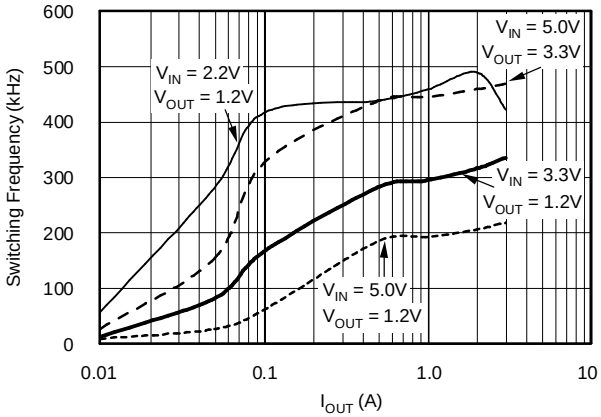


Figure 7.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1

BUCK OUTPUT VOLTAGE RIPPLE

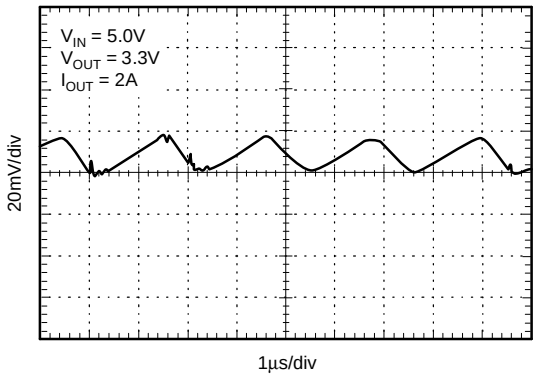


Figure 8.

EFFICIENCY vs I_{OUT}

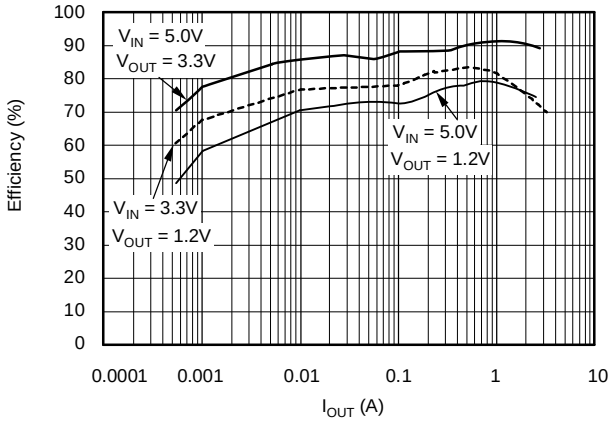


Figure 9.

BUCK START-UP vs V_{IN} and I_{OUT}

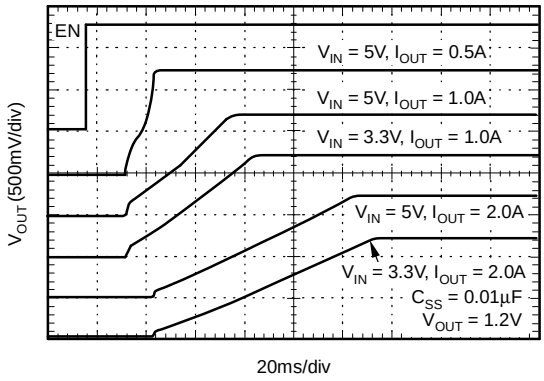


Figure 10.

BUCK START-UP vs V_{IN} and C_{OUT}

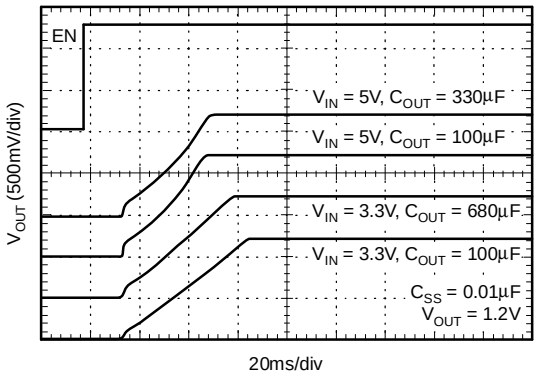


Figure 11.

BUCK START-UP vs V_{IN} and C_{SS}

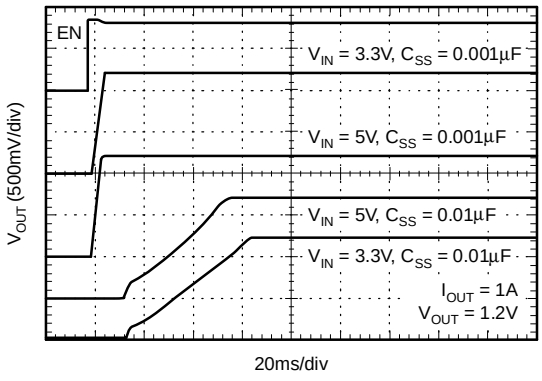


Figure 12.

BUCK START-UP vs I_{OUT} and C_{SS}

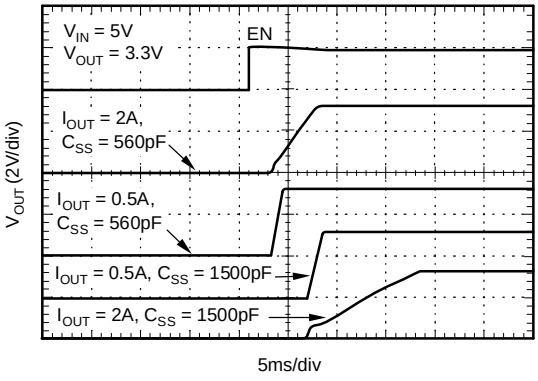


Figure 13.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1

BUCK START-UP vs V_{IN} and R_{SENSE}

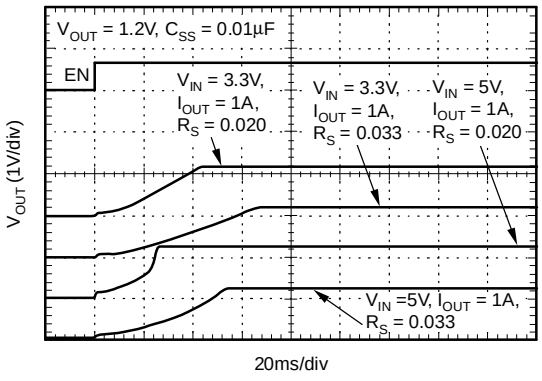


Figure 14.

LDO Converter

LDO LOAD REGULATION

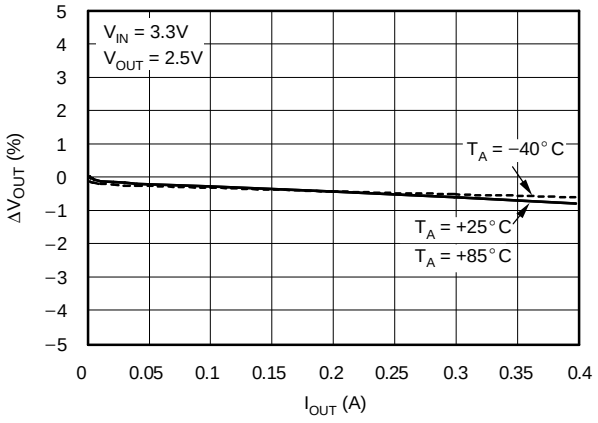


Figure 15.

LDO LINE REGULATION

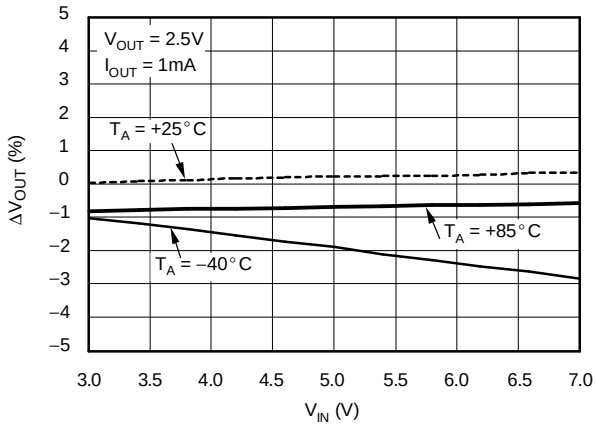


Figure 16.

LDO DROPOUT vs I_{OUT}

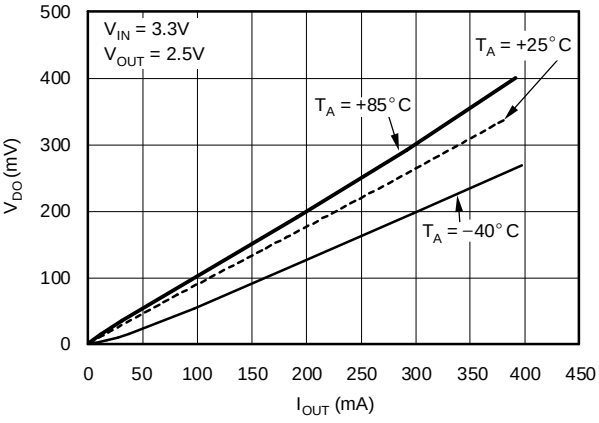


Figure 17.

LDO DROPOUT vs T_A

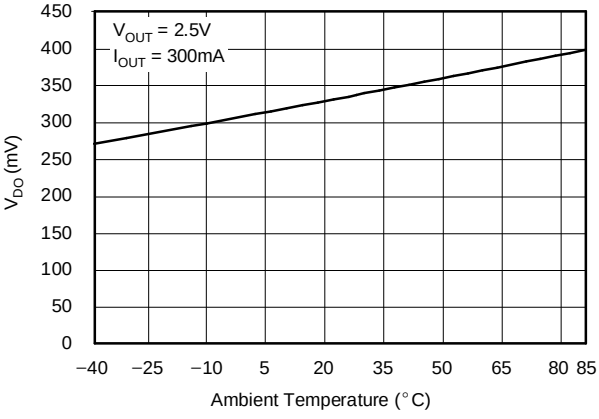


Figure 18.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

Measured using circuit in Figure 1

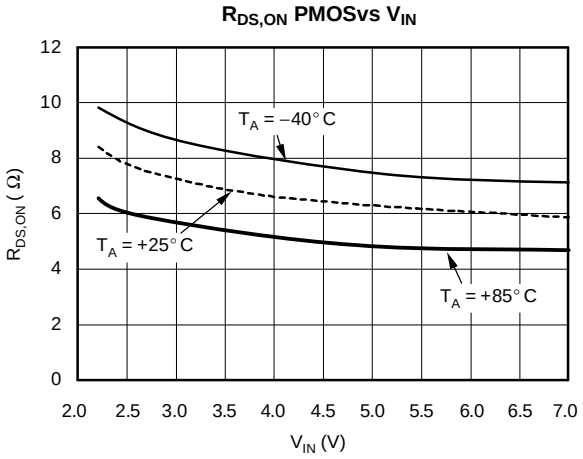


Figure 19.

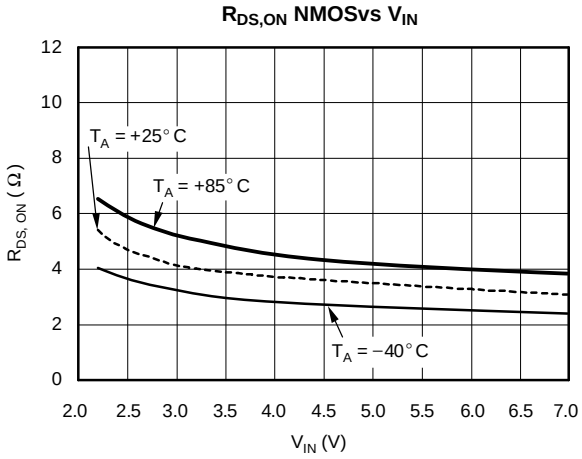


Figure 20.

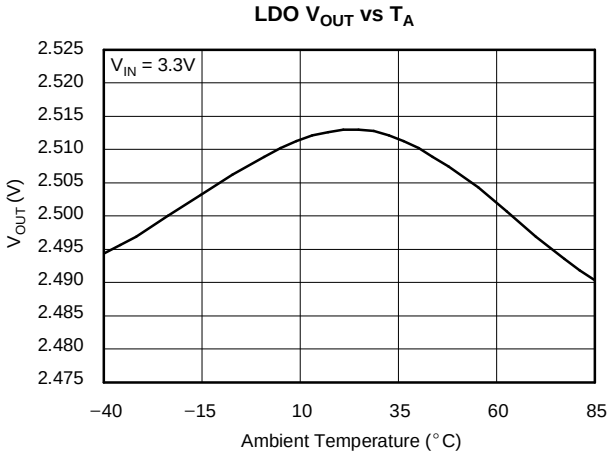


Figure 21.

PRODUCT PREVIEW

APPLICATION INFORMATION

The TPS75003 is an integrated power management IC designed specifically to power DSPs and FPGAs such as the Xilinx Spartan-3 and Spartan-3L. Two non-synchronous buck controllers can be configured to supply up to 3A for both CORE and I/O rails. A low dropout linear regulator powers auxiliary rails up to 300mA. All channels have independent enable and soft-start, allowing control of inrush current and output voltage ramp time as required by the application.

Figure 1 shows a typical application circuit for powering the Xilinx Spartan-3 FPGA. Table 1 shows component values that have been tested for use with 2A and 3A load currents. Other similar external components can be substituted as desired; however, in all cases the circuits that are used should be tested for compliance to application requirements.

Table 1. Components Tested for 1A and 3A Load Circuits

DATA	FORTHCOMING
FORTHCOMING	DATA
DATA	FORTHCOMING

OPERATION (BUCK CONTROLLERS)

Channels 1 and 2 contain two identical non-synchronous buck controllers that use minimum on-time/minimum off-time hysteretic control. (Refer to Figure 1.) For clarity, BUCK1 is used throughout the discussion of device operation. When V_{OUT1} is below its target, an external PMOS (Q1) is turned on for at least the minimum on-time, increasing current through the inductor (L1) until V_{OUT1} reaches its target value or the current limit (set by R1) is reached. Once either of these conditions is met, the PMOS is switched off for at least the minimum off-time of the device. After the minimum off-time has passed, the output voltage is monitored and the switch is turned on again when necessary.

When output current is low, the buck controllers operate in discontinuous mode. In this mode, each switching cycle begins at zero inductor current, rises to a maximum value, then falls back to zero current. When current reaches zero on the falling edge, ringing occurs at the resonant frequency of the inductor and stray switch node capacitance. This is normal operation; it does not affect circuit performance, and can be minimized if desired by using an RC snubber and/or a resistor in series with the gate of the PMOS, as shown in Figure 22.

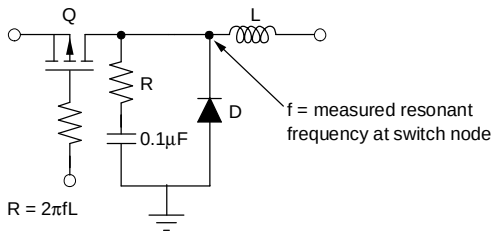


Figure 22. RC Snubber and Series Gate Resistor Used to Minimize Ringing

At higher output currents, the TPS75003 operates in continuous mode. In continuous mode, there is no ringing at the switch node and V_{OUT} is equal to V_{IN} times the duty cycle of the switching waveform.

When V_{IN} approaches or falls below V_{OUT}, the buck controllers operate in 100% duty cycle mode, fully turning on the external PMOS to allow regulation at lower dropout than would otherwise be possible.

Enable (Buck Controllers)

The enable pins (EN1 and EN2) for the buck controllers are active high. When the enable pin is driven low and input voltage is present at IN1 or IN2, an on-chip FET is turned on to discharge the soft-start pin SS1 or SS2, respectively. If the soft-start feature is being used, enable should be driven high at least 10µs after V_{IN} is applied to ensure this discharge cycle occurs.

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UVLO (Buck Controllers)

An under-voltage lockout circuit is present to prevent turning on the external PMOS (Q1 or Q2) until a reliable operating voltage is reached on the appropriate regulator (IN1 or IN2). This prevents the buck controllers from mis-operation at low input voltages.

Current Limit (Buck Controllers)

An external resistor (R1 or R2) is used to set the current limit for the external PMOS transistor (Q1 or Q2). These resistors are connected between IN1 and IS1 (or IN2 and IS2) to provide a reference voltage across these pins that is proportional to the current flowing through the PMOS transistor. This reference voltage is compared to an internal reference to determine if an over-current condition exists. When current limit is exceeded, the external PMOS is turned off for the minimum off-time. Current limit detection is disabled for 10ns any time the PMOS is turned on to avoid triggering on switching noise. In 100% duty cycle mode, current limit is always enabled. Current limit is calculated using the V_{IS1} or V_{IS2} specification in the *Electrical Characteristics* section, shown in Equation 1:

$$I_{LIMIT} = \frac{V_{IS1,2}}{R_{1,2}} \quad (1)$$

The current limit resistor must be appropriately rated for the dissipated power determined by its RMS current calculated by Equation 2:

$$I_{RMS} = I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

$$P_{DISS} = (I_{RMS})^2 \cdot R \quad (2)$$

For low-cost applications the $I_{S1,2}$ pin can be connected to the drain of the PMOS, using $R_{DS,ON}$ instead of R1 or R2 to set current limit. Variations in the PMOS $R_{DS,ON}$ must be taken into account to ensure that current limit will protect external components such as the inductor, the diode, and the switch itself from damage as a result of over-current.

Short-Circuit Protection (Buck Controllers)

In an overload condition, the current rating of the external components (PMOS, diode, and inductor) can be exceeded. To help guard against this, the TPS75003 increases its minimum off-time when the voltage at the feedback pin is lower than the reference voltage. When the output is shorted (V_{FB} is zero), minimum off-time is increased to approximately 4µs. The increase in off-time is proportional to the difference between the voltage at the feedback pin and the internal reference.

Soft-Start (Buck Controllers)

The buck controllers each have independent soft-start capability to limit inrush during start-up and to meet timing requirements of the Xilinx Spartan-3 FPGA. Limiting inrush current by using soft-start, or by staggering the turn-on of power rails, also guards against voltage drops at the input source due to its output impedance. Refer to the soft-start circuitry shown in Figure 23 and the soft-start timing diagram shown in Figure 24. BUCK 1 will be discussed in this section; it is identical to BUCK2. Note that pins SS1 and SS2 are very high-impedance and cannot be probed using a typical oscilloscope setup. When input voltage is applied at IN1 and EN1 is driven low, any charge on the SS pin is discharged by an on-chip pull-down transistor. When EN1 is driven high, an on-chip current source starts charging the external soft-start capacitor C_{SS1}. The voltage on the capacitor is compared to the voltage across the current sense resistor R1 to determine if an over-current condition exists. If the voltage drop across the sense resistor goes above the reference voltage, then the external PMOS is shut off for the minimum off-time. This implementation provides a cycle-by-cycle current limit and allows the user to program the soft-start time over a wide range for most applications. For detailed information on choosing C_{SS1} and C_{SS2}, see the section, *Selecting the Soft-Start Cap.*

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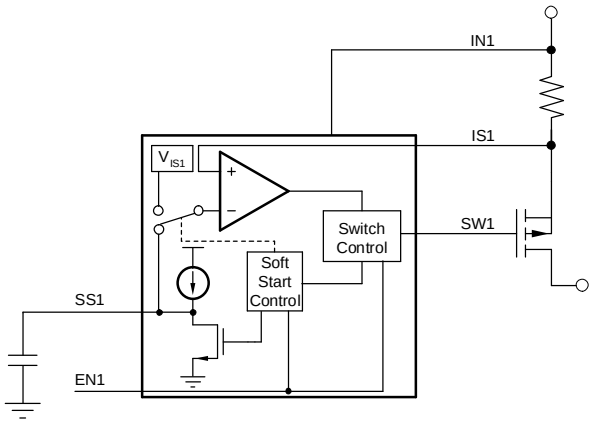

Figure 23. Soft-Start Circuitry

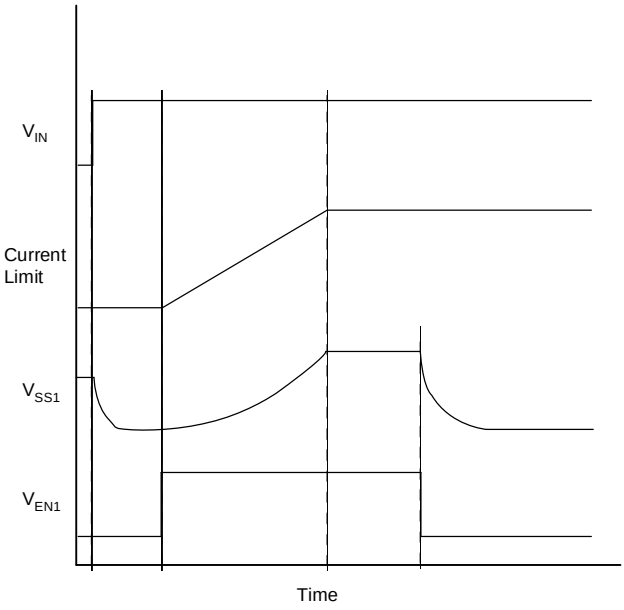

Figure 24. Soft-Start Timing Diagram

Input Capacitor C_{IN1}, C_{IN2} Selection (Buck Controllers)

It is good analog design practice to place input capacitors near the inputs of the device in order to ensure a low impedance input supply. 10µF to 22µF of capacitance for each buck converter is adequate for most applications, and should be placed within 100mils (0.001in) of the IN1 and IN2 pins to minimize the effects of pulsed current switching noise on the soft-start circuitry during the first ~1V of output voltage ramp. Low ESR capacitors also help to minimize noise on the supply line. The minimum value of capacitance can be estimated using Equation 3:

$$C_{IN,\,MIN} = \frac{(1/2)L \times (\Delta I_L)^2}{V_{(RIPPLE)} \times V_{IN}} \approx \frac{(1/2)L \times (0.3 \times I_{OUT})^2}{V_{(RIPPLE)} \times V_{IN}} \quad (3)$$

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Note that the capacitors must be able to handle the RMS current in continuous conduction mode, which can be calculated using Equation 4:

$$I_{C,IN(RMS)} \approx I_{OUT} \sqrt{\left(\frac{V_{OUT}}{V_{IN,MIN}}\right)} \quad (4)$$

Inductor Value Selection (Buck Controllers)

The inductor is chosen based on inductance value and maximum current rating. Larger inductors reduce current ripple (and therefore, output voltage ripple) but are physically larger and more expensive. Inductors with lower DC resistance typically improve efficiency, but also have higher cost and larger physical size. The buck converters work well with inductor values between 4.7µF and 47µF in most applications. When selecting an inductor, the current rating should exceed the current limit set by R_{IS} or $R_{DS,ON}$ (see *Current Limit* section). To determine the minimum inductor size, first determine if the device will operate in minimum on-time or minimum off-time mode. The device will operate in minimum on-time mode if Equation 5 is satisfied:

$$V_{IN} - V_{OUT} - I_{OUT} \times r_{DS(on)} - R_L \times I_{OUT} \geq \frac{t_{(OFF,min)} \times \left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT}\right)}{t_{ON,MIN}} \quad (5)$$

where R_L = the inductor's DC resistance.

Minimum inductor size needed when operating in minimum on-time mode is given by Equation 6:

$$L_{MIN} = \frac{\left(V_{IN} - V_{OUT} - I_{OUT} \times r_{DS(on)} - R_L \times I_{OUT}\right) \times t_{ON,MIN}}{\Delta I} \quad (6)$$

Minimum inductor size needed when operating in minimum off-time mode is given by Equation 7:

$$L_{MIN} = \frac{\left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT}\right) \times t_{OFF,MIN}}{\Delta I} \quad (7)$$

External PMOS Transistor Selection (Buck Controllers)

The external PMOS transistor is selected based on threshold voltage (V_T), on-resistance ($R_{DS,ON}$), gate capacitance (C_G) and voltage rating. The PMOS V_T magnitude must be much lower than the lowest voltage at IN1 or IN2 that will be used. A V_T magnitude that is 0.5V less than the lowest input voltage is normally sufficient. The PMOS gate will see voltages from 0V to the maximum input voltage, so gate-to-source breakdown should be a few volts higher than the maximum input supply. The drain-to-source of the device will also see this full voltage swing, and should therefore be a few volts higher than the maximum input supply. The RMS current in the PMOS can be estimated by using Equation 8:

$$I_{PMOS(RMS)} \approx I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}} \quad (8)$$

The power dissipated in the PMOS is comprised of both conduction and switching losses. Switching losses are typically insignificant. The conduction losses are a function of the RMS current and the $R_{DS,ON}$ of the PMOS, and are calculated by Equation 9:

$$P_{(cond)} = \left(I_{OUT}\sqrt{D}\right)^2 \times r_{DS(on)} \times \left(1 + TC \times \left[T_J - 25^\circ C\right]\right) \approx \left(I_{OUT}\sqrt{D}\right) \times r_{DS(on)} \quad (9)$$

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Diode Selection (Buck Controllers)

The diode is off when the PMOS is on, and on when the PMOS is off. Since it will be turned on and off at a relatively high frequency, a Schottky diode is recommended for good performance. The peak current rating of the diode should exceed the peak current limit set by the sense resistor $R_{IS1,2}$. A diode with low reverse leakage current and low forward voltage at operating current will optimize efficiency. Equation 10 calculates the estimated average power dissipation:

$$I_{(diode)(RMS)} \approx I_{OUT}(1-D) = I_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

Output Capacitor Selection (Buck Controllers)

The output capacitor is selected based on output voltage ripple and transient response requirements. As a result of the nature of the hysteretic control loop, a minimum ESR of a few tens of mΩ should be maintained for good operation unless a feed-forward resistor is used. Low ESR bulk tantalum or PosCap capacitors work best in most applications. A 1.0µF ceramic capacitor can be used in parallel with this capacitor to filter higher frequency spikes. The output voltage ripple can be estimated by Equation 11:

$$\Delta V_{PP} = \Delta I \times \left[ESR + \left(\frac{1}{8 \times C_{OUT} \times f}\right)\right] \approx 1.1\Delta I \times ESR \quad (11)$$

To calculate the capacitance needed to achieve a given voltage ripple as a result of a load transient from zero output to full current, use Equation 12:

$$C_{OUT} = \frac{L \times \Delta I_{OUT}^{2}}{(V_{IN}-V_{OUT}) \times \Delta V} \quad (12)$$

If only ceramic or other very low ESR output capacitor configurations are desired, additional voltage ripple must be passed to the feedback pin. This can be accomplished by using the application circuit in Figure 1. Resistor R_{1B} adds additional control signal to the feedback loop. This circuit works best with R_{1B} = 2 to 4 x R_{1A}. If R_{1B} is too low, the output shows worse load regulation. R_{1A} and R_{1B} can be calculated using Equation 13:

$$R1 = \frac{1}{\frac{1}{R1_A}+\frac{1}{R1_B}} \text{ and } R1_B = \frac{1}{\frac{1}{R1}-\frac{1}{R1_A}} \quad (13)$$

Use Equation 14 to calculate $R1_A$ if $R1_B = (4)(R1_A)$:

$$R1_A = \frac{5}{4}R1 \quad (14)$$

Output Voltage Ripple Effect on V_{OUT} (Buck Controllers)

Output voltage ripple causes V_{OUT} to be higher or lower than the target value by half of the peak-to-peak voltage ripple. For minimum on-time, the ripple adds to the voltage; for minimum off-time, it subtracts from the voltage.

Soft-Start Capacitor Selection (Buck Controllers)

BUCK1 is discussed in this section; it is identical to BUCK2. Soft-start is implemented on the buck controllers by ramping current limit from 0 to its target value (set by R1) over a user-defined time. This time is set by the external soft-start cap connected to pin SS1. If SS1 is left open, a small on-chip capacitor will provide a current limit ramp time of approximately 250µs. Figure 25 shows the effects of R1 and SS1 on the current limit start-up ramp.

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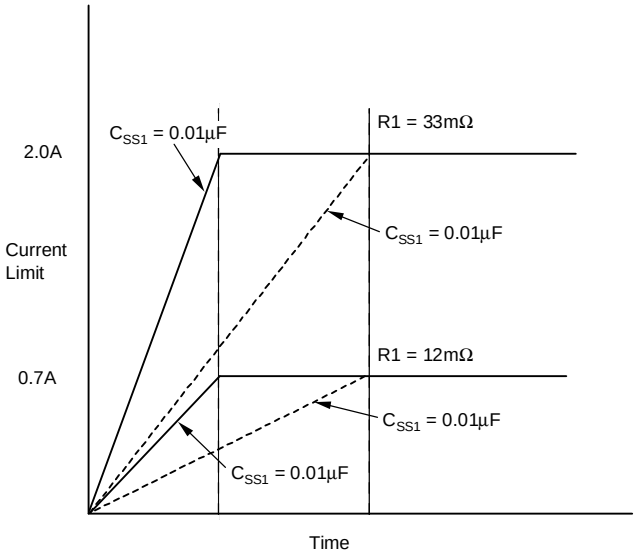

Figure 25. Effects of C_{SS1} and R_1 on Current Ramp Limit

This soft-start current limit ramo can be used to provide inrush current control or output voltage ramp control. While the current limit ramp can be easily understood by looking at Figure 25, the output voltage ramp is a complex function of many variables. The dominant variables in this process are V_{OUT1}, C_{SS1}, I_{OUT1}, and R_1. Less important variables are V_{IN1} and L_1.

The best way to set a target start-up time is through bench measurement under target conditions, adjusting C_{SS1} to get the desired startup profile. To stay above a minimum start-up time, set the nominal start-up time to approximately five times the minimum. To stay below a maximum time, set the nominal start-up time at one-fifth of the maximum. Fastest start-up times occur at maximum V_{IN1}, with minimum V_{OUT1}, L_1, C_{OUT1}, C_{SS1}, and I_{OUT1}. Slowest start-up times occur under opposite conditions.

Refer to Figure 10 to Figure 14 for characterization curves showing how the start-up profile is affected by these critical parameters.

Output Voltage Setting Selection (Buck Controllers)

Output voltage is set using two resistors as shown for Buck2 in Figure 1. Output voltage is then calculated using Equation 15:

$$V_{OUT} = V_{FB}\left(\frac{R_5}{R_6} + 1\right) \quad (15)$$

where V_{FB} = 1.24V.

LDO OPERATION

The TPS75003 LDO uses a PMOS pass element and is offered in an adjustable version for ease of programming to any output voltage. When used to power $V_{CC,AUX}$ it is set to 2.5V; it can optionally be set to other output voltages to power other circuitry. The LDO has integrated soft-start, independent enable, and short-circuit and thermal protection. The LDO can be used to power $V_{CC,AUX}$ on the Xilinx Spartan-3 FPGA when 3.3V JTAG signals are used as described in Application Note SLVA159 (available for download from www.ti.com).

Input Capacitor Selection (LDO)

Although an input capacitor is not required, it is good analog design practice to connect a 0.1µF to 10µF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, stability, and ripple rejection. A higher value capacitor may be needed if large, fast rise-time load transients are anticipated, or if the device is located far from its power source.

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Output Capacitor Selection (LDO)

A 2.2µF or greater capacitor is required near the output of the device to ensure stability. The LDO is stable with any capacitor type, including ceramic. If improved transient response or ripple rejection is required, larger and/or lower ESR output capacitors can be used.

Soft-Start (LDO)

The LDO uses an external soft-start capacitor, C_{SS3}, to provide an RC-ramped reference voltage to the control loop. (See the Functional Block Diagram.) This is a voltage-controlled soft-start, as compared to the current-controlled soft-start used by the buck controllers.

Setting Output Voltage (LDO)

Output voltage is set using two resistors as shown in Figure 1. Output voltage is then calculated using Equation 16:

$$V_{OUT} = V_{FB}\left(\frac{R_3}{R_4} + 1\right) \quad (16)$$

where V_{FB} = 0.507V.

Internal Current Limit (LDO)

The internal current limit of the LDO helps protect the regulator during fault conditions. When an over-current condition is detected, the output voltage will be reduced until the current falls to a level that will not damage the device. For good device reliability, the LDO should not operate at current limit.

Enable Pin (LDO)

The active high enable pin (EN3) can be used to put the device into shutdown mode. If shutdown and soft-start capability are not required, EN3 can be tied to IN3.

Dropout Voltage (LDO)

The LDO uses a PMOS transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the pass device is in its linear region of operation, and the input-output resistance is the $R_{DS,ON}$ of the pass transistor. In this region, the regulator is said to be out of regulation; ripple rejection, line regulation, and load regulation degrade as (V_{IN} – V_{OUT}) falls much below 0.5V.

Transient Response (LDO)

The LDO does not have an on-chip pull-down circuit for output is over-voltage conditions. This feature permits applications that connect higher voltage sources such as an alternate power supply to the output. This design also results in an output overshoot of several percent if the load current quickly drops to zero. The amplitude of overshoot can be reduced by increasing C_{OUT}; the duration of overshoot can be reduced by adding a load resistor.

Thermal Protection (LDO)

Thermal protection disables the output when the junction temperature, T_J, reaches unsafe levels. When the junction cools, the output is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage. For good long term reliability, the device should not be continuously operated at or near thermal shutdown.

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Power Dissipation (LDO)

The TPS75003 comes in a QFN-style package with an exposed lead frame on the package underside. The exposed lead frame is the primary path for removing heat and should be soldered to a PC board that is configured to remove the amount of power dissipated by the LDO, as calculated by Equation 17:

$$P_D = \left(V_{IN3} - V_{OUT3}\right) \times I_{OUT3} \quad (17)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage. The two buck converters do not contribute a significant amount of dissipated power. Using heavier copper will increase the overall effectiveness of removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

PCB Layout Considerations

As with any switching regulators, careful attention must be paid to board layout. A typical application circuit and corresponding recommended printed circuit board (PCB) layout with emphasis on the most sensitive areas are shown in Figure 26 through Figure 28.

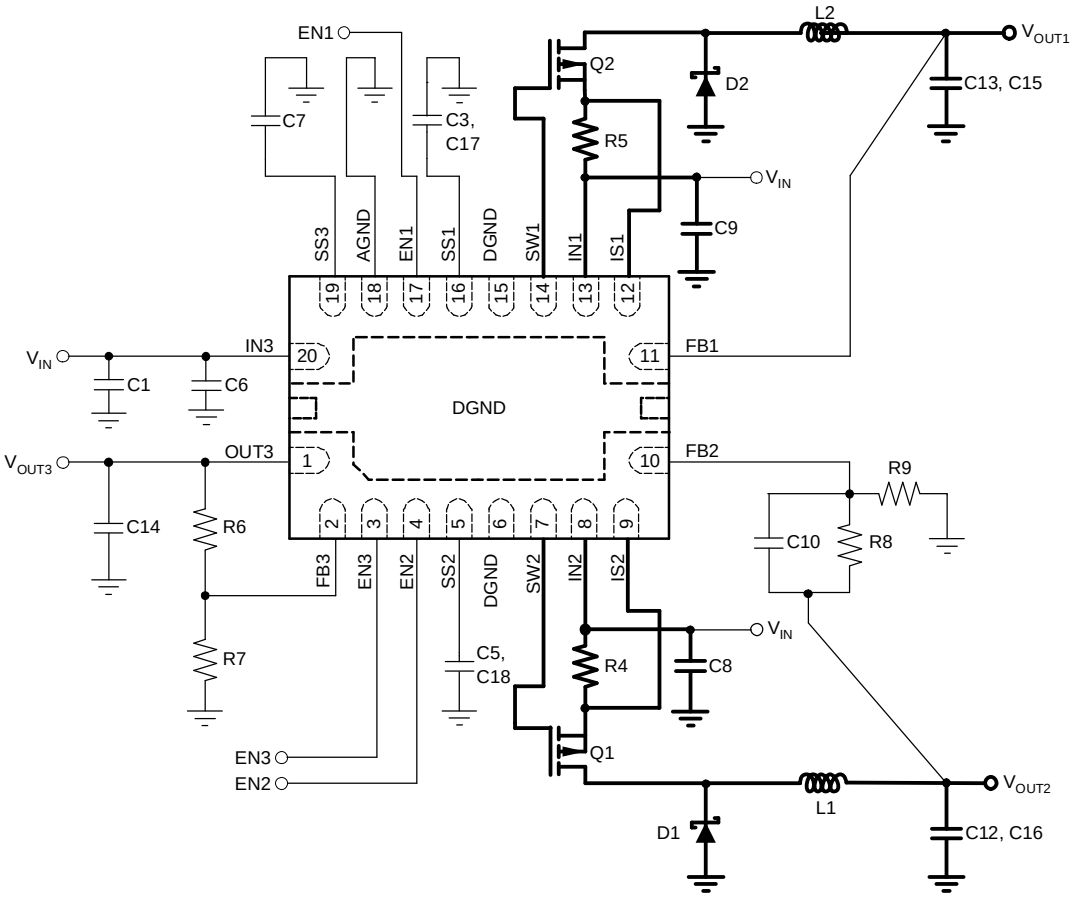

Figure 26. Typical Application Circuit

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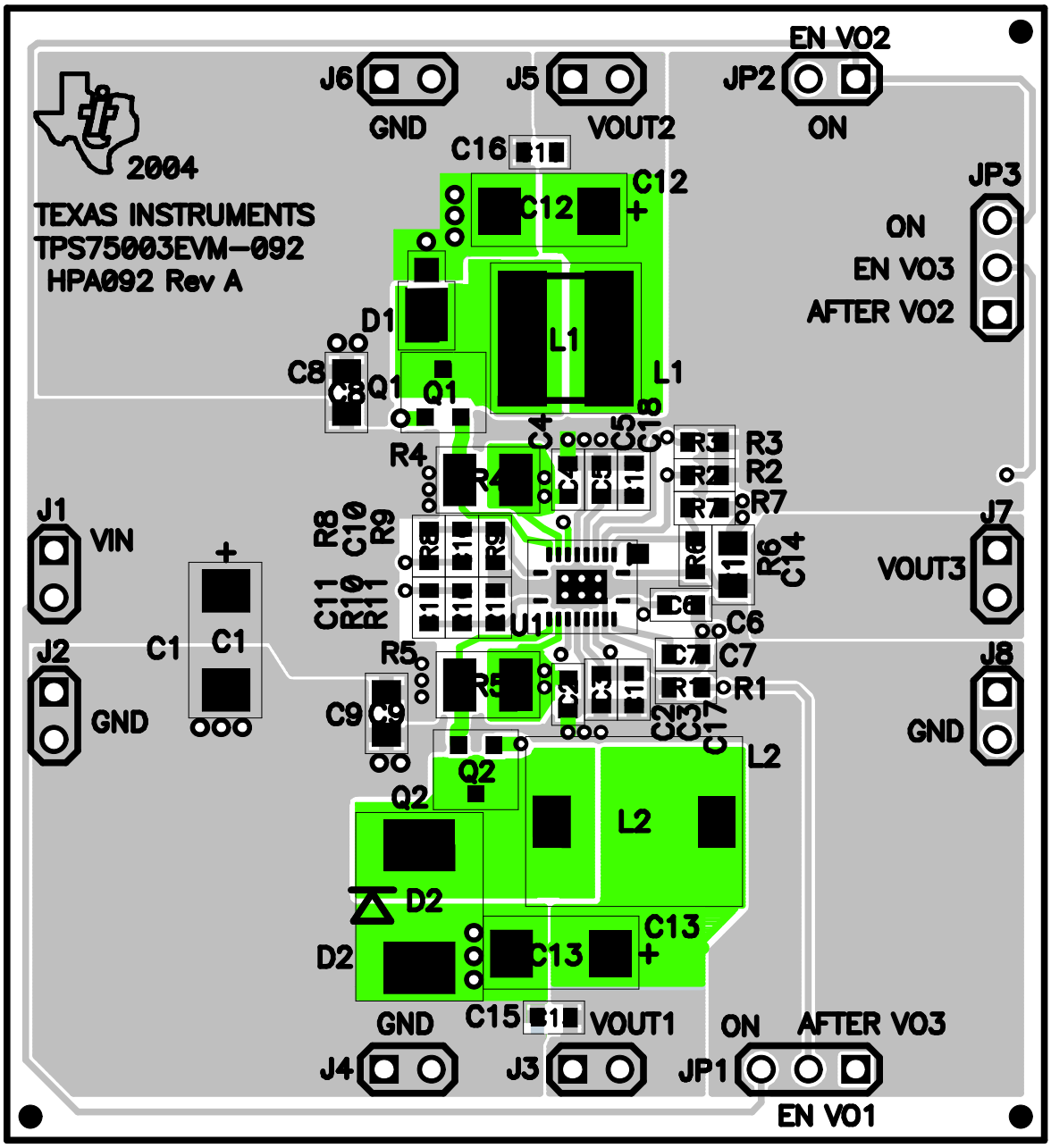

Figure 27. Recommended PCB Layout, Component Side, Top View

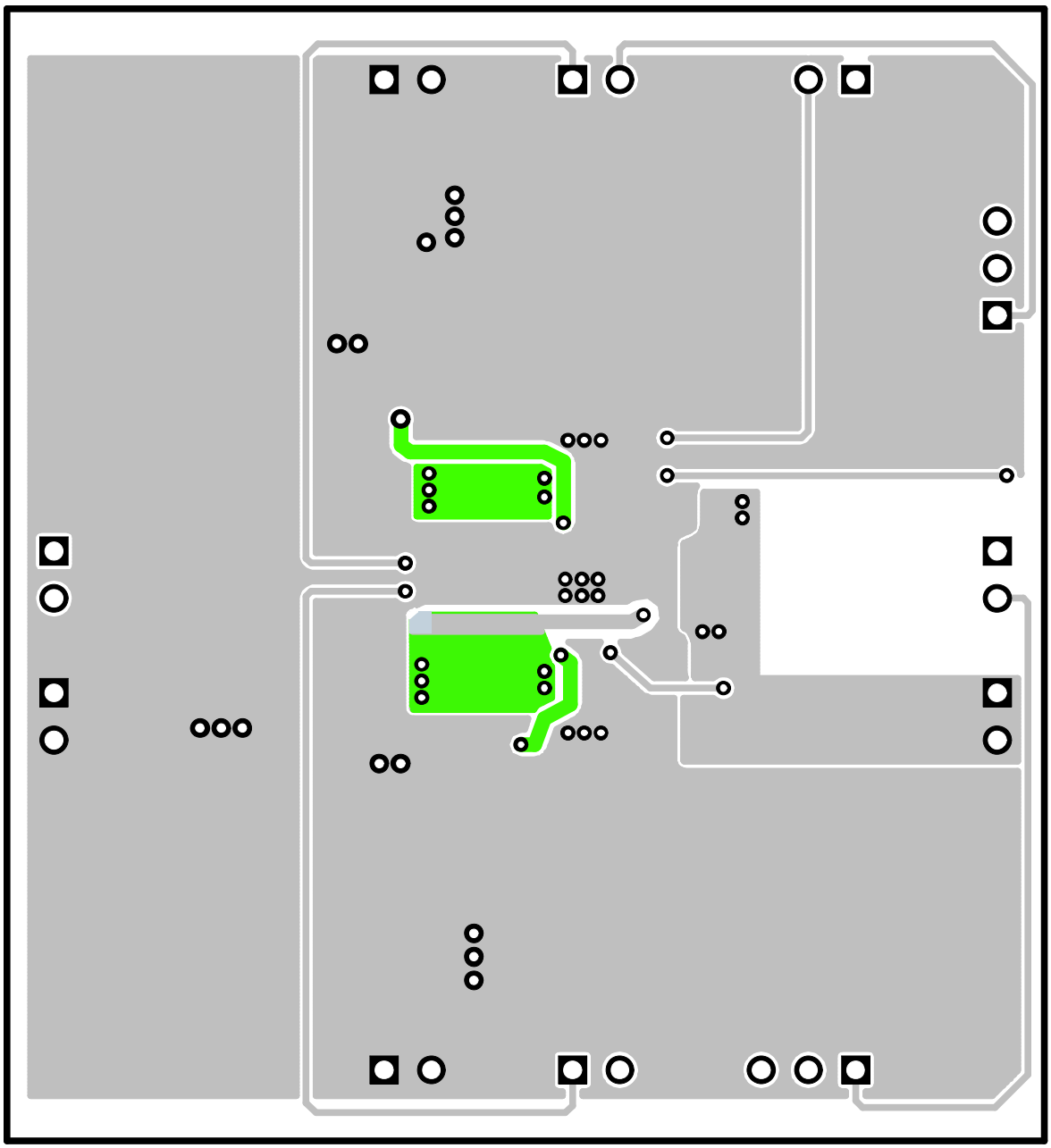

Figure 28. Recommended PCB Layout, Bottom Side, Top View

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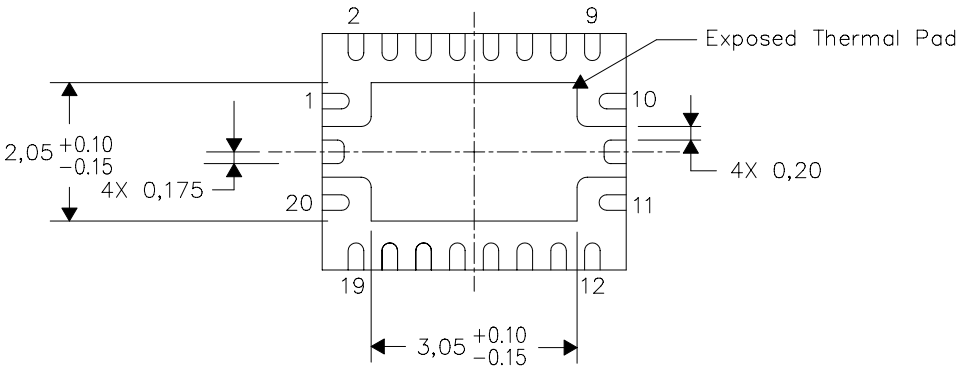
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

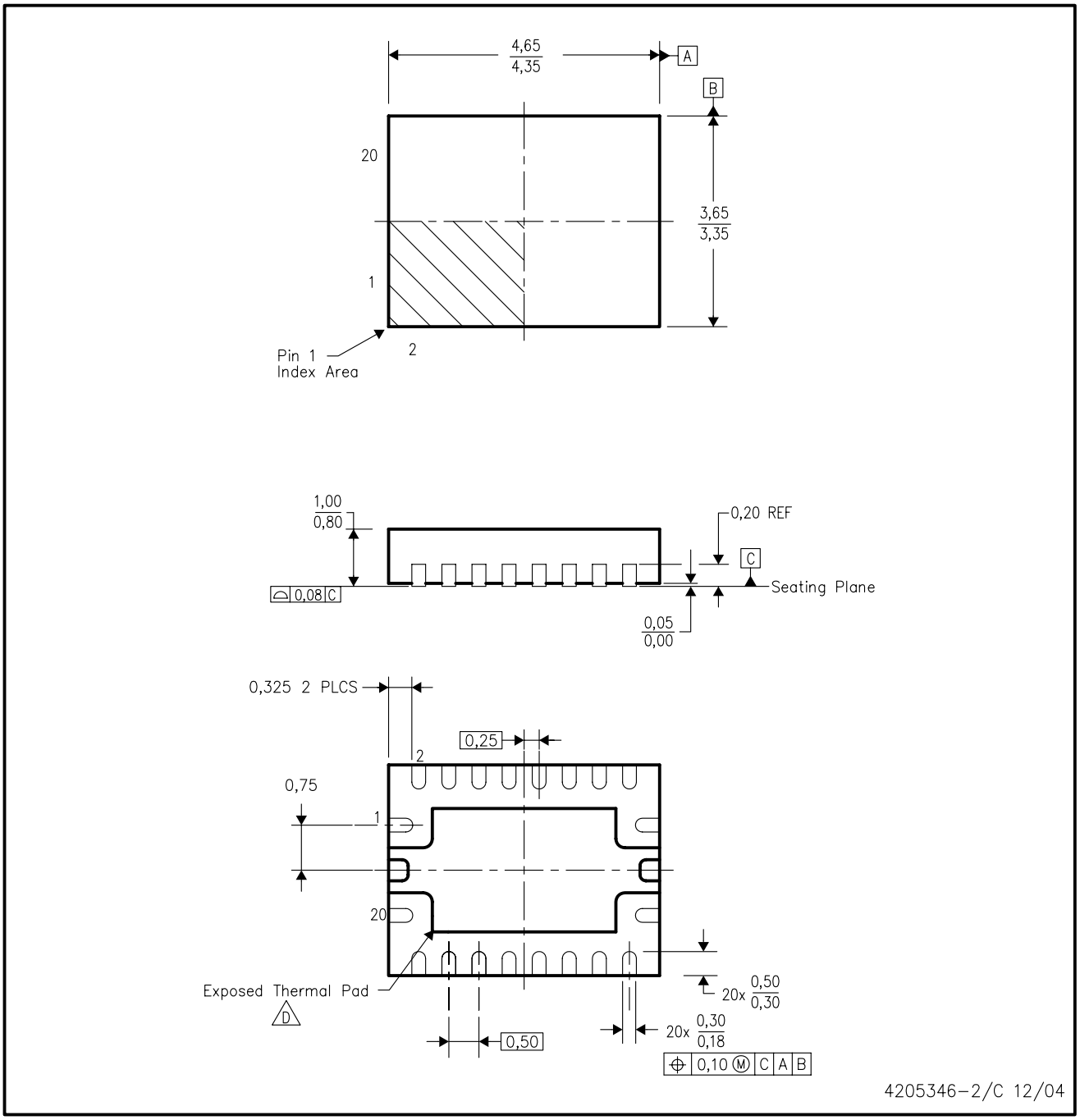


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHL (R–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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