

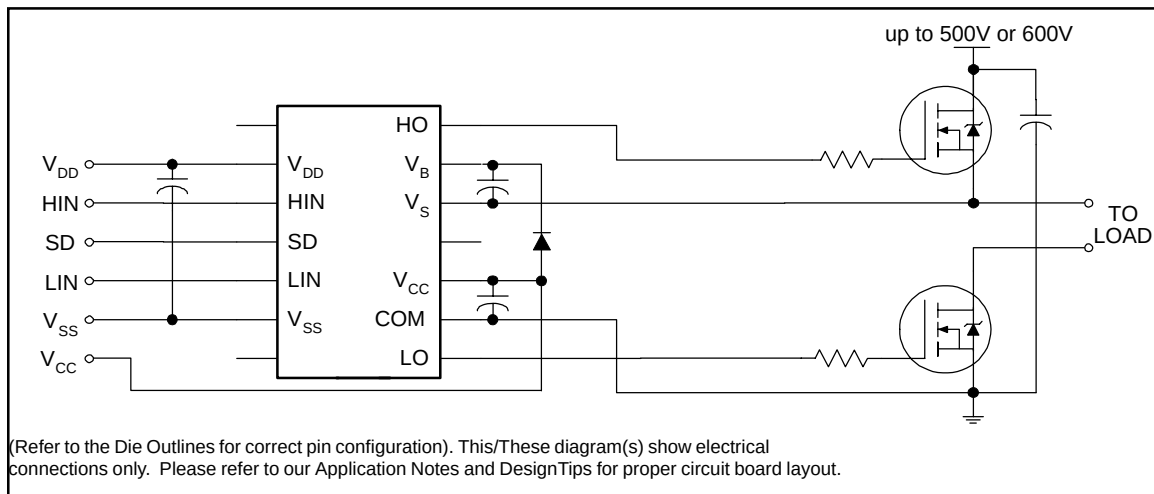
IR2110C/IR2113C

HIGH AND LOW SIDE DRIVER IN DIE WAFER FORM

Features

- 100 % Tested at Probe^①
- Available in Chip Pack, Unsawn Wafer, Sawn on Film^②
- Floating channel designed for bootstrap operation
Fully operational to +500V or +600V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
Separate logic supply range from 3.3V to 20V
Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Typical Connection



Note:

① This IR product is 100% tested at wafer level and is manufactured using established, mature and well characterized processes. Due to restrictions in die level processing, die may not be equivalent to standard package products and are therefore offered with a conditional performance guarantee. The above data sheet is based on IR sample testing under certain predetermined and assumed conditions, and are provided for illustration purposes only. Customers are encouraged to perform testing in actual proposed packaged and use conditions. IR die products are tested using IR-based quality assurance procedures and are manufactured using IR's established processes. Programs for customer-specified testing are available upon request. IR has experienced assembly yields of generally 95% or greater for individual die; however, customer's results will vary. Estimates such as those described and set forth in this data sheet for semiconductor die will vary depending on a number of packaging, handling, use and other factors. Sold die may not perform on an equivalent basis to standard package products and are therefore offered with a limited warranty as described in IR's applicable standard terms and conditions of sale. All IR die sales are subject to IR's applicable standard terms and conditions of sale, which are available upon request. For customers requiring a particular parameter to be guaranteed, special testing can be carried out or product can be purchased as known good die.

② Part number shown is for die in wafer. Contact factory for these other options.

IR2110C/IR2113C

International
IR Rectifier

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V _B	High side floating supply voltage (IR2110)	-0.3	525	V
	(IR2113)	-0.3	625	
V _S	High side floating supply offset voltage	V _B - 25	V _B + 0.3	
V _{HO}	High side floating output voltage	V _S - 0.3	V _B + 0.3	
V _{CC}	Low side fixed supply voltage	-0.3	25	
V _{LO}	Low side output voltage	-0.3	V _{CC} + 0.3	
V _{DD}	Logic supply voltage	-0.3	V _{SS} + 25	
V _{SS}	Logic supply offset voltage	V _{CC} - 25	V _{CC} + 0.3	
V _{IN}	Logic input voltage (HIN, LIN & SD)	V _{SS} - 0.3	V _{DD} + 0.3	
dV _S /dt	Allowable offset supply voltage transient (figure 2)	—	50	V/ns
T _J	Junction temperature	—	150	°C
T _S	Storage temperature	-55	150	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage (IR2110)	Note 1	500	
	(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	$V_{SS} + 3$	$V_{SS} + 20$	
V_{SS}	Logic supply offset voltage	-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

Static Electrical Characteristics

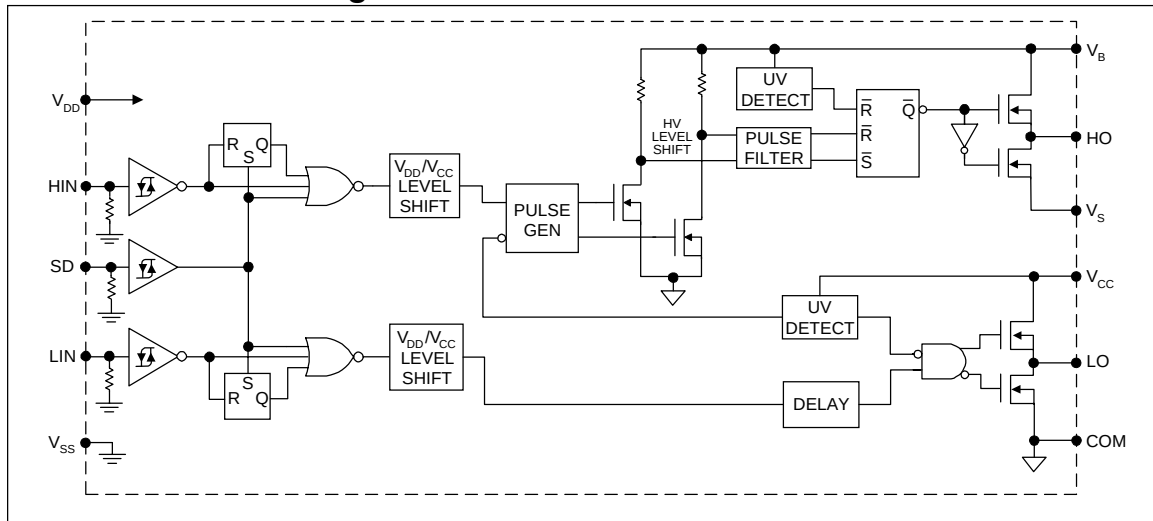
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.2		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	16	—	—	50	μA	$V_B = V_S = 500V/600V$
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

Mechanical Data

Nominal Front Metal Composition, Thickness	Al-Si (Si: 1.0% $\pm$ 0.1%), 2 μm
Wafer Diameter	125mm with std. <100> flat
Wafer Thickness	625 $\pm$ 25 μm
Minimum Street Width	0.006"
Reject Ink Dot Size	0.02" – 0.03"
Recommended Storage Environment	Store in original container, in dessicated nitrogen, with no contamination.

Functional Block Diagram



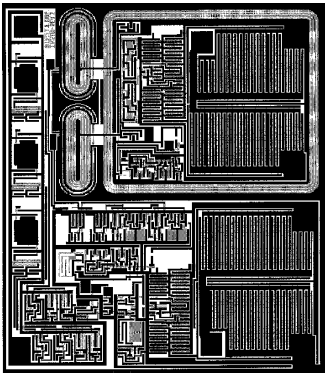
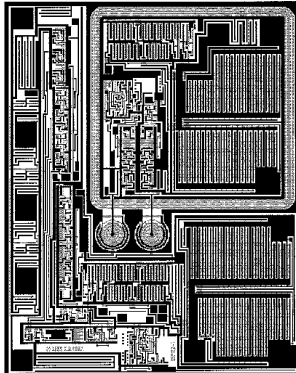
Bonding Pad Definitions

Symbol	Description
V _{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V _{SS}	Logic ground
V _B	High side floating supply
HO	High side gate drive output
V _S	High side floating supply return
V _{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

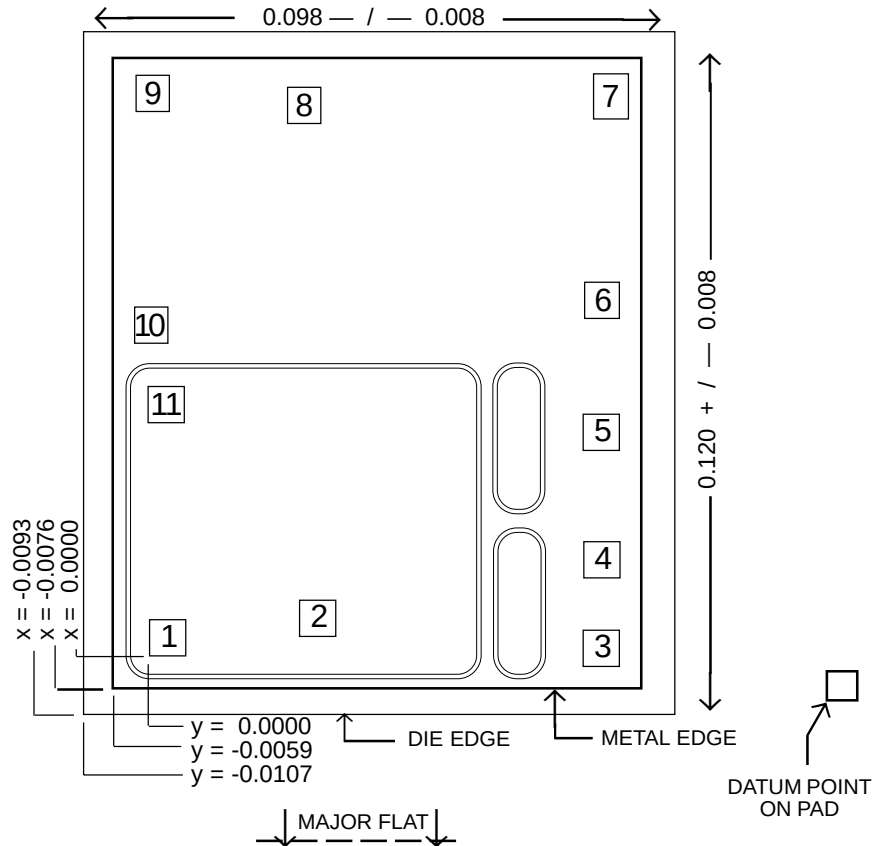
IR2110C/IR2113C

International
IR Rectifier

Device Information

Process & Design Rule			HVDCMOS 600V		
Transistor Count		IR2110	168	IR2113	220
Die Size:		IR2110	98 x 120 mils	IR2113	131 x 99 mils
Die Outline IR2110			Die Outline IR2113		
					
Thickness of Gate Oxide			800Å		
Connections		Material	Poly Silicon		
First Layer	Width	4.0 µm			
	Spacing	6.0 µm			
	Thickness	5000Å			
	Material	Al - Si (Si: 1.0% ±0.1%)			
Second Layer	Width	6.0 µm			
	Spacing	9.0 µm			
	Thickness	20,000Å			
	Contact Hole Dimension	5.0 µm X 5.0 µm			
Insulation Layer	Material	PSG (SiO ₂)			
	Thickness	1.5 µm			
Passivation	Material	PSG (SiO ₂)			
	Thickness	1.6 µm			
Method of Saw			Full Cut		
Method of Die Bond			Ablebond 84 - 1		
Wire Bond	Method	Thermosonic			
	Material	Au (1.3 mil)			
Leadframe	Material	Cu			
	Die Area	Ag			
	Lead Plating	70-90% Sn (Balance Pb)			
Package	Types	14-Lead PDIP & 16-Lead SOIC			
	Materials	EME6300 / EME6600RA			
Remarks: * Patent Pending					

Die Outline:
IR2110C
(in inches)

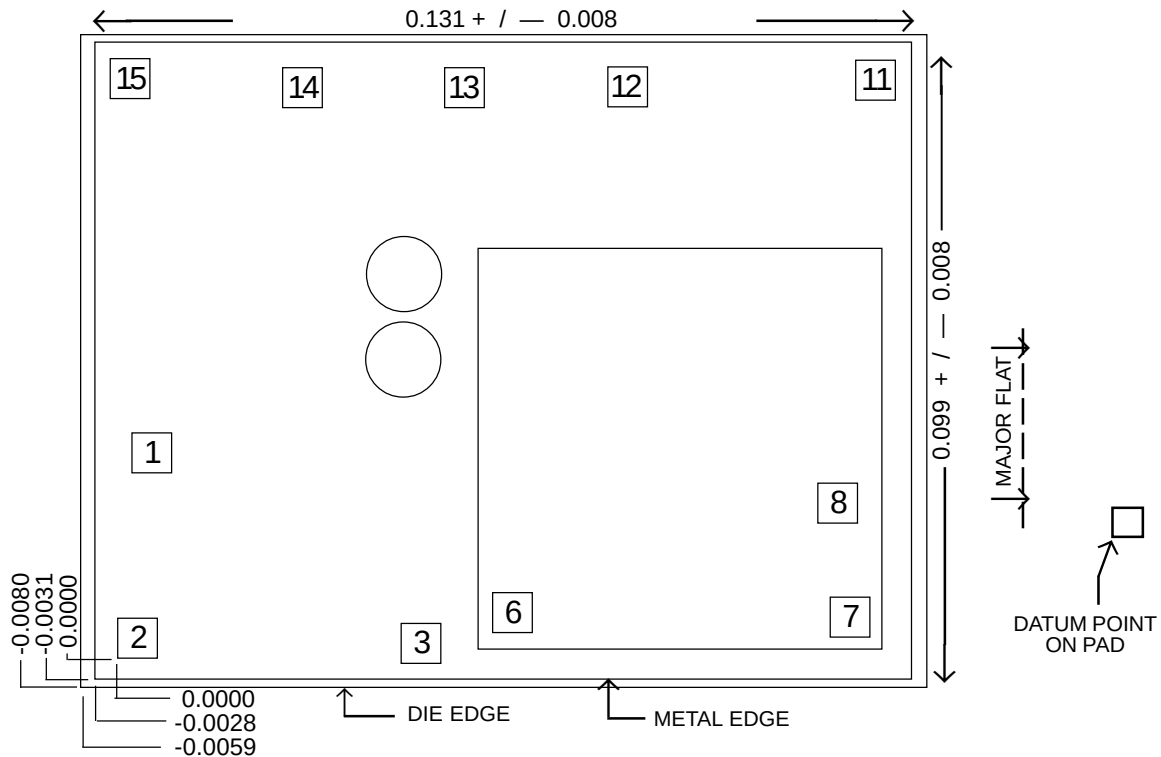


All pad sizes are 0.004 x 0.004 inches. All units are in inches.

IR2110C/IR2113C

International
IR Rectifier

Die Outline: IR2113C (in inches)



Pad #	Function	Datum		PAD SIZE
		X	Y	
1	LO	0.0020	0.0274	0.0061 X 0.0058
2	COM	0.0000	0.0000	0.0061 X 0.0058
3	VCC	0.0426	-0.0007	0.0059 X 0.0059
6	VS	0.0559	0.0040	0.0061 X 0.0058
7	VB	0.1062	0.0032	0.0059 X 0.0059
8	HO	0.1042	0.0198	0.0061 X 0.0058
11	VDD	0.1098	0.0815	0.0060 X 0.0060
12	HIN	0.0726	0.0803	0.0060 X 0.0060
13	SD	0.0488	0.0803	0.0060 X 0.0060
14	LIN	0.0252	0.0803	0.0060 X 0.0060
15	VSS	-0.0009	0.0819	0.0060 X 0.0060
X and Y Tolerances +/- 0.0002				

All pad sizes are 0.004 x 0.004 inches. All units are in inches.

IR2110C/IR2113C

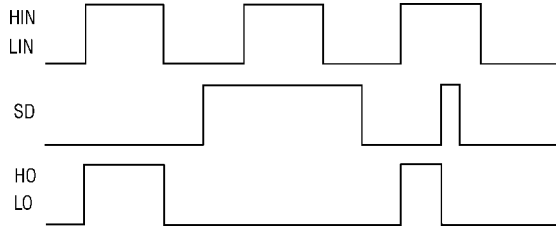


Figure 1. Input/Output Timing Diagram

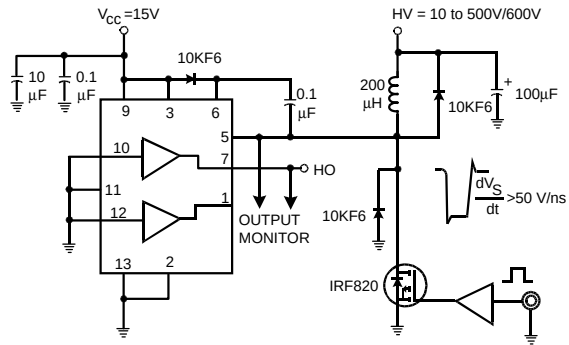


Figure 2. Floating Supply Voltage Transient Test Circuit

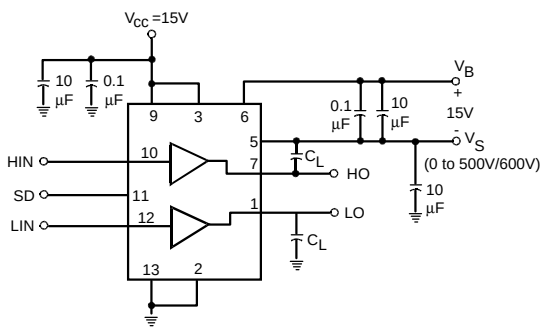


Figure 3. Switching Time Test Circuit

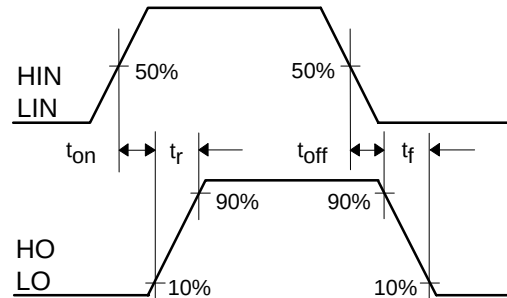


Figure 4. Switching Time Waveform Definition

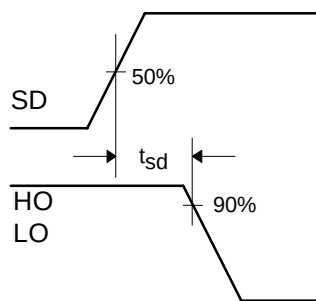


Figure 5. Shutdown Waveform Definitions

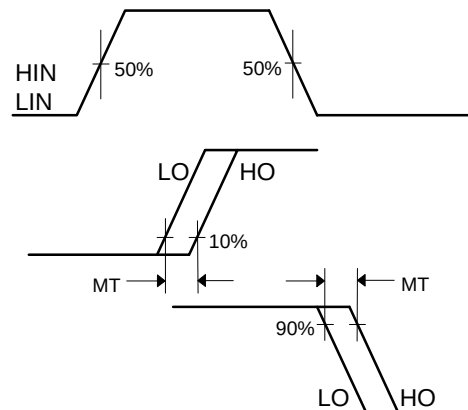


Figure 6. Delay Matching Waveform Definitions

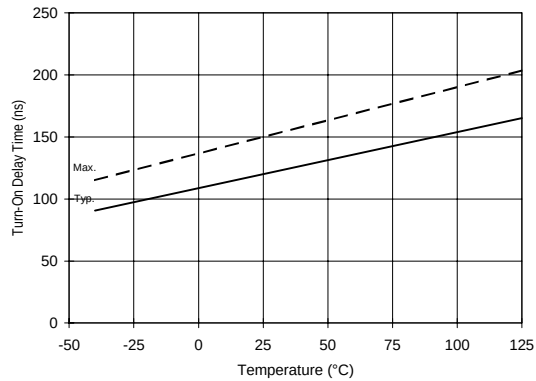


Figure 7A. Turn-On Time vs. Temperature

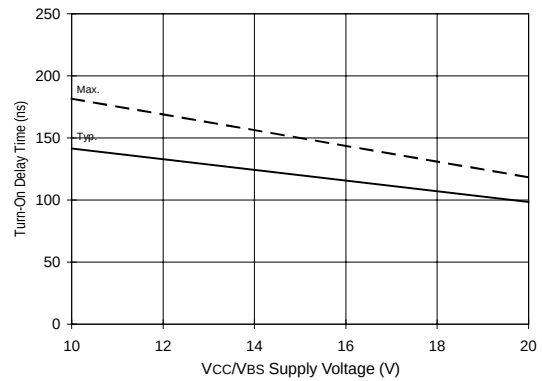


Figure 7B. Turn-On Time vs. Vcc/Vbs Supply Voltage

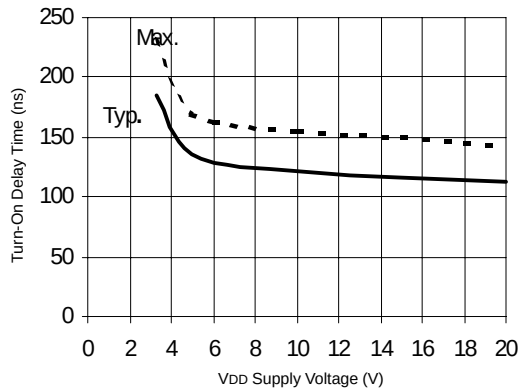


Figure 7C. Turn-On Time vs. VDD Supply Voltage

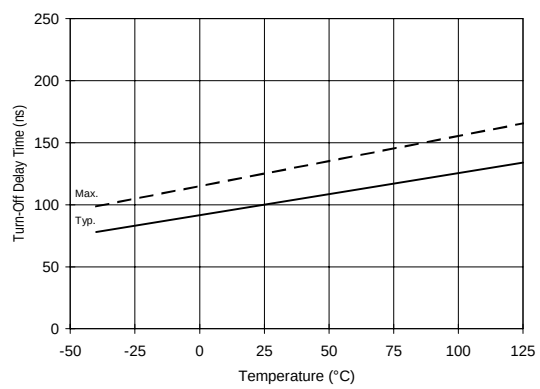


Figure 8A. Turn-Off Time vs. Temperature

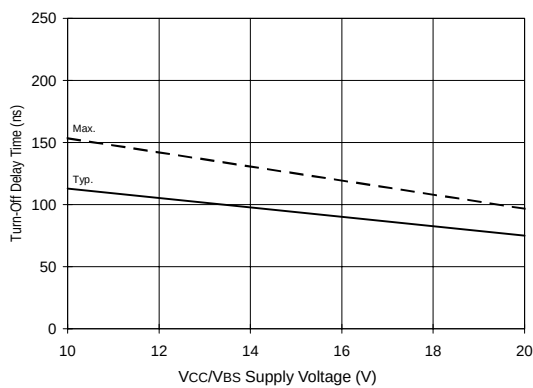


Figure 8B. Turn-Off Time vs. Vcc/Vbs Supply Voltage

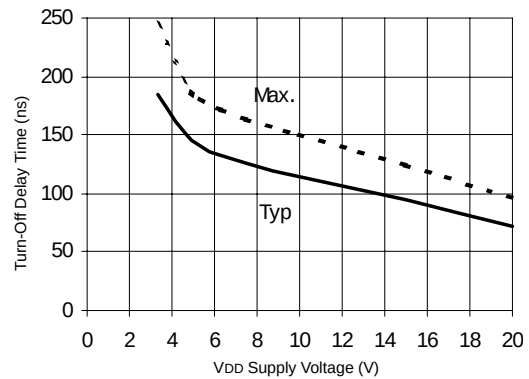


Figure 8C. Turn-Off Time vs. VDD Supply Voltage

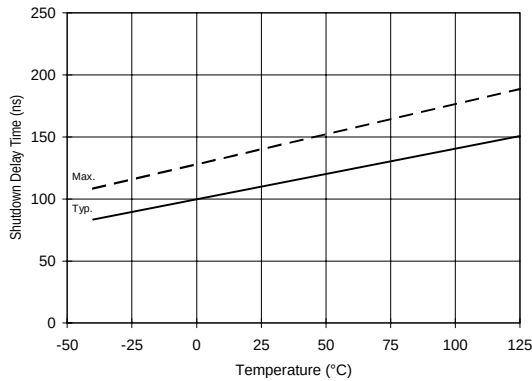


Figure 9A. Shutdown Time vs. Temperature

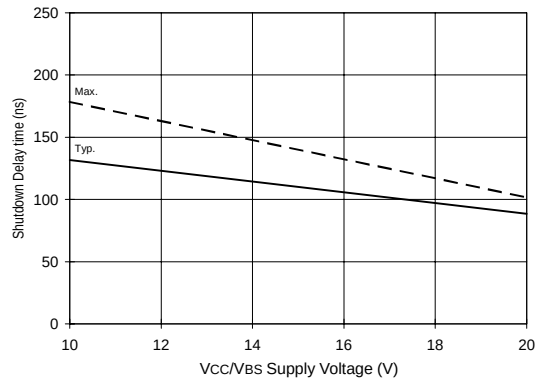


Figure 9B. Shutdown Time vs. Vcc/Vbs Supply Voltage

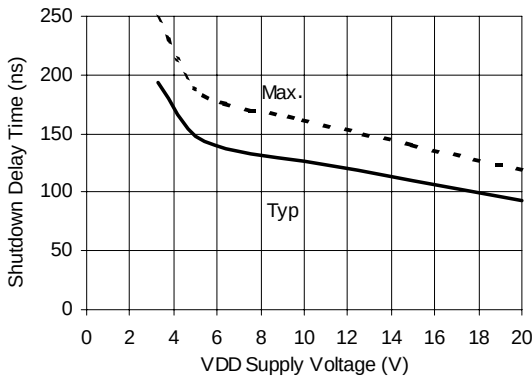


Figure 9C. Shutdown Time vs. VDD Supply Voltage

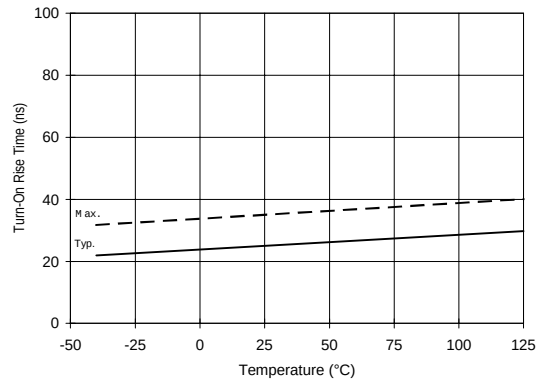


Figure 10A. Turn-On Rise Time vs. Temperature

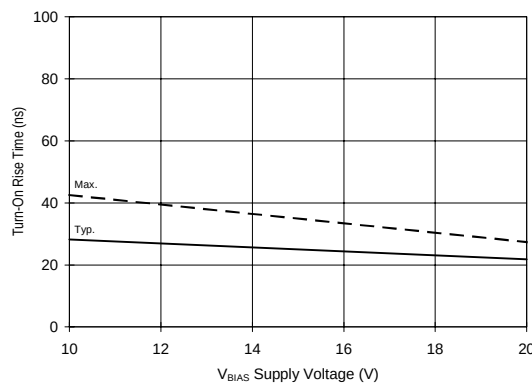


Figure 10B. Turn-On Rise Time vs. Voltage

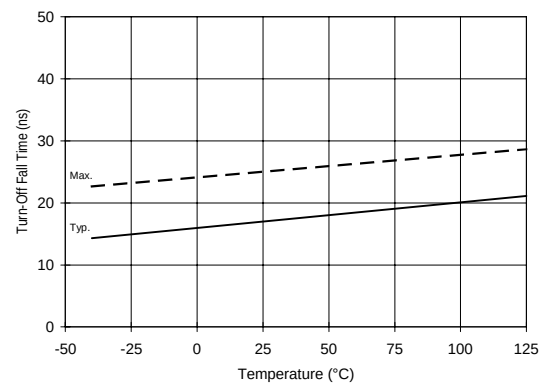


Figure 11A. Turn-Off Fall Time vs. Temperature

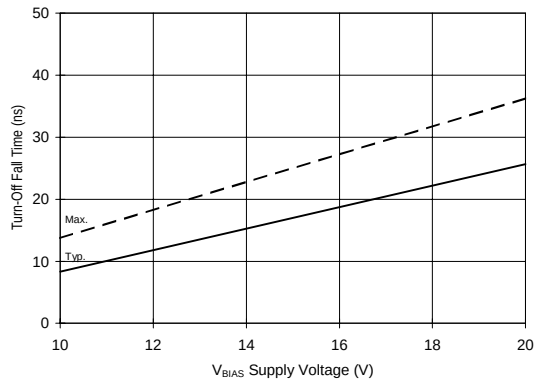


Figure 11B. Turn-Off Fall Time vs. Voltage

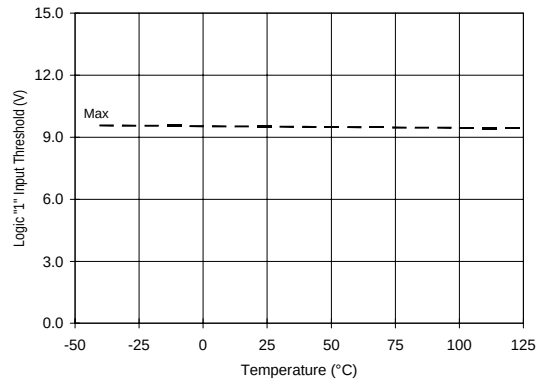


Figure 12A. Logic "1" Input Threshold vs. Temperature

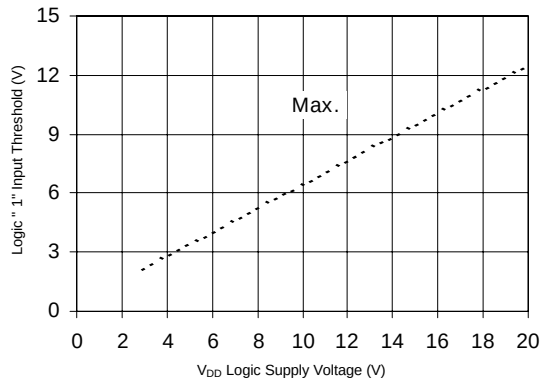


Figure 12B. Logic "1" Input Threshold vs. Voltage

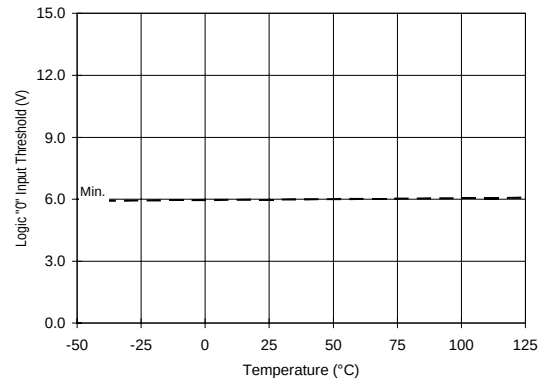


Figure 13A. Logic "0" Input Threshold vs. Temperature

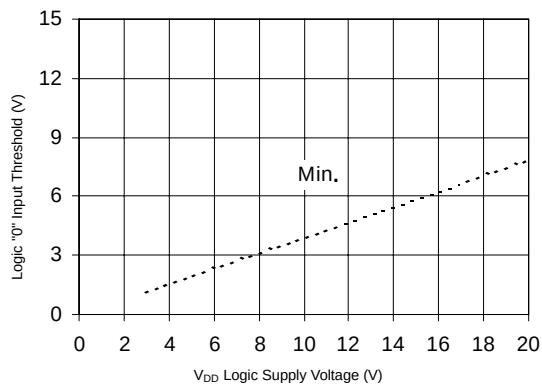


Figure 13B. Logic "0" Input Threshold vs. Voltage

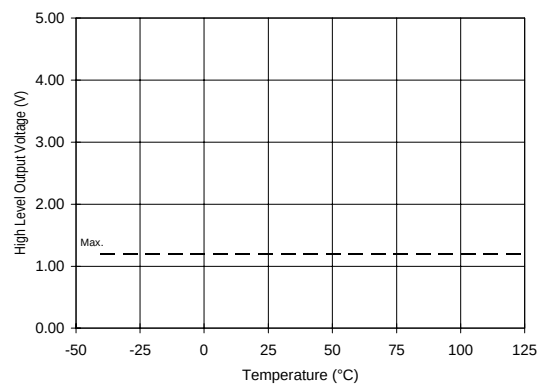


Figure 14A. High Level Output vs. Temperature

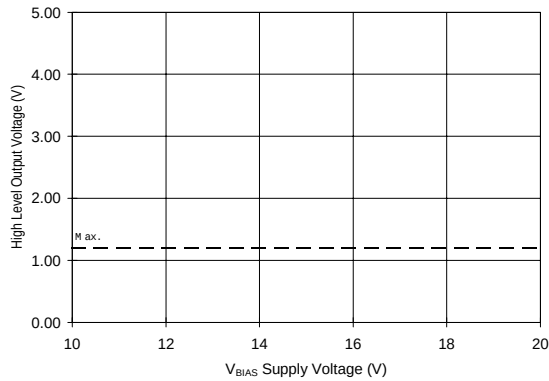


Figure 14B. High Level Output vs. Voltage

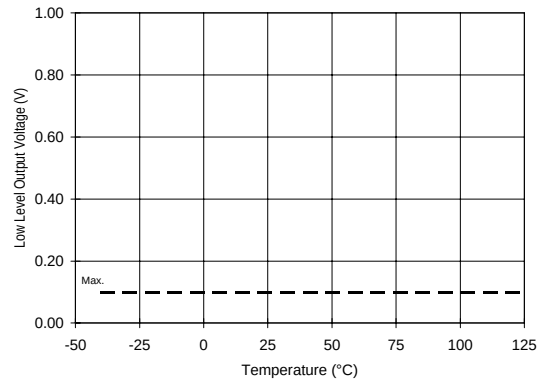


Figure 15A. Low Level Output vs. Temperature

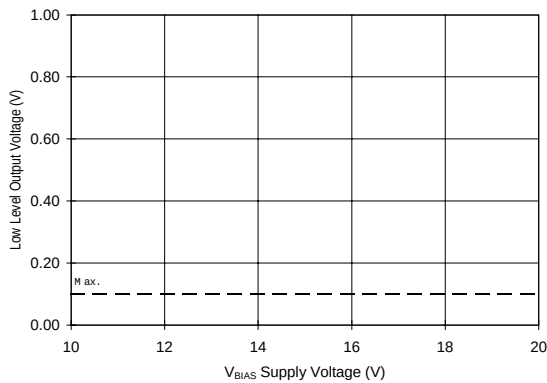


Figure 15B. Low Level Output vs. Voltage

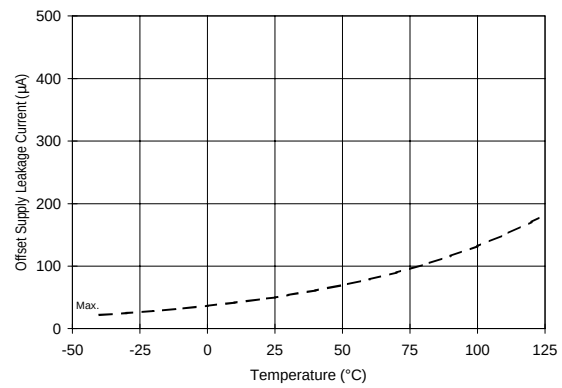


Figure 16A. Offset Supply Current vs. Temperature

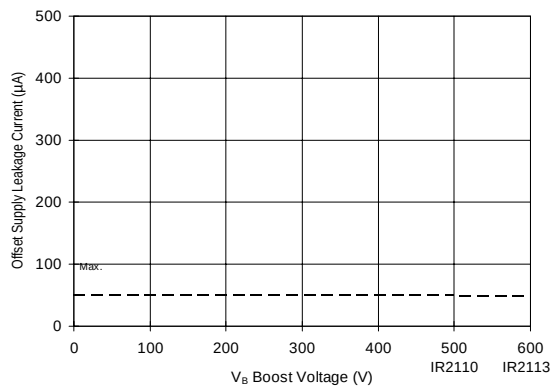


Figure 16B. Offset Supply Current vs. Voltage

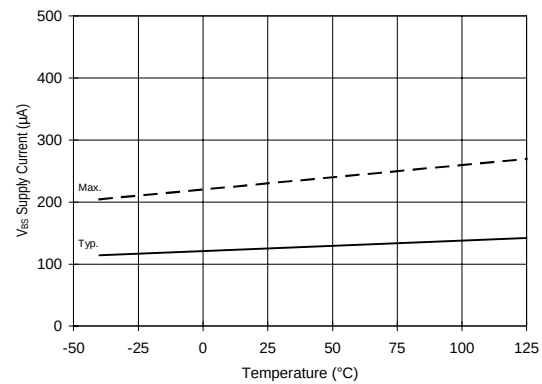


Figure 17A. V_{BS} Supply Current vs. Temperature

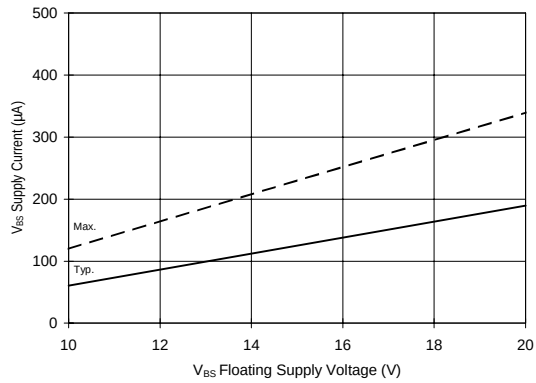


Figure 17B. V_{BS} Supply Current vs. Voltage

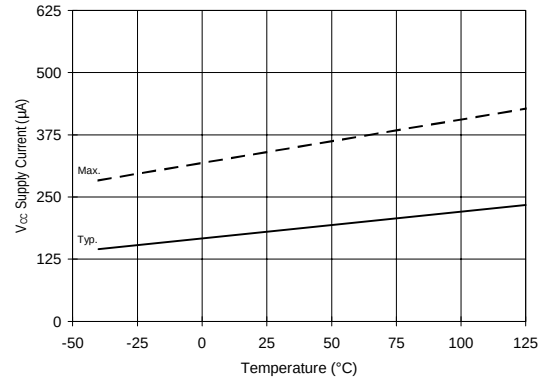


Figure 18A. V_{CC} Supply Current vs. Temperature

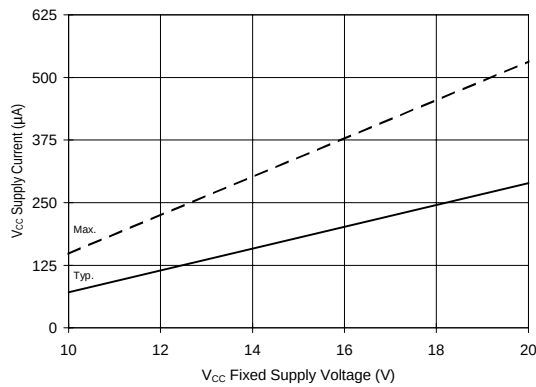


Figure 18B. V_{CC} Supply Current vs. Voltage

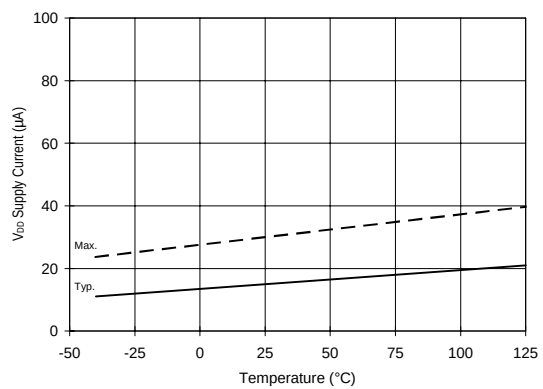


Figure 19A. V_{DD} Supply Current vs. Temperature

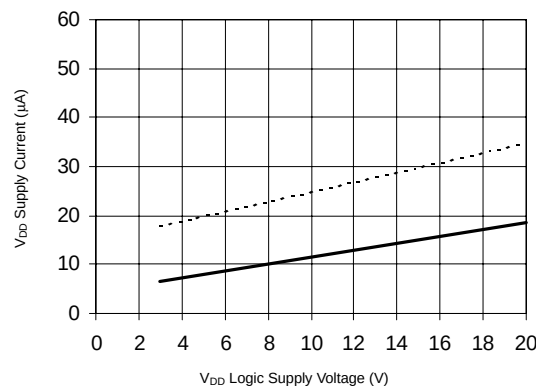


Figure 19B. V_{DD} Supply Current vs. V_{DD} Voltage

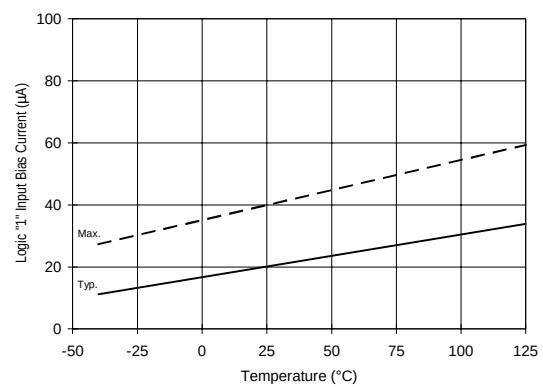


Figure 20A. Logic "1" Input Current vs. Temperature

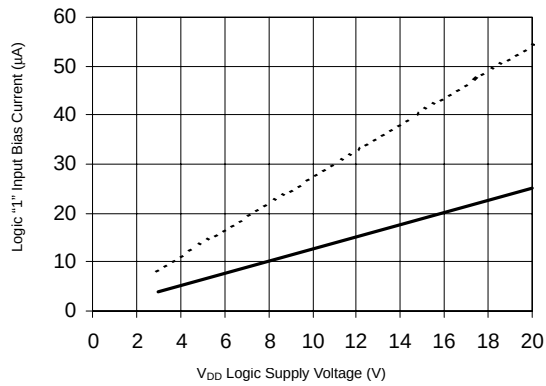


Figure 20B. Logic "1" Input Current vs. V_{DD} Voltage

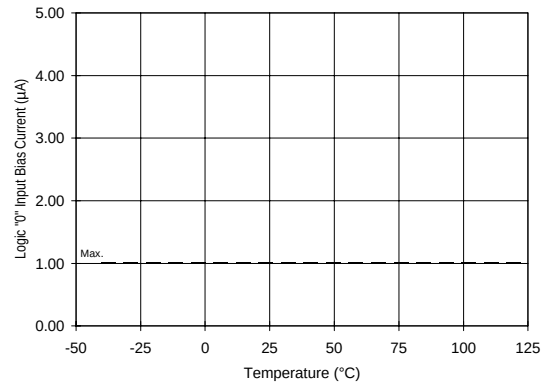


Figure 21A. Logic "0" Input Current vs. Temperature

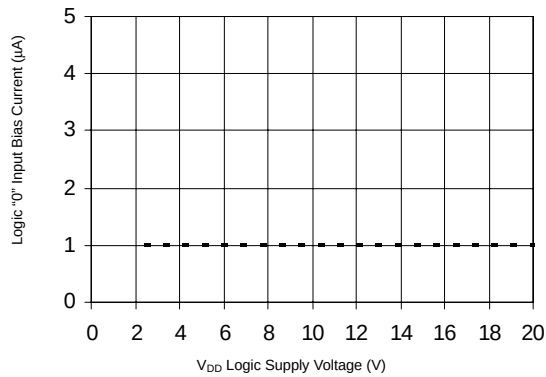


Figure 21B. Logic "0" Input Current vs. V_{DD} Voltage

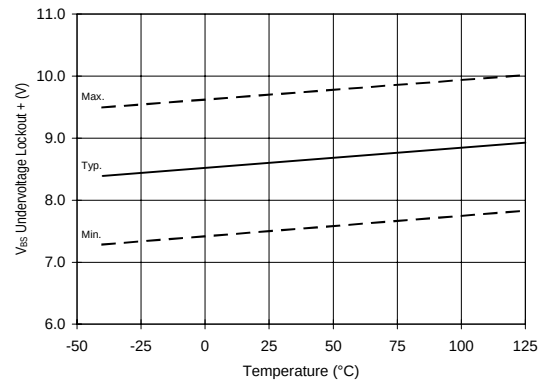


Figure 22. V_{BS} Undervoltage (+) vs. Temperature

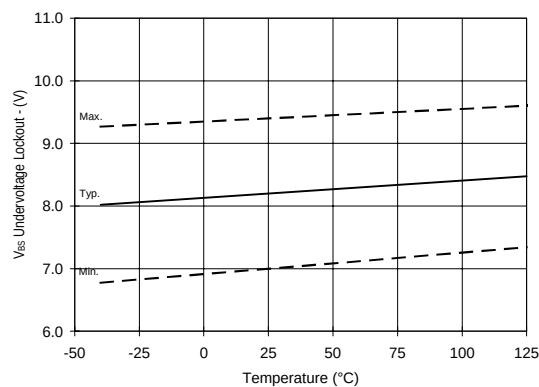


Figure 23. V_{BS} Undervoltage (-) vs. Temperature

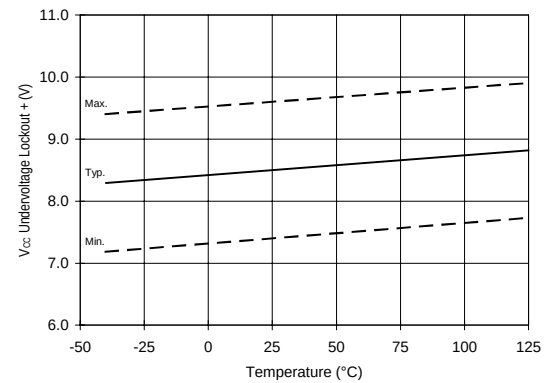


Figure 24. V_{CC} Undervoltage (+) vs. Temperature

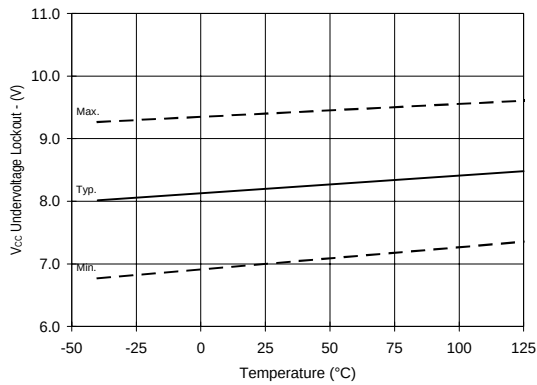


Figure 25. Vcc Undervoltage (-) vs. Temperature

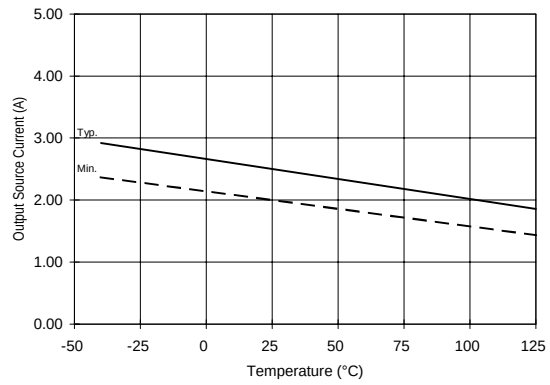


Figure 26A. Output Source Current vs. Temperature

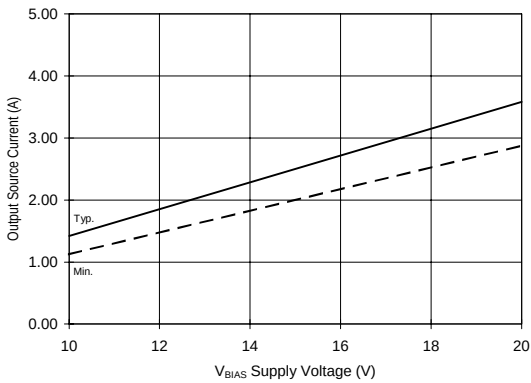


Figure 26B. Output Source Current vs. Voltage

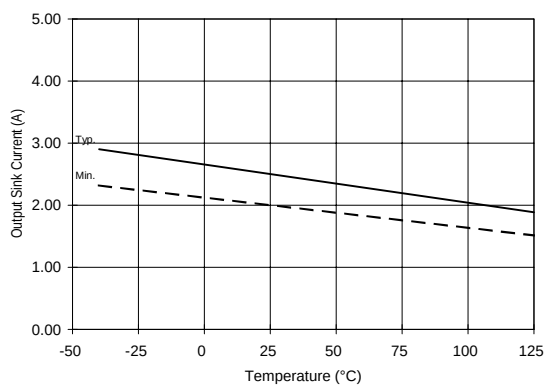


Figure 27A. Output Sink Current vs. Temperature

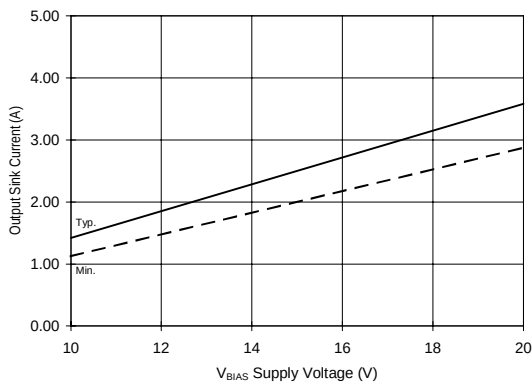


Figure 27B. Output Sink Current vs. Voltage

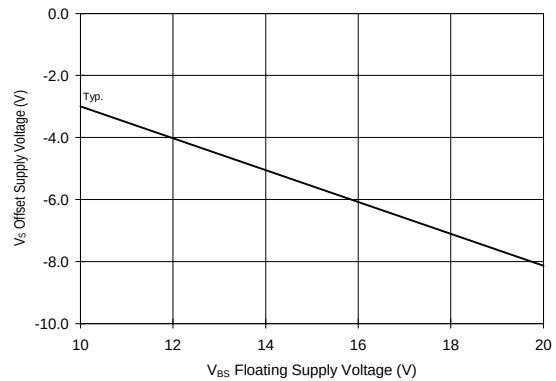
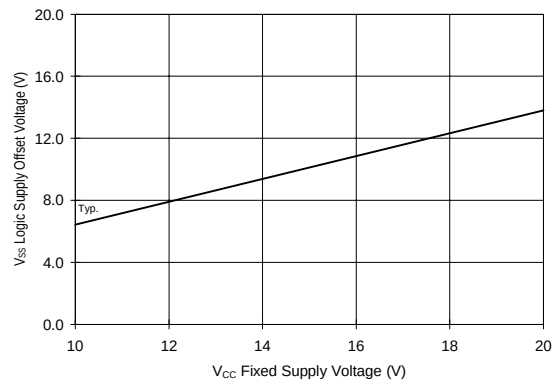


Figure 28. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage



**Figure 29. Maximum V_{SS} Positive Offset vs.
V_{CC} Supply Voltage**

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Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Three shipping options are offered as standard.

- Un-sawn wafer
- Die in waffle pack
- Die on film

Tape and Reel is also available for some products.

Please specify your required shipping option when requesting prices and ordering Die product. If not specified, Un-sawn wafer will be assumed.

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Un-sawn wafers and singulated die can be stored for up to 12 months when in the original sealed packaging at room temperature (45% +/- 15% RH controlled environment).
- Un-sawn wafers and singulated die that have been opened can be stored when returned to their containers and placed in a Nitrogen purged cabinet, at room temperature (45% +/- 15% RH controlled environment).
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.
- Die in Surf Tape type carrier tape are intended for immediate use and have a limited shelf life. This is primarily due to the nature of the adhesive tape used to hold the product in the carrier tape cavity. This product can be stored for up to 30 days. This applies whether or not the material has remained in its original sealed container.

For further information: Please contact your local IR Sales office or email your enquiry to <http://die.irf.com>

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