

# LM5111

## Dual 5A Compound Gate Driver

### General Description

The LM5111 Dual Gate Driver replaces industry standard gate drivers with improved peak output current and efficiency. Each "compound" output driver stage includes MOS and bipolar transistors operating in parallel that together sink more than 5A peak from capacitive loads. Combining the unique characteristics of MOS and bipolar devices reduces drive current variation with voltage and temperature. Under-voltage lockout protection is also provided. The drivers can be operated in parallel with inputs and outputs connected to double the drive current capability. This device is available in the SOIC-8 package.

### Features

- Independently drives two N-Channel MOSFETs
- Compound CMOS and bipolar outputs reduce output current variation
- 5A sink/3A source current capability
- Two channels can be connected in parallel to double the drive current

- Independent inputs (TTL compatible)
- Fast propagation times (25 ns typical)
- Fast rise and fall times (14 ns/12 ns rise/fall with 2 nF load)
- Available in dual non-inverting, dual inverting and combination configurations
- Supply rail under-voltage lockout protection
- Pin compatible with industry standard gate drivers

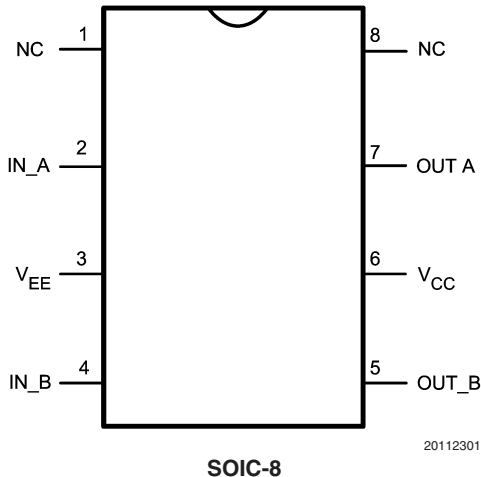
### Typical Applications

- Synchronous Rectifier Gate Drivers
- Switch-mode Power Supply Gate Driver
- Solenoid and Motor Drivers

### Package

- SOIC-8

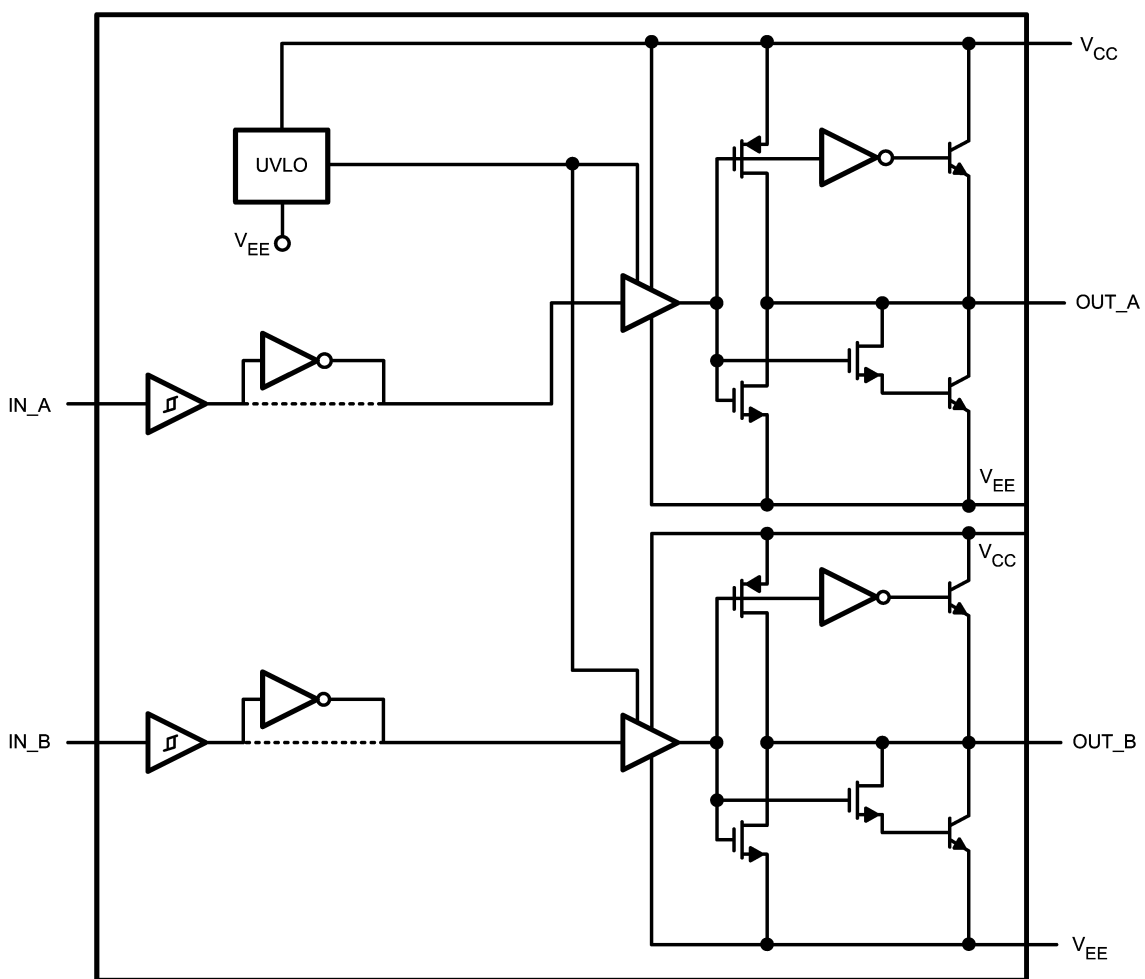
### Pin Configurations



## Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM5111-1M	SOIC-8	M08A	Shipped in anti-static units, 95 Units/Rail
LM5111-1MX	SOIC-8	M08A	2500 shipped in Tape & Reel
LM5111-2M	SOIC-8	M08A	Shipped in anti-static units, 95 Units/Rail
LM5111-2MX	SOIC-8	M08A	2500 shipped in Tape & Reel
LM5111-3M	SOIC-8	M08A	Shipped in anti-static units, 95 Units/Rail
LM5111-3MX	SOIC-8	M08A	2500 shipped in Tape & Reel

## Block Diagram



Block Diagram of LM5111

20112303

## Pin Description

Pin	Name	Description	Application Information
1	NC	No Connect	
2	IN_A	'A' side control input	TTL compatible thresholds.
3	V <sub>EE</sub>	Ground reference for both inputs and outputs	Connect to power ground.
4	IN_B	'B' side control input	TTL compatible thresholds.
5	OUT_B	Output for the 'B' side driver.	Voltage swing of this output is from V <sub>CC</sub> to V <sub>EE</sub> . The output stage is capable of sourcing 3A and sinking 5A.
6	V <sub>CC</sub>	Positive output supply	Locally decouple to V <sub>EE</sub> .
7	OUT_A.	Output for the 'A' side driver.	Voltage swing of this output is from V <sub>CC</sub> to V <sub>EE</sub> . The output stage is capable of sourcing 3A and sinking 5A.
8	NC	No Connect	

## Configuration Table

Part Number	"A" Output Configuration	"B" Output Configuration	Package
LM5111-1M	Non-Inverting	Non-Inverting	SOIC- 8
LM5111-2M	Inverting	Inverting	SOIC- 8
LM5111-3M	Inverting	Non-Inverting	SOIC- 8

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{CC}$ to $V_{EE}$	-0.3V to 15V
IN to $V_{EE}$	-0.3V to 15V

Storage Temperature Range, ( $T_{STG}$ )	-55°C to +150°C
Maximum Junction Temperature, ( $T_J(max)$ )	+150°C
Operating Junction Temperature	+125°C
ESD Rating	2kV

**Electrical Characteristics**

$T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ ,  $V_{EE} = 0\text{V}$ , No Load on OUT\_A or OUT\_B, unless otherwise specified.

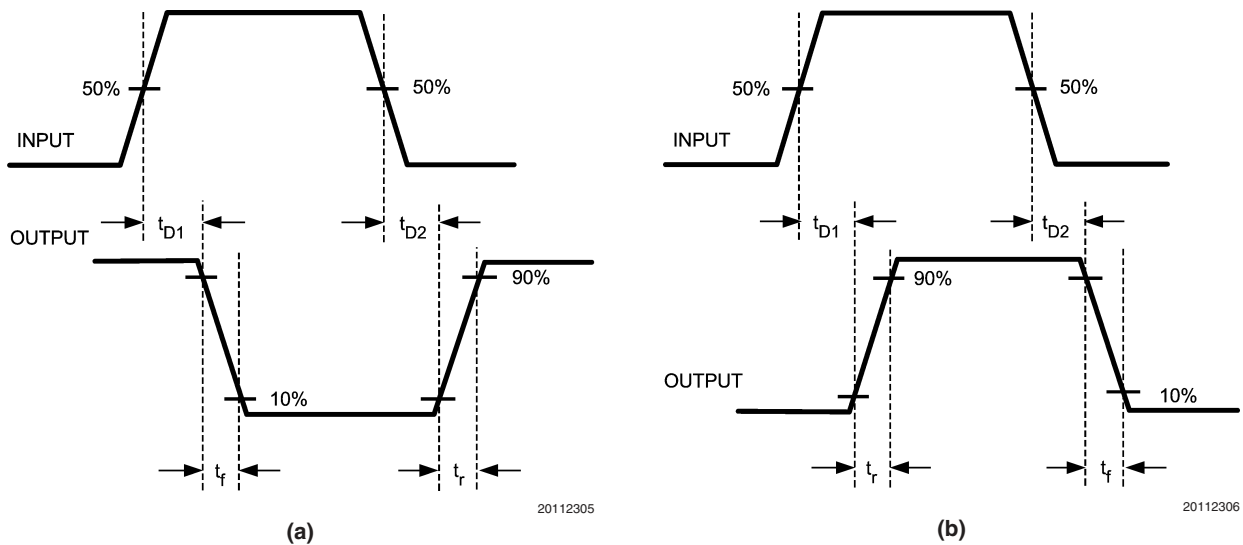
Symbol	Parameter	Conditions	Min	Typ	Max	Units
	V <sub>CC</sub> Operating Range	V <sub>CC</sub> -V <sub>EE</sub>	3.5		14	V
V <sub>CCR</sub>	V <sub>CC</sub> Under Voltage Lockout (rising)	V <sub>CC</sub> -V <sub>EE</sub>	2.3	2.9	3.5	V
V <sub>CCH</sub>	V <sub>CC</sub> Under Voltage Lockout Hysteresis			230		mV
I <sub>CC</sub>	V <sub>CC</sub> Supply Current (I <sub>CC</sub> )	IN_A = IN_B = 0V (5111-1)		1	2	mA
		IN_A = IN_B = V <sub>CC</sub> (5111-2)		1	2	
		IN_A = V <sub>CC</sub> , IN_B = 0V (5111-3)		1	2	
CONTROL INPUTS						
V <sub>IH</sub>	Logic High			1.75	2.2	V
V <sub>IL</sub>	Logic Low		0.8	1.35		V
HYS	Input Hysteresis			400		mV
I <sub>IL</sub>	Input Current Low	IN_A=IN_B=V <sub>CC</sub> (5111-1-2-3)	-1	0.1	1	μA
I <sub>IH</sub>	Input Current High	IN_B=V <sub>CC</sub> (5111-3)	10	18	25	
		IN_A=IN_B=V <sub>CC</sub> (5111-2)	-1	0.1	1	
		IN_A=IN_B=V <sub>CC</sub> (5111-1)	10	18	25	
		IN_A=V <sub>CC</sub> (5111-3)	-1	0.1	1	
OUTPUT DRIVERS						
R <sub>OH</sub>	Output Resistance High	I <sub>OUT</sub> = -10 mA		30	50	Ω
R <sub>OL</sub>	Output Resistance Low	I <sub>OUT</sub> = + 10 mA		1.4	2.5	Ω
I <sub>Source</sub>	Peak Source Current	OUTA/OUTB = V <sub>CC</sub> /2, 200 ns Pulsed Current		3		A
I <sub>Sink</sub>	Peak Sink Current	OUTA/OUTB = V <sub>CC</sub> /2, 200 ns Pulsed Current		5		A

**Electrical Characteristics** (Continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{CC} = 12\text{V}$ ,  $V_{EE} = 0\text{V}$ , No Load on OUT\_A or OUT\_B, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>SWITCHING CHARACTERISTICS</b>						
td1	Propagation Delay Time Low to High, IN rising (IN to OUT)	$C_{LOAD} = 2\text{ nF}$ , see <i>Figure 1</i>		25	40	ns
td2	Propagation Delay Time High to Low, IN falling (IN to OUT)	$C_{LOAD} = 2\text{ nF}$ , see <i>Figure 1</i>		25	40	ns
$t_r$	Rise Time	$C_{LOAD} = 2.0\text{ nF}$ , see <i>Figure 1</i>		14	25	ns
$t_f$	Fall Time	$C_{LOAD} = 2\text{ nF}$ , see <i>Figure 1</i>		12	25	ns
<b>LATCHUP PROTECTION</b>						
	AEC - Q100, Method 004	$T_J = 150^{\circ}\text{C}$		500		mA

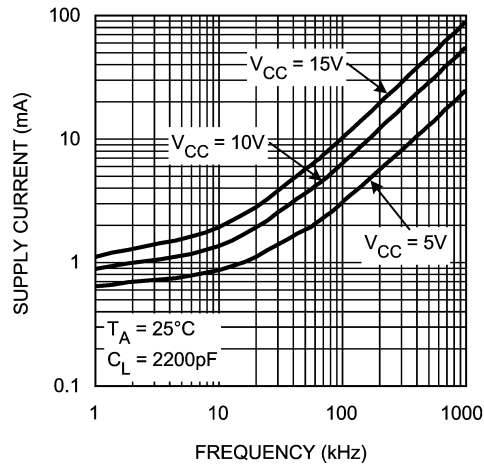
**Note 1:** Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

**Timing Waveforms**

**FIGURE 1. (a) Inverting, (b) Non-Inverting**

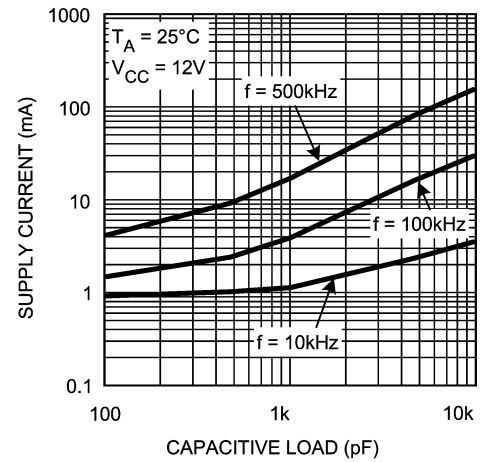
## Typical Performance Characteristics

### Supply Current vs Frequency



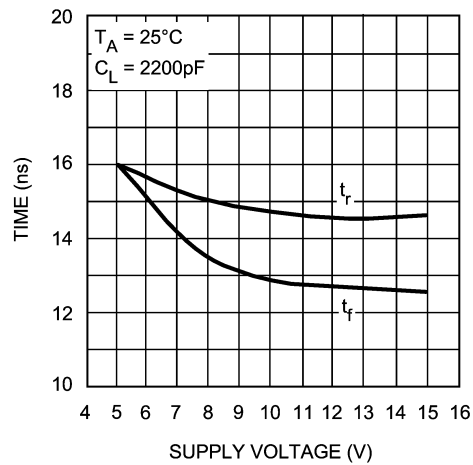
20112310

### Supply Current vs Capacitive Load



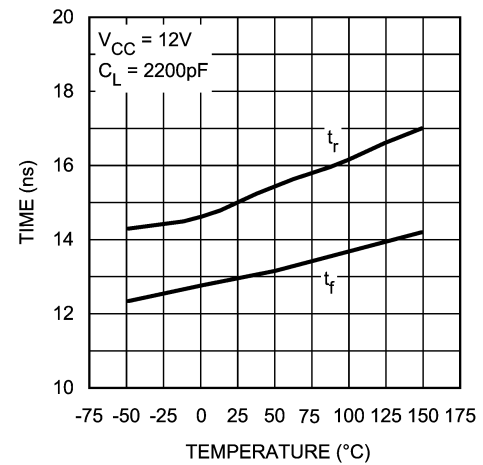
20112311

### Rise and Fall Time vs Supply Voltage



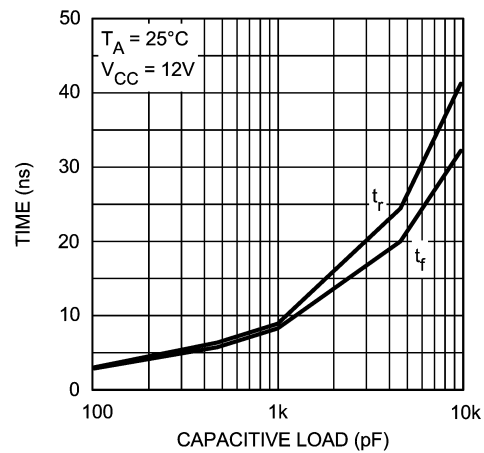
20112312

### Rise and Fall Time vs Temperature



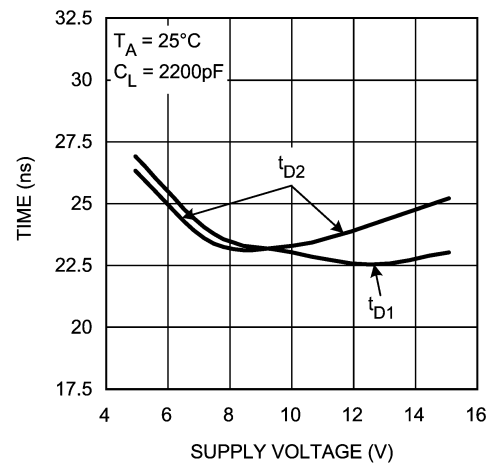
20112313

### Rise and Fall Time vs Capacitive Load



20112314

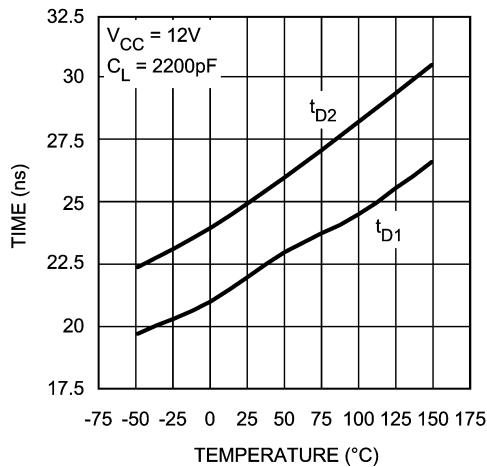
### Delay Time vs Supply Voltage



20112315

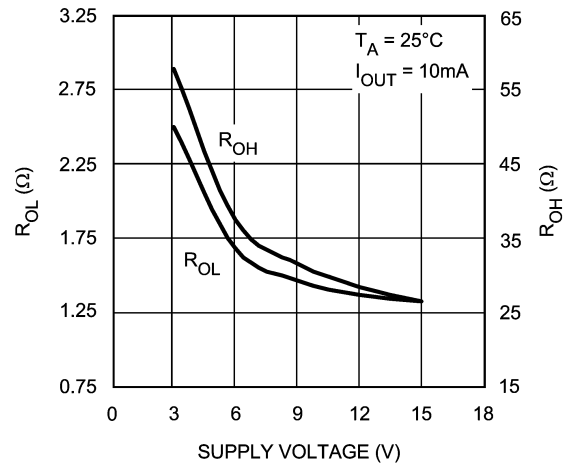
## Typical Performance Characteristics (Continued)

Delay Time vs Temperature



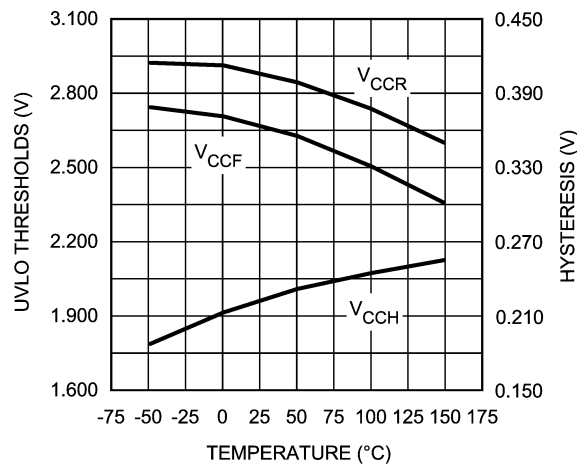
20112316

RDSON vs Supply Voltage



20112317

UVLO Thresholds and Hysteresis vs Temperature



20112318

## Detailed Operating Description

LM5111 dual gate driver consists of two independent and identical driver channels with TTL compatible logic inputs and high current totem-pole outputs that source or sink current to drive MOSFET gates. The driver output consist of a compound structure with MOS and bipolar transistor operating in parallel to optimize current capability over a wide output voltage and operating temperature range. The bipolar device provides high peak current at the critical threshold region of the MOSFET VGS while the MOS devices provide rail-to-rail output swing. The totem pole output drives the MOSFET gate between the gate drive supply voltage  $V_{CC}$  and the power ground potential at the  $V_{EE}$  pin.

The control inputs of the drivers are high impedance CMOS buffers with TTL compatible threshold voltages. The LM5111 pinout was designed for compatibility with industry standard gate drivers in single supply gate driver applications.

The two driver channels of the LM5111 are designed as identical cells. Transistor matching inherent to integrated circuit manufacturing ensures that the AC and DC performance of the channels are nearly identical. Closely matched propagation delays allow the dual driver to be

operated as a single with inputs and output pins connected. The drive current capability in parallel operation is precisely 2X the drive of an individual channel. Small differences in switching speed between the driver channels will produce a transient current (shoot-through) in the output stage when two output pins are connected to drive a single load. The efficiency loss for parallel operation has been characterized at various loads, supply voltages and operating frequencies. The power dissipation in the LM5111 increases by less than 1% relative to the dual driver configuration when operated as a single driver with inputs/ outputs connected.

An Under Voltage Lock Out (UVLO) circuit is included in the LM5111, which senses the voltage difference between  $V_{CC}$  and the chip ground pin,  $V_{EE}$ . When the  $V_{CC}$  to  $V_{EE}$  voltage difference falls below 2.8V both driver channels are disabled. The UVLO hysteresis prevents chattering during brown-out conditions and the driver will resume normal operation when the  $V_{CC}$  to  $V_{EE}$  differential voltage exceeds approximately 3.0V.

The LM5111 is available in dual non-inverting (-1), dual Inverting (-2) and the combination inverting plus non-inverting (-3) configurations. All three configurations are offered in the SOIC-8 plastic package.

## Layout Considerations

Attention must be given to board layout when using LM5111. Some important considerations include:

1. A Low ESR/ESL capacitor must be connected close to the IC and between the  $V_{CC}$  and  $V_{EE}$  pins to support high peak currents being drawn from  $V_{CC}$  during turn-on of the MOSFET.
2. Proper grounding is crucial. The drivers need a very low impedance path for current return to ground avoiding inductive loops. The two paths for returning current to ground are a) between LM5111  $V_{EE}$  pin and the ground of the circuit that controls the driver inputs, b) between LM5111  $V_{EE}$  pin and the source of the power MOSFET being driven. All these paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance. All these ground paths should be kept distinctly separate to avoid coupling between the high current output paths and the logic signals that drive the LM5111. A good method is to dedicate one copper plane in a multi-layered PCB to provide a common ground surface.
3. With the rise and fall times in the range of 10 ns to 30 ns, care is required to minimize the lengths of current carrying conductors to reduce their inductance and EMI from the high di/dt transients generated by the LM5111.
4. The LM5111 SOIC footprint is compatible with other industry standard drivers including the TC4426/27/28 and UCC27323/4/5.
5. If either channel is not being used, the respective input pin (IN\_A or IN\_B) should be connected to either  $V_{EE}$  or  $V_{CC}$  to avoid spurious output signals.

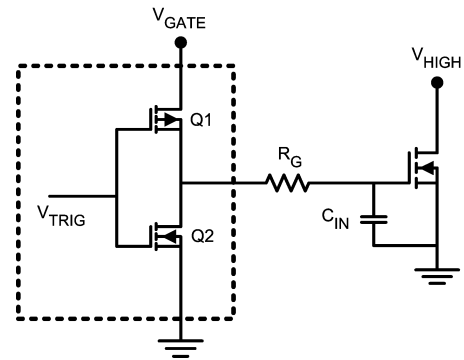
## Thermal Performance

### INTRODUCTION

The primary goal of thermal management is to maintain the integrated circuit (IC) junction temperature ( $T_J$ ) below a specified maximum operating temperature to ensure reliability. It is essential to estimate the maximum  $T_J$  of IC components in worst case operating conditions. The junction temperature is estimated based on the power dissipated in the IC and the junction to ambient thermal resistance  $\theta_{JA}$  for the IC package in the application board and environment. The  $\theta_{JA}$  is not a given constant for the package and depends on the printed circuit board design and the operating environment.

### DRIVE POWER REQUIREMENT CALCULATIONS IN LM5111

The LM5111 dual low side MOSFET driver is capable of sourcing/sinking 3A/5A peak currents for short intervals to drive a MOSFET without exceeding package power dissipation limits. High peak currents are required to switch the MOSFET gate very quickly for operation at high frequencies.



20112307

FIGURE 2.

The schematic above shows a conceptual diagram of the LM5111 output and MOSFET load. Q1 and Q2 are the switches within the gate driver.  $R_G$  is the gate resistance of the external MOSFET, and  $C_{IN}$  is the equivalent gate capacitance of the MOSFET. The gate resistance  $R_G$  is usually very small and losses in it can be neglected. The equivalent gate capacitance is a difficult parameter to measure since it is the combination of  $C_{GS}$  (gate to source capacitance) and  $C_{GD}$  (gate to drain capacitance). Both of these MOSFET capacitances are not constants and vary with the gate and drain voltage. The better way of quantifying gate capacitance is the total gate charge  $Q_G$  in coulombs.  $Q_G$  combines the charge required by  $C_{GS}$  and  $C_{GD}$  for a given gate drive voltage  $V_{GATE}$ .

Assuming negligible gate resistance, the total power dissipated in the MOSFET driver due to gate charge is approximated by

$$P_{DRIVER} = V_{GATE} \times Q_G \times F_{SW}$$

Where

$F_{SW}$  = switching frequency of the MOSFET.

For example, consider the MOSFET MTD6N15 whose gate charge specified as 30 nC for  $V_{GATE} = 12V$ .

The power dissipation in the driver due to charging and discharging of MOSFET gate capacitances at switching frequency of 300 kHz and  $V_{GATE}$  of 12V is equal to

$$P_{DRIVER} = 12V \times 30 \text{ nC} \times 300 \text{ kHz} = 0.108W.$$

If both channels of the LM5111 are operating at equal frequency with equivalent loads, the total losses will be twice as this value which is 0.216W.

In addition to the above gate charge power dissipation, - transient power is dissipated in the driver during output transitions. When either output of the LM5111 changes state, current will flow from  $V_{CC}$  to  $V_{EE}$  for a very brief interval of time through the output totem-pole N and P channel MOSFETs. The final component of power dissipation in the driver is the power associated with the quiescent bias current consumed by the driver input stage and Under-voltage lockout sections.

Characterization of the LM5111 provides accurate estimates of the transient and quiescent power dissipation components. At 300 kHz switching frequency and 30 nC load used in the example, the transient power will be 8 mW. The 1 mA nominal quiescent current and 12V  $V_{GATE}$  supply produce a 12 mW typical quiescent power.

Therefore the total power dissipation

$$P_D = 0.216 + 0.008 + 0.012 = 0.236W.$$



## Thermal Performance (Continued)

We know that the junction temperature is given by

$$T_J = P_D \times \theta_{JA} + T_A$$

Or the rise in temperature is given by

$$T_{RISE} = T_J - T_A = P_D \times \theta_{JA}$$

For SOIC-8 package  $\theta_{JA}$  is estimated as 170°C/W for the conditions of natural convection.

Therefore  $T_{RISE}$  is equal to

$$T_{RISE} = 0.236 \times 170 = 40.1^\circ\text{C}$$

### CONTINUOUS CURRENT RATING OF LM5111

The LM5111 can deliver pulsed source/sink currents of 3A and 5A to capacitive loads. In applications requiring continuous load current (resistive or inductive loads), package power dissipation, limits the LM5111 current capability far below the 5A sink/3A source capability. Rated continuous current can be estimated both when sourcing current to or sinking current from the load. For example when sinking, the maximum sink current can be calculated as:

$$I_{SINK} (MAX) := \sqrt{\frac{T_J(MAX) - T_A}{\theta_{JA} \cdot R_{DS} (ON)}}$$

where  $R_{DS(on)}$  is the on resistance of lower MOSFET in the output stage of LM5111.

Consider  $T_J(max)$  of 125°C and  $\theta_{JA}$  of 170°C/W for an SO-8 package under the condition of natural convection and no air

flow. If the ambient temperature ( $T_A$ ) is 60°C, and the  $R_{DS(on)}$  of the LM5111 output at  $T_J(max)$  is 2.5Ω, this equation yields  $I_{SINK(max)}$  of 391mA which is much smaller than 5A peak pulsed currents.

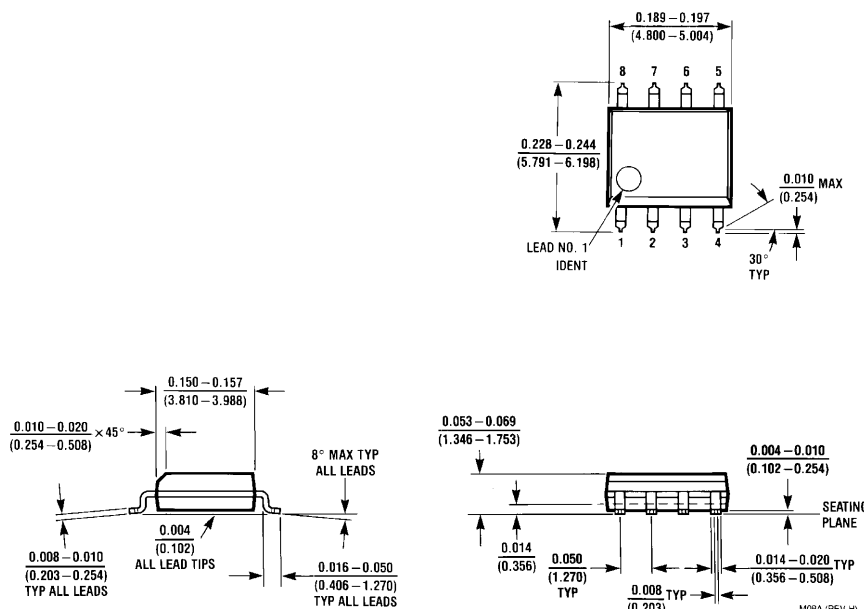
Similarly, the maximum continuous source current can be calculated as

$$I_{SOURCE} (MAX) := \frac{T_J(MAX) - T_A}{\theta_{JA} \cdot V_{DIODE}}$$

where  $V_{DIODE}$  is the voltage drop across hybrid output stage which varies over temperature and can be assumed to be about 1.1V at  $T_J(max)$  of 125°C. Assuming the same parameters as above, this equation yields  $I_{SOURCE(max)}$  of 347mA.

**Physical Dimensions** inches (millimeters)

unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH TO BE 200 MICRONS/5.08 MICROMETERS MINIMUM LEAD/TIN(SOLDER) ON COPPER.
2. DIMENSION DOES NOT INCLUDE MOLD FLASH.
3. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA, DATED MAY 1990.

**8-Lead SOIC Package**  
**NS Package Number M08A**

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**BANNED SUBSTANCE COMPLIANCE**

National Semiconductor certifies that the products and packing materials meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.



**National Semiconductor**  
**Americas Customer**  
**Support Center**  
 Email: new.feedback@nsc.com  
 Tel: 1-800-272-9959

www.national.com

**National Semiconductor**  
**Europe Customer Support Center**  
 Fax: +49 (0) 180-530 85 86  
 Email: europe.support@nsc.com  
 Deutsch Tel: +49 (0) 69 9508 6208  
 English Tel: +44 (0) 870 24 0 2171  
 Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**  
**Asia Pacific Customer**  
**Support Center**  
 Email: ap.support@nsc.com

**National Semiconductor**  
**Japan Customer Support Center**  
 Fax: 81-3-5639-7507  
 Email: jpn.feedback@nsc.com  
 Tel: 81-3-5639-7560