SII
Seiko Instruments

G2446/G242C/G321D

LIQUID CRYSTAL DISPLAY MODULE WITH FL BACKLIGHTING

USER'S MANUAL

1. SPECIFICATION

1.1 General

The G2446, G242C, and G321D are thin liquid crystal display (LCD) module that consist of full dot matrix LCD panel, CMOS LSIs and FL backlight. also CMOS graphic LCD controller, SED1330FB (EPSON), can be built in the LCD module. The panel features a wide viewing angle and high contrast black and white display. The full dot matrix structure allows both graphics and character display. In addition, the display is clear and stable, with no image warping or position skew, because the display position is specified by the intersection of transparent electrodes in a matrix.

1.2 Features

-Full dot matrix structure and duty

G2446	240 dots × 64 dots	1/64 duty
G242C	240 dots × 128 dots	1/128 duty
G321D	320 dots × 200 dots	1/200 duty

-Transmissive type STN LCD Black and White mode using retardation control film

-Negative mode

Display data "H"(display ON) : White

Display data "L"(display OFF) : Black

-Built in Controller SED1330FBA (EPSON)

-Built in display RAM

G2446	8K bytes RAM
G242C	8K bytes RAM
G321D	32K bytes RAM

-Power supply

G2446	Single power supply	Vdd = +5V	built in DC/DC converter
G242C	Single power supply	Vdd = +5V	built in DC/DC converter
G321D	Two power supply	Vdd = +5V	Vlcd = -24V

-Contrast adjustment (V0)

-Built in FL backlight what is side edge type and using one CCFL

-Weight

G2446	200g typ.
G242C	280g typ.
G321D	350g typ.

1.3 Standard specification

Model name	LCD	Controller and Display RAM	Light source	Viewing angle
G2446X5R1AC	Black and White mode using retardation control film Antiglare	Built in the LCD module	Transmissive LCD FL backlighting	12 o'clock
G242CX5R1AC	Black and White mode using retardation control film Antiglare	Built in the LCD module	Transmissive LCD FL backlighting	12 o'clock
G321DX5R1AC	Black and White mode using retardation control film Antiglare	Built in the LCD module	Transmissive LCD FL backlighting	12 o'clock

Model name	LCD	Controller and Display RAM	Light source	Viewing angle
G2446X5R1A0	Black and White mode using retardation control film Antiglare	Not built in the LCD module	Transmissive LCD FL backlighting	12 o'clock
G242CX5R1A0	Black and White mode using retardation control film Antiglare	Not built in the LCD module	Transmissive LCD FL backlighting	12 o'clock
G321DX5R1A0	Black and White mode using retardation control film Antiglare	Not built in the LCD module	Transmissive LCD FL backlighting	12 o'clock

1.4 Absolute maximun ratings

1.4.1 G2446

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD		-0.3	6	V
	VLC**		VDD - 20	VDD	V
	V0*	V0 => VLC	VDD - 20	VDD	V
Input voltage	Vin		- 0.3	VDD + 0.3	V
Operating temperature	Topr		0	+ 50	°C
Storage temperature	Tstg		- 20	+ 60	°C
Storage humidity		<= 48 hrs	20	85	%R
		<= 1000 hrs	20	65	%R

1.4.2 G242C

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD		-0.3	6	V
	VLC**		VDD - 30	VDD	V
	V0*	V0 => VLC	VDD - 30	VDD	V
Input voltage	Vin		- 0.3	VDD + 0.3	V
Operating temperature	Topr		0	+ 50	°C
Storage temperature	Tstg		- 20	+ 60	°C
Storage humidity		<= 48 hrs	20	85	%R
		<= 1000 hrs	20	65	%R

1.4.3 G321D

Item	Symbol	Condition	Min	Max	Unit
Power supply voltage	VDD		-0.3	6	V
	VLC**		VDD - 30	VDD	V
	V0*	V0 => VLC	VDD - 30	VDD	V
Input voltage	Vin		- 0.3	VDD + 0.3	V
Operating temperature	Topr		0	+ 50	°C
Storage temperature	Tstg		- 20	+ 60	°C
Storage humidity		<= 48 hrs	20	85	%R
		<= 1000 hrs	20	65	%R

General condition VSS = 0V

* V0 is used when the DC/DC converter is used (G2446 and G242C) , and the contrast is adjusted by external potentiometer

** VLC is used when the DC/DC converter is not used (G2446 and G242C)

1.5 Electrical characteristics of controller built_in type (Excluding FL backlighting)

1.5.1 G2446

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC*1	VDD=5V	- 22.0	- 7.8	- 3.0	V
Input voltage*3	High	VIH	VDD=5V±5%	2.2	-	VDD+0.3	V
	Low	VIL		- 0.3	-	0.8	V
Input voltage*4	High	VIH	VDD=5V±5%	0.8VDD	-	-	V
	Low	VIL		-	-	0.2VDD	V
Input voltage*5	High	VIH	VDD=5V±5%	0.5VDD	0.7VDD	0.8VDD	V
	Low	VIL		0.2VDD	0.3VDD	0.5VDD	V
Output voltage*6	High	VOH	IHO=-5.0mA	2.4	-	-	V
	Low	VOL	IOL=5.0mA	-	-	0.4	V
Current consumption		IDD*2	TA=25°C	-	15	30	mA

1.5.2 G242C

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC*1	VDD=5V	- 22.0	- 12.0	- 3.0	V
Input voltage*3	High	VIH	VDD=5V±5%	2.2	-	VDD+0.3	V
	Low	VIL		- 0.3	-	0.8	V
Input voltage*4	High	VIH	VDD=5V±5%	0.8VDD	-	-	V
	Low	VIL		-	-	0.2VDD	V
Input voltage*5	High	VIH	VDD=5V±5%	0.5VDD	0.7VDD	0.8VDD	V
	Low	VIL		0.2VDD	0.3VDD	0.5VDD	V
Output voltage*6	High	VOH	IHO=-5.0mA	2.4	-	-	V
	Low	VOL	IOL=5.0mA	-	-	0.4	V
Current consumption		IDD*2	TA=25°C	-	40	50	mA

1.5.3 G321D

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC	VDD=5V V0=>VLC	- 24.5	- 24.0	- 23.5	V
		V0		- 22.0	- 17.0	- 3.0	V
Input voltage*3	High	VIH	VDD=5V±5%	2.2	-	VDD+0.3	V
	Low	VIL		- 0.3	-	0.8	V
Input voltage*4	High	VIH	VDD=5V±5%	0.8VDD	-	-	V
	Low	VIL		-	-	0.2VDD	V
Input voltage*5	High	VIH	VDD=5V±5%	0.5VDD	0.7VDD	0.8VDD	V
	Low	VIL		0.2VDD	0.3VDD	0.5VDD	V
Output voltage*6	High	VOH	IHO=-5.0mA	2.4	-	-	V
	Low	VOL	IOL=5.0mA	-	-	0.4	V
Current consumption		IDD	Ta=25°C	-	23	30	mA
		ILC		-	6	12	mA

*1 VLC is used when the internal DC/DC converter is not used

*2 Current consumption is the addition of logic circuit consumption+ILC+DC/DC converter

*3 Applied to $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, A0 , DB0 ~ DB7

*4 Applied to $\overline{SEL1}$, $\overline{SEL2}$

*5 Applied to $\overline{RES}$

*6 Applied to DB0 ~ DB7

1.6 Electrical characteristics of controller not_built_in type (Excluding FL backlighting)

1.6.1 G2446

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC*	VDD=5V	- 22.0	- 7.8	- 3.0	V
Input voltage	High	VIH	VDD=5V±5%	0.8VDD	-	VDD	V
	Low	VIL		0	-	0.2VDD	V
Current consumption		IDD**	TA=25°C	-	12	22	mA

1.6.2 G242C

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC*	VDD=5V	- 22.0	- 12.0	- 3.0	V
Input voltage	High	VIH	VDD=5V±5%	0.8VDD	-	VDD	V
	Low	VIL		0	-	0.2VDD	V
Current consumption		IDD**	TA=25°C	-	30	40	mA

1.6.3 G321D

Item		Symbol	Condition	Min	Typ	Max	Unit
power supply voltage		VDD		4.75	5.00	5.25	V
		VLC	VDD=5.0V V0=>VLC	- 24.5	- 24.0	- 23.5	V
		V0		- 22.0	- 17.0	- 3.0	V
Input voltage	High	VIH	VDD=5V±5%	0.8VDD	-	VDD	V
	Low	VIL		0	-	0.2VDD	V
Current consumption		IDD	Ta=25°C	-	8	15	mA
		ILC		-	6	12	mA

* VLC is used when the internal DC/DC converter is not used

** IDD is the addition of logic circuit consumption + ILC + DC/DC converter

1.7 Optical characteristics (When FL backlight is ON)

1.7.1 G2446

Item	Symbol	Conditions	Min	Typ	Max	Reference
Viewing angle	θ2–θ1	C = 2.0 , ϕ =180°	70°	-	-	Note1 and 2
Contrast	C	θ = -5° , ϕ =180°	5	6	-	Note3
Response time Ton	ton	θ = 0° , ϕ =180°	-	-	490	Note4
Response time Toff	toff		-	-	410	Note5

1.7.2 G242C

Item	Symbol	Conditions	Min	Typ	Max	Reference
Viewing angle	θ2–θ1	C = 2.0 , ϕ =180°	55°	-	-	Note1 and 2
Contrast	C	θ = -5° , ϕ =180°	5	6	-	Note3
Response time Ton	ton	θ = 0° , ϕ =180°	-	-	490	Note4
Response time Toff	toff		-	-	410	Note5

1.7.3 G321D

Item	Symbol	Conditions	Min	Typ	Max	Reference
Viewing angle	θ2–θ1	C = 2.0 , ϕ =180°	55°	-	-	Note1 and 2
Contrast	C	θ = -5° , ϕ =180°	5	6	-	Note3
Response time Ton	ton	θ = 0° , ϕ =180°	-	-	490	Note4
Response time Toff	toff		-	-	410	Note5

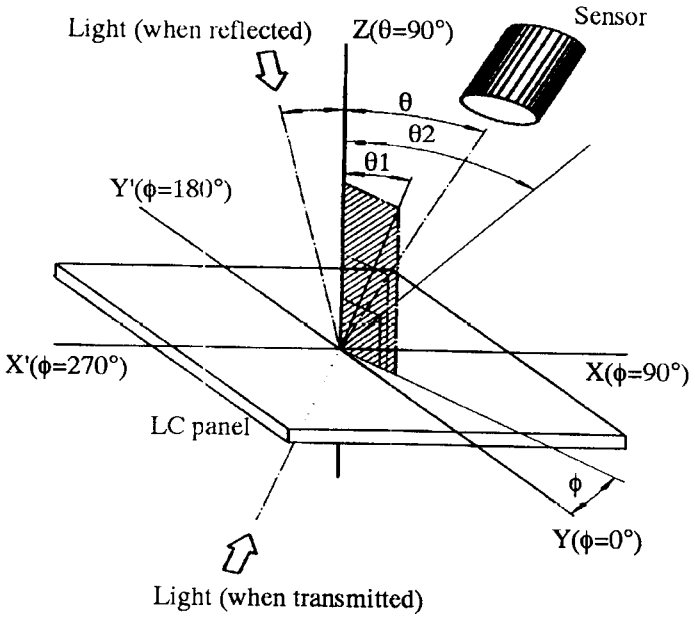
General conditions are as indicated below,

1) G2446
- -Ta=25°C
- -1/64 duty
- -1/8.7 bias
- -Vopr=12.8V

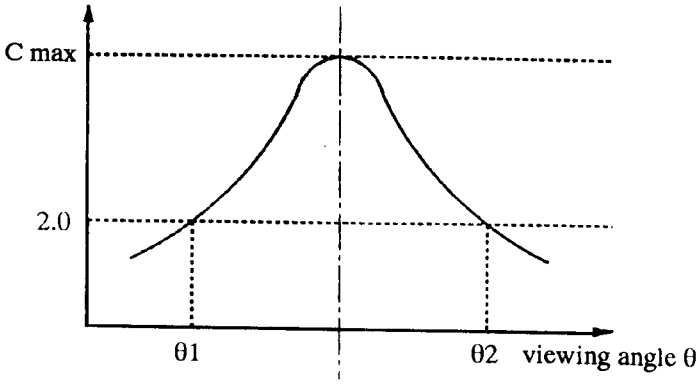
2) G242C
- -Ta=25°C
- -1/128 duty
- -1/12.2 bias
- -Vopr=17.0V

3) G321D
- -Ta=25°C
- -1/200 duty
- -1/14.9 bias
- -Vopr=22.0V

Note1 : Definition of angles θ and ϕ

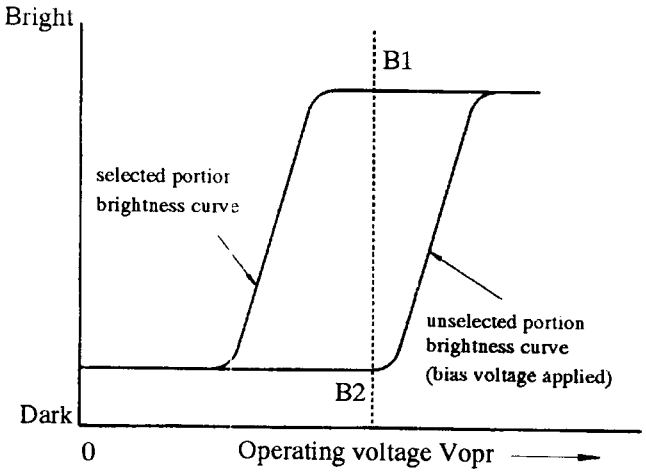


Note2 : Definition of viewing angle θ1 and θ2



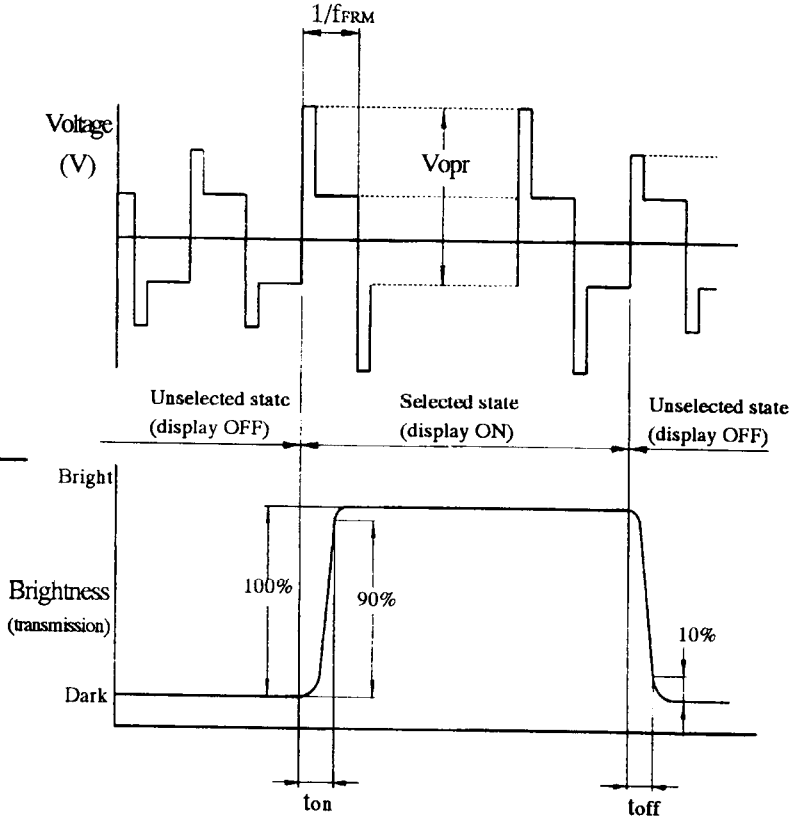
* Optimum vision with the naked eye and viewing angle θ at C max above are not always the same.

Note3 : Definition of contrast C



$$C = \frac{\text{B1 (brightness of selected portion)}}{\text{B2(brightness of unselected portion)}}$$

Note4 : Definition of response time



Vopr : Operating voltage fFRM : Frame frequency

ton : Response time toff : Response time

1.8 I/O Terminal functions

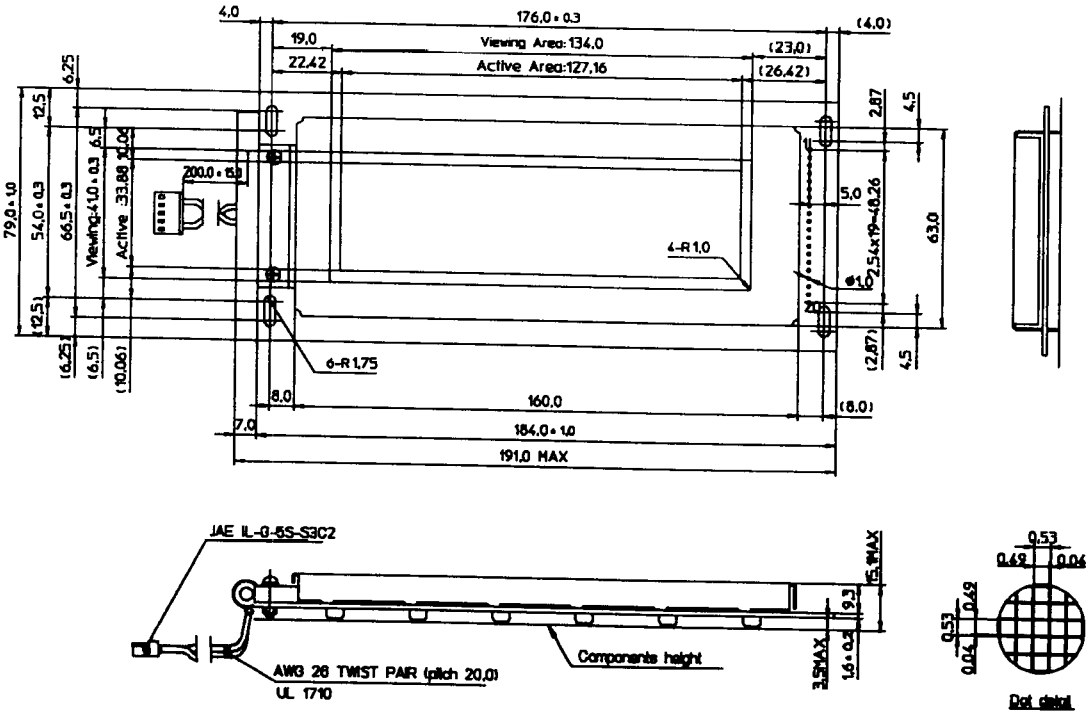
No.	Without controller		With controller	
	Name	Function	Name	Function
1	NC	Not connected	/RES	Reset
2	NC	Not connected	/RD	Read
3	NC	Not connected	/WR	Write
4	NC	Not connected	SEL1	SEL1,SEL2: 008080;SEL1,SEL2: 10 6800
5	NC	Not connected	SEL2	MPU interface configuration
6	NC	Not connected	/CS	SED 1330 chip select
7	INHX	Display ON/OFF control signal (H: on L: off)	A0	Command mode set
8	D0	Display data input	DB0	Data bus
9	D1	Display data input	DB1	Data bus
10	D2	Display data input	DB2	Data bus
11	D3	Display data input	DB3	Data bus
12	FLM	Input scan start-up pulse	DB4	Data bus
13	M	Liquid crystal AC drive control signal	DB5	Data bus
14	CL2	Display data shift clock	DB6	Data bus
15	CL1	Display data latch clock	DB7	Data bus
16	VDD	Logic power supply	VDD	Logic power supply
17	VSS	GND 0V	VSS	GND 0V
18	V0 *	Liquid crystal contrast adjustment	V0 *	Liquid crystal contrast adjustment
19	VLC **	Liquid crystal drive voltage	VLC **	Liquid crystal drive voltage
20	FGND	Frame ground	FGND	Frame ground

* V0 is used as a terminal when the DC/DC converter is used, and the contrast is adjusted by external potentiometer

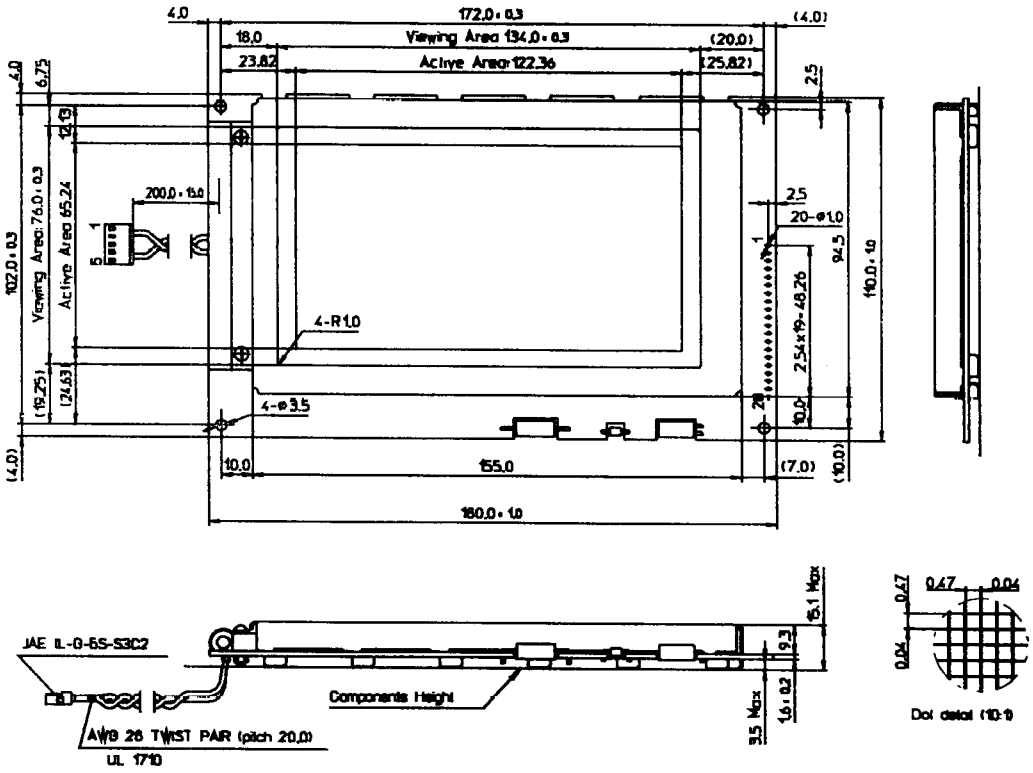
** VLC is used as a terminal when the DC/DC converter is not used

1.9 Dimensions

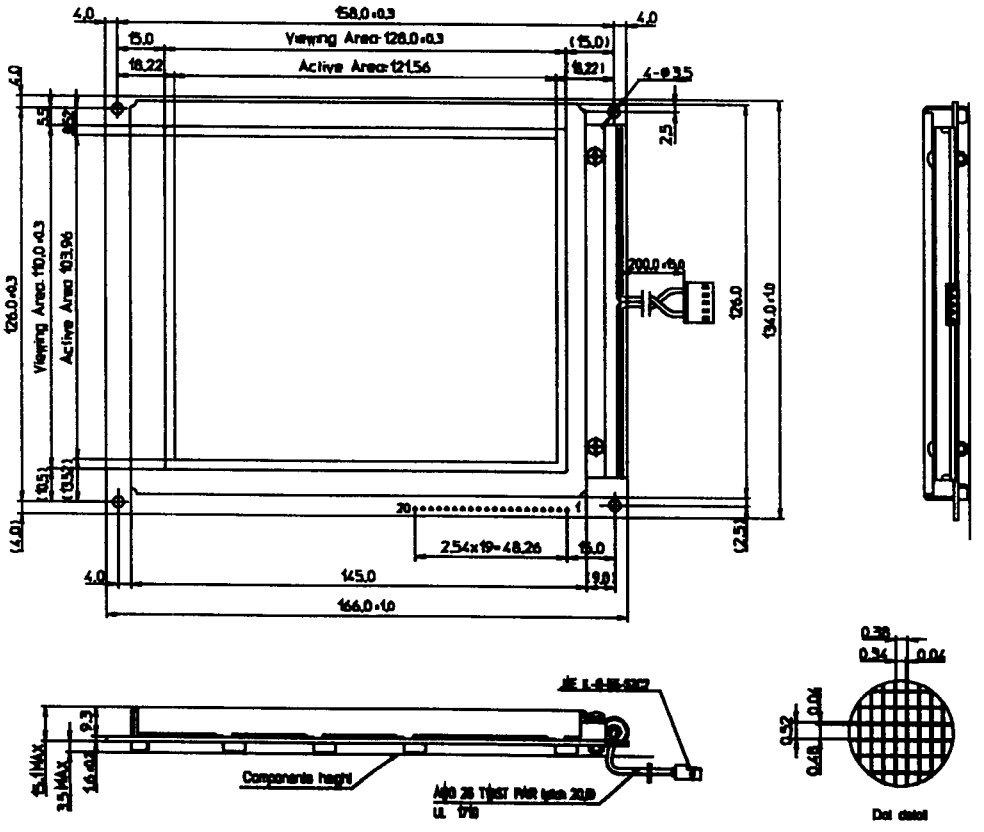
1.9.1 G2446 dimensions



1.9.2 G242C dimensions



1.9.3 G321D dimensions



2. CIRCUIT STRUCTURE

2.1 Liquid Crystal Driving Circuit

The drive waveform of the LCD panel is shown in Figure 2.1.1 on the next page. Since DC voltage will damage the liquid crystal, an AC voltage is applied between the two frames. The signal controlling this is the liquid crystal AC drive control signal (M). The display quality of some LCD panels may be improved by increasing the frequency of the liquid crystal AC drive waveform. For the G321D and the G242C the liquid crystal driving circuit includes a circuit that generates AC drive control signals (Mx) of higher frequency than M. The frequency of Mx signals is set according to the LCD panel so that the best display quality can be obtained. The frame frequency is normally set to about 70 Hz ± 3% to prevent screen flicker.

The common electrodes are selected within a frame by time division from electrode 1 to the last electrode of the display (Table 2.1.1).

Table 2.1.1

Display	Duty	Common electrodes
G2446	1 / 64	1 ~ 64
G242C	1 / 128	1 ~ 128
G321D	1 / 200	1 ~ 200

This is called line sequential scanning. When the common electrode is selected, the voltage level of the segment electrodes determines whether the dots at the intersection of the segment electrodes are selected or not. As shown in Table 2.1.2, there are six drive waveform voltage levels, VDD to VLC. The voltage between the segment and the common electrodes is thus applied to the liquid crystal.

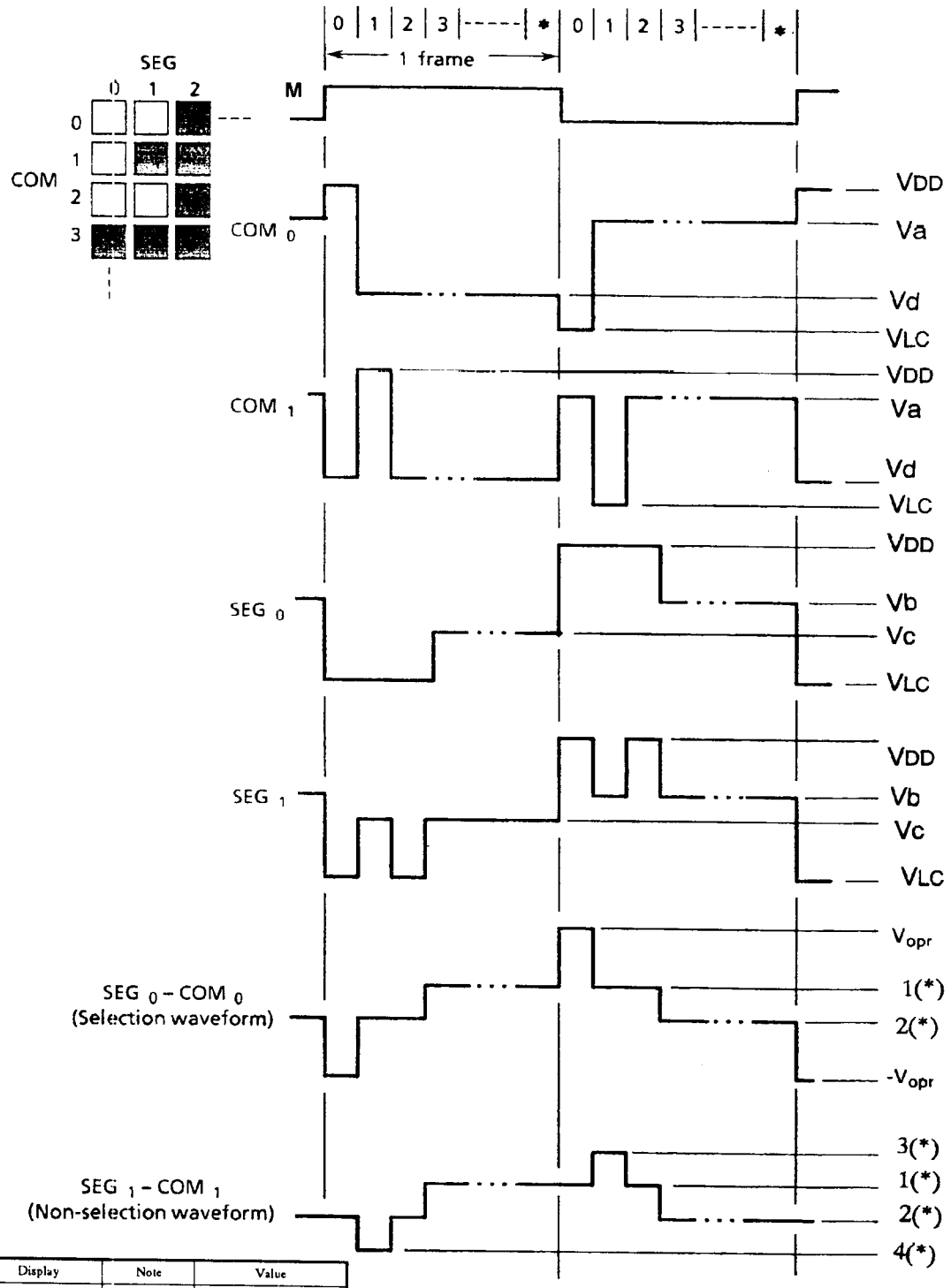
Table 2.1.2

VDD	Common and segment selection level
Va	Common non-selection level
Vb	Segment non-selection level
Vc	Segment non-selection level
Vd	Common non-selection level
VLC	Common and segment selection level

The selection waveform for SEG0 - COM0 and the non-selected waveform for SEG1 - COM1 are shown in Figure 2.1.1. The size of the effective voltage of the waveform determines whether the liquid crystal under the selected dots is in the selected or non-selected state.

Since the LCD is in the negative mode, the display data is white at "H" and black at "L".

Figure 2.1.1



Display	Note	Value
G2446	1(*)	1 / 8.7 Vopr
	2(*)	- 1 / 8.7 Vopr
	3(*)	6.7 / 8.7 Vopr
	4(*)	- 6.7 / 8.7 Vopr
G242C	1(*)	1 / 12.2 Vopr
	2(*)	- 1 / 12.2 Vopr
	3(*)	10.2 / 12.2 Vopr
	4(*)	-10.2 / 12.2 Vopr
G321D	1(*)	1 / 14.9 Vopr
	2(*)	- 1 / 14.9 Vopr
	3(*)	12.9 / 14.9 Vopr
	4(*)	- 12.9 / 14.9 Vopr

2.2 Circuit structure

2.2.1 G2446

The G2446 consists of common drivers, segment drivers, a bias voltage generation circuit and a DC/DC converter. Figure 2.2.1.1 shows the circuit block diagram.
The version with controller uses the SED1330 controller and 8kBytes of memory. Figure 2.2.1.2 shows the circuit block diagram.

2.2.2 G242C

The G242C consists of common drivers, segment drivers, a bias voltage generation circuit, an Mx generation circuit and a DC/DC converter. Figure 2.2.2.1 shows the circuit block diagram.
The version with controller uses the SED1330 controller and 8kBytes of memory. Figure 2.2.2.2 shows the circuit block diagram.

2.2.3 G321D

The G321D consists of common drivers, segment drivers, a bias voltage generation circuit and a Mx generation circuit. Figure 2.2.3.1 shows the circuit block diagram.
The version with controller uses the SED1330 controller and 32kBytes of memory. Figure 2.2.3.2 shows the circuit block diagram.

(1) Common driver (OKI MSM5298)

A common driver (CD) is a CMOS IC with 68 drive outputs.
G2446: 1 Common driver
G242C: 2 Common drivers
G321D: 3 Common drivers
They operate as follows. Input scan start-up pulse (FLM) is taken into the internal shift register by the falling edge trigger of the display data latch signal (CL1x), and sequentially shifted. After a number of CL1x input corresponding to the display duty, the next FLM is input and the same operation is repeated. As shown in Table 2.2(1).1, the common output is selected according to the shift register contents and the liquid crystal AC drive control signal (Mx) in the circuit, and the common drive waveform is formed. For the G2446, M and CL1 instead of Mx and CL1x are input to the CDs.

Table 2.2(1).1

Shift register content	Mx *	COM output
H	L	VDD
	H	VLC
L	L	Vd
	H	Va

* M instead of Mx for G2446

Figure 2.2.1.1

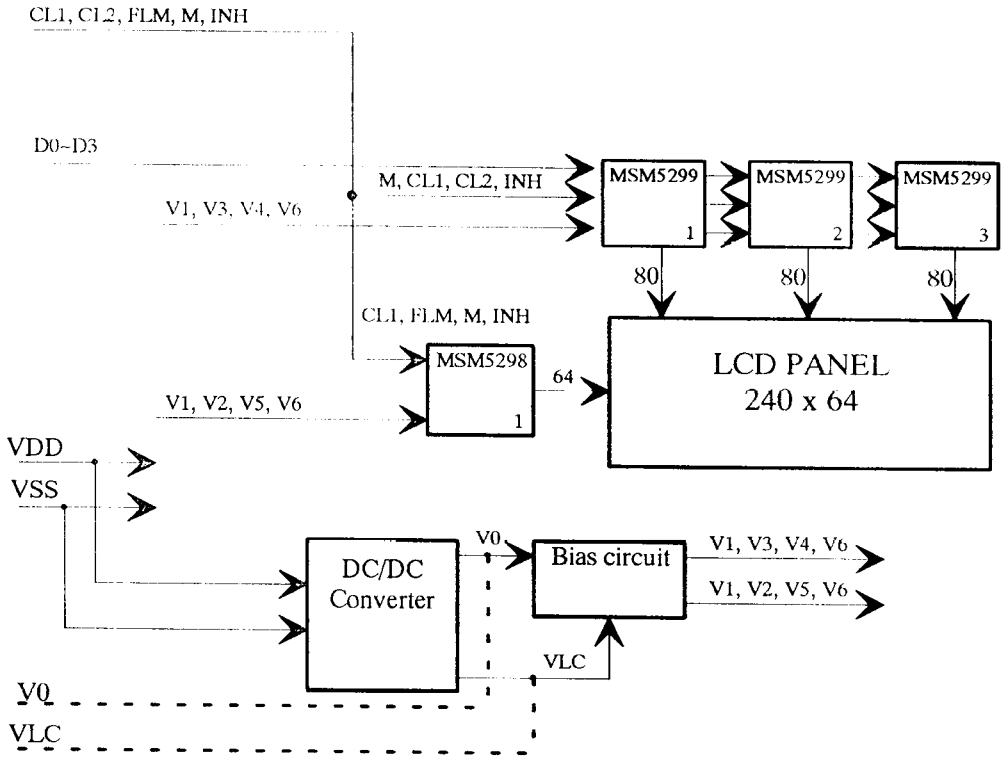


Figure 2.2.1.2

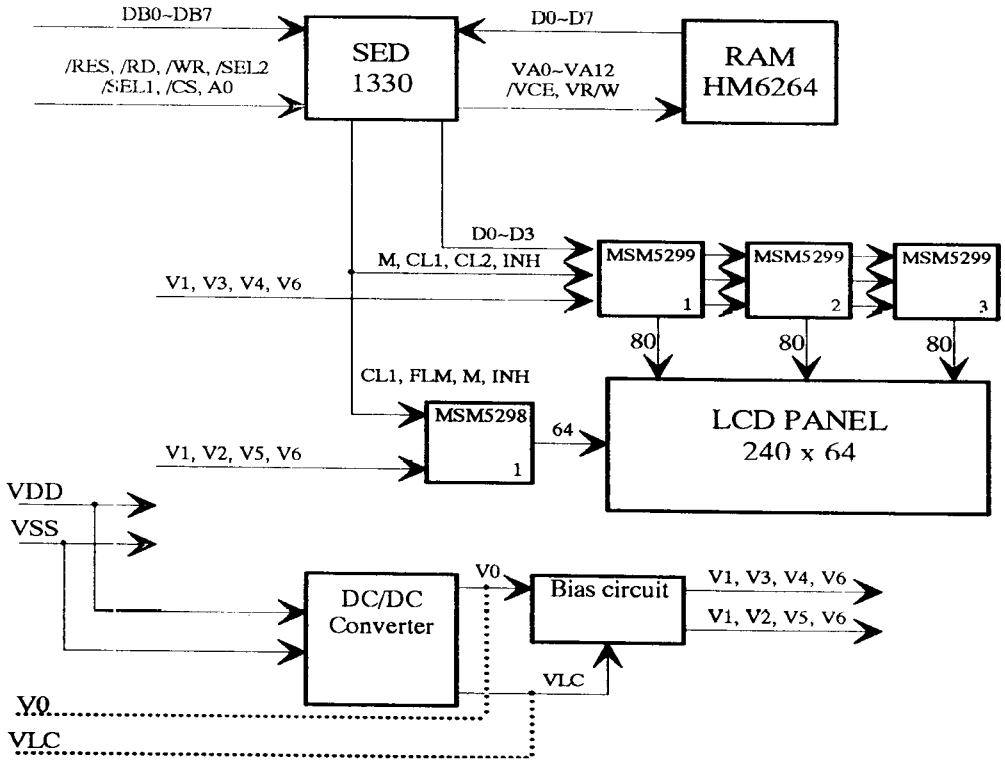


Figure 2.2.2.1

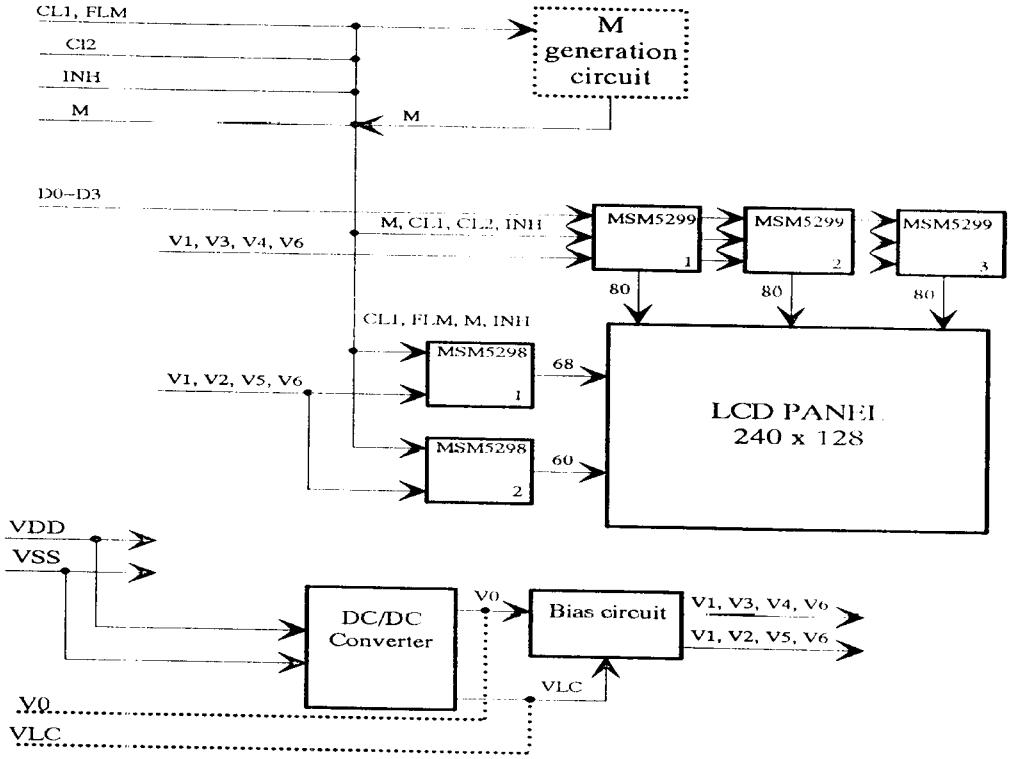


Figure 2.2.2.2

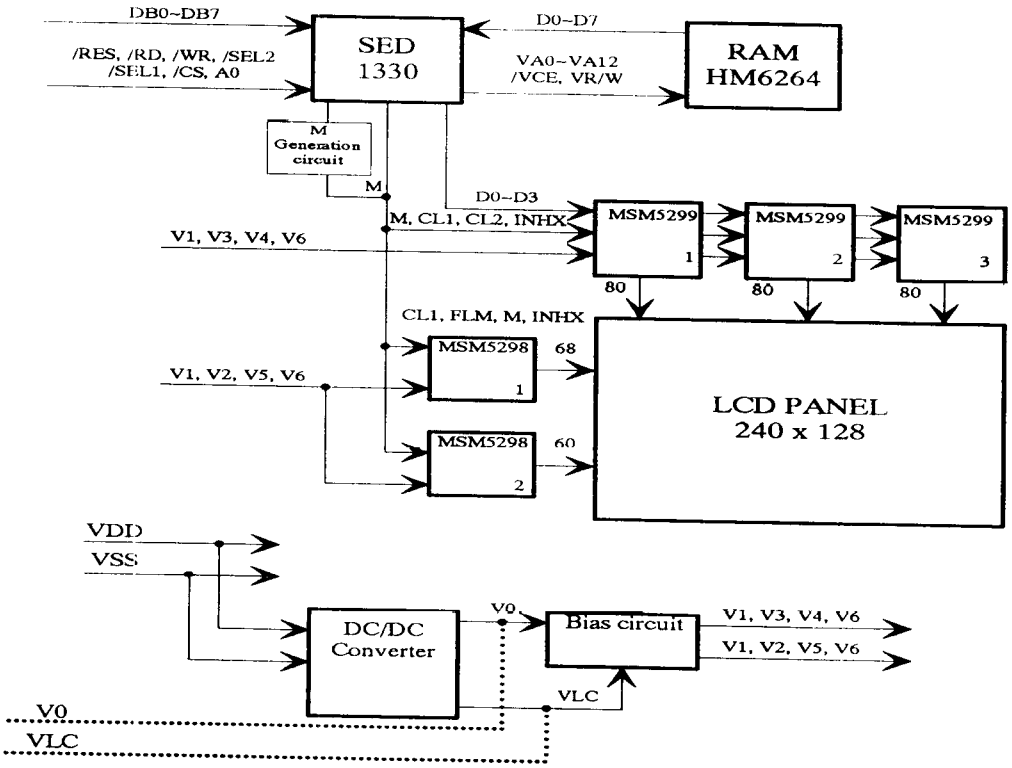


Figure 2.2.3.1

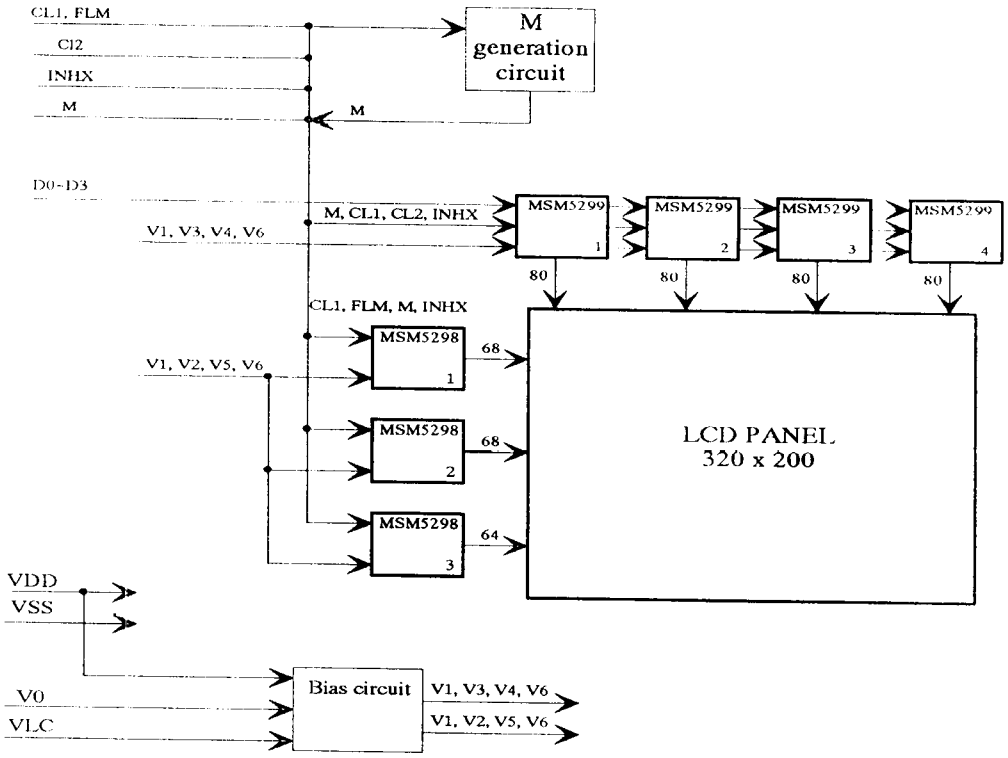
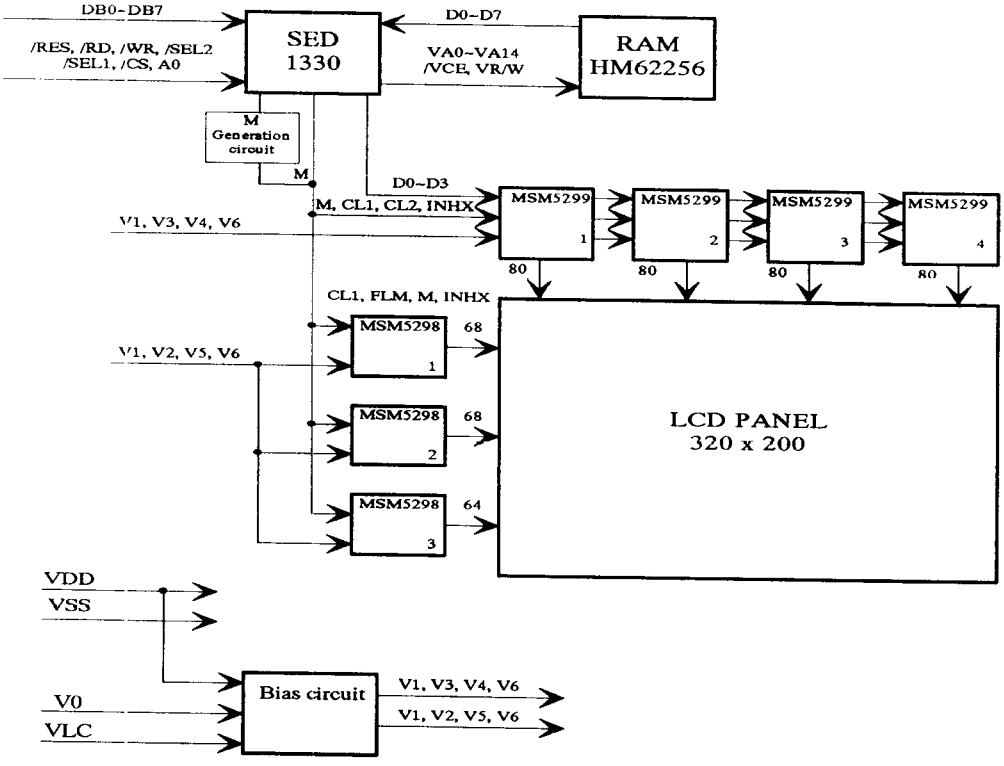


Figure 2.2.3.2



(2) Segment driver (OKI MSM5299B)

A segment driver (SD) is a CMOS IC with 80 drive outputs.
G2446: 3 Segment drivers
G242C: 3 Segment drivers
G323D: 4 Segment drivers
They operate as follows. Input four-bit data is sequentially taken into the internal register of SD by the falling edge trigger of the display data shift clock (CL2). SD has a chip enable function. After 80 bits of data are taken into SD1, the next data is automatically taken into SD2. 240 bits can be taken into the segment drivers of G242C and G2446, 320 bits can be taken into the segment drivers of G321D. The display data taken into internal registers are latched by the falling edge trigger of CL1x. As shown in Table 2.2(2).1, the segment output is selected according to the display data and the liquid crystal AC drive control signal (Mx) in the circuit, and the segment drive waveform is formed. For the G2446, M instead of Mx is input to the SDs.

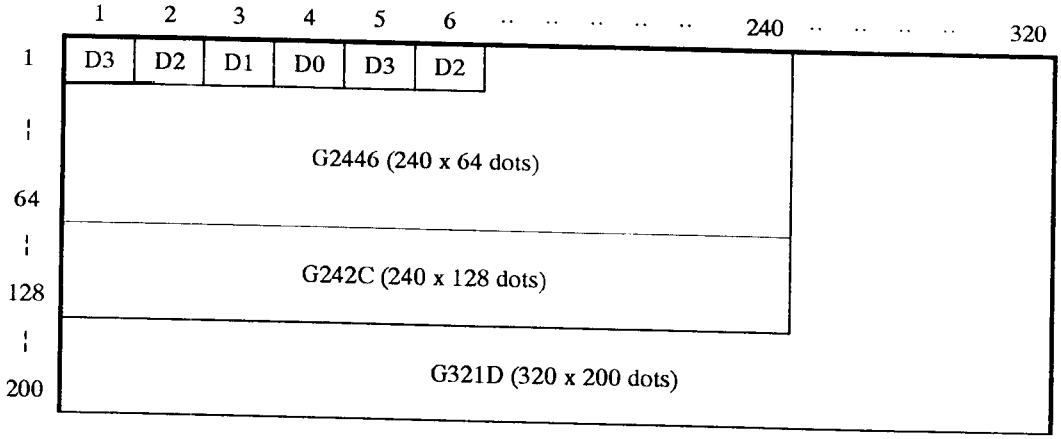
Table 2.2(2).1

Display data	Mx *	SEG output
H	L	VLC
	H	VDD
L	L	Vc
	H	Vb

* M instead of Mx for G2446

The relationship between the dislay data and display screen is shown in Figure 2.2(2).2.

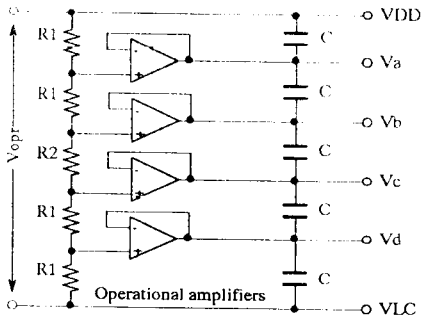
Figure 2.2(2).2



(3) Bias voltage generation circuit

Six levels of voltage, VDD to VLC, are applied to the common and segment drivers. The voltage is generated through operational amplifier by resistance-division from liquid crystal operating voltage (Vopr). Here, an operational amplifier is used as a voltage follower. See Figure 2.2(3).1

Figure 2.2(3).1



Also, display screen contrast and viewing angle are influenced by the ambient temperature. See Table 2.2(3).2 for the recommended Vopr level at different temperatures. See also (5) DC/DC Converter.

Table 2.2(3).2

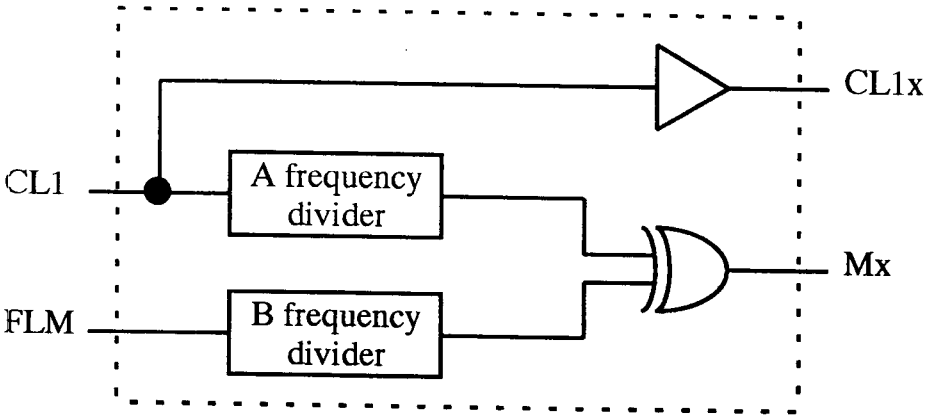
Display module	Recommended Vopr (V)		
	0 °C	25 °C	50 °C
G2446	13.8	12.8	11.8
G242C	18.0	17.0	16.2
G321D	23	22	20.8

(4) Mx generation circuit (G321D and G242C)

As shown in Figure 2.2(4).1, the Mx generation circuit takes Ex-OR from a display data latch signal (CL1) on which A time division is performed and a scan start-up pulse (FLM) on which B time division is performed, and outputs liquid crystal AC drive control signal Mx. Values A and B are set according to the LCD panel so that the best display quality can be obtained and the drive voltage can be alternated.

CL1x is the buffer output of CL1.

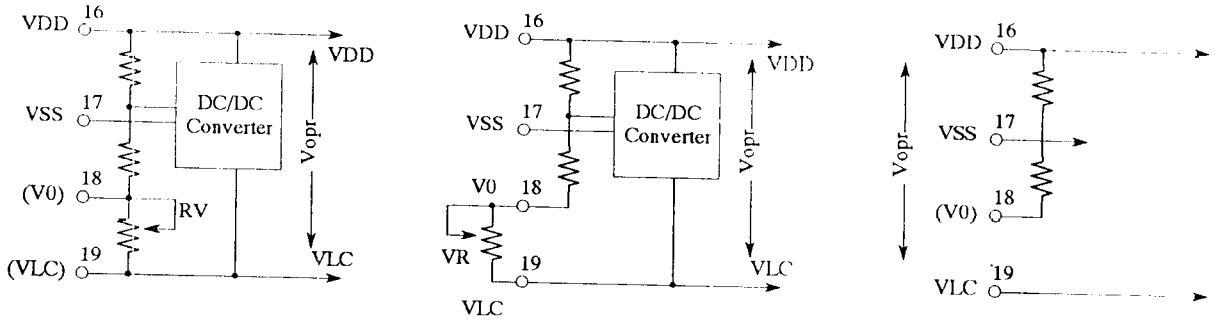
Figure 2.2(4).1



(5) DC/DC converter (G242C and G2446)

As shown in Figure 2.2(5).1, the liquid crystal drive voltage (VLC) is obtained from the power supply voltage (VDD, +5V). VLC is a negative value voltage. The operating voltage is defined in the following way: Vopr = VDD - VLC. The display screen contrast can be changed by turning the trimmer RV on the PCB.

Figure 2.2(5).1



Terminal 18 (V0) and 19 (VLC) are used as an input terminal when the DC/DC converter is used, and the contrast is adjusted by external variable resistor (VR); for the value of this resistor, see Table 2.2(5).2. In this case the trimmer RV is not assembled on the PCB.

Terminal 19 (VLC) is used as an input terminal when the DC/DC converter is not assembled. In this case the liquid crystal drive voltage VLC must be supplied.

Table 2.2(5).2

Display module	Resistor value
G2446	100 k ohm
G242C	6.8 k ohm

(6) Controller circuit

The SED1330 LCD controller IC generates all the signals required by the display memory and by the common and segment drivers, and has a built-in character generator ROM. The MPU interface can be configured for both the 6800 family and 8080 family processors. Text, graphics, and overlayed text and graphics can be displayed. Table 2.2(6).1 is a command list summary.

Table 2.2(6).1

Command	Code (HEX)	Description
SYSTEM SET	40	System and display initialization
SLEEP IN	53	Enter standby mode
DISP ON/OFF	58,59	Display blinking and blanking
SCROLL	44	Set display starting address and display area
CSRFORM	5D	Set cursor type
CSRDIR	4C~4F	Set cursor movement direction
OVLAY	5B	Set overlay format
CGRAM ADR	5C	Set CGRAM start address
HDOT SCR	5A	Set horizontal scroll position
CSRW	46	Set cursor address
CSRR	47	Read cursor address
MWRITE	42	Write data to display memory
MREAD	43	Read data from memory

On the following pages you can find the initialization examples for the three display modules. Transferring the parameters to the display modules will set up a display system having:

single screen drive mode
Layer 1, character display
Layer 2, graphic display
Character font, 8 x 8 pixels
CGRAM, 32 characters max.

Table 2.2(6).2 Initialization example for G2446

Command	Code (HEX)	Function D7	D6	D5	D4	D3	D2	D1	D0	Description
SYSTEM SET	40	0	1	0	0	0	0	0	0	System and display initialization command
Parameter 1	30	PKT	0	IV	1	W/S	M2	M1	M0	M0: 0 Internal CGROM M1: 0 CGRAM 32 characters Max M2: 0 Character height = 8 pixels W/S: 0 Single screen display I/V: 1 Character offset disabled PKT: 0
Parameter 2	87	WF	0	0	0	0	← FX →			FX: 7 Character field width = 8 WF: 1 Two frame AC Drive
Parameter 3	07	0	0	0	0	← FY →				FY: 7 Character field height = 8
Parameter 4	1D	← C/R →								C/R: 29d Characters per row = 30
Parameter 5	94	← T C/R →								T C/R: 148d Timing characters per row = 149d fOSC = 6 MHz; Frame Freq. = 70 Hz
Parameter 6	3F	← L/F →								L/F: 63 Number of lines per screen = 64
Parameter 7	1E	← APL →								APL: 30d Address pitch = C/R + 1
Parameter 8	00	← APH →								APH: 00H
SCROLL	44	0	1	0	0	0	1	0	0	Set display starting address and display area
Parameter 1	00	← SAD1L →								Screen1 start address (low) = 00H
Parameter 2	00	← SAD1H →								Screen1 start address (high) = 00H
Parameter 3	3F	← SL1 →								SL1: 63d Number of lines in Screen 1 = 64d
Parameter 4	00	← SAD2L →								Screen2 start address (low) = 00H
Parameter 5	05	← SAD2H →								Screen2 start address (high) = 05H
Parameter 6	3F	← SL2 →								SL2: 63d Number of lines in Screen 2 = 64d
CSRDIR	4C	0	1	0	0	1	1	CD1	CD2	Set cursor movement direction CD1, CD2: 0 0 Shift direction = Right
HDOT SCR	5A	0	1	0	1	1	0	1	0	Set horizontal scroll position
Parameter 1	00	0	0	0	0	0	← CD1 →			CD1: 0d Don't scroll display horizontally
CSRW	46	0	1	0	0	0	1	1	0	Set cursor address
Parameter 1	00	← CSRL →								Cursor address (low) = 00
Parameter 2	00	← CSRH →								Cursor address (high) = 00
MWRITE	42	0	1	0	0	0	0	1	0	Write data to display memory
Parameter 1 ~ n	--	← Character codes →								Write n characters to the display memory
OVLAY	5B	0	1	0	1	1	0	1	1	Set overlay format
Parameter 1	01	0	0	0	OV	DM2	DM1	MX1	MX0	MX1, MX0: 01 L1 exOR L2 DM2, DM1: 00 1st and 3rd screens in character mode OV: 0 Two layer synthesis
DISP ON/OFF	59	0	1	0	1	1	0	0	D	Display blinking and blanking D: 1 Entire display active
Parameter 1	04	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0	FC1, FC0: 00 Cursor display OFF FP1, FP0: 01 1st screen ON FP3, FP2: 00 2nd screen OFF FP5, FP4: 00 3rd screen OFF

Note: d: decimal notation, H: hex notation

Table 2.2(6).3 Initialization example for G242C

Command	Code (HEX)	Function								Description
		D7	D6	D5	D4	D3	D2	D1	D0	
SYSTEM SET	40	0	1	0	0	0	0	0	0	System and display initialization command
Parameter 1	30	PKT	0	IV	1	W/S	M2	M1	M0	M0: 0 Internal CGROM M1: 0 CGRAM 32 characters Max M2: 0 Character height = 8 pixels W/S: 0 Single screen display I/V: 1 Character offset disabled PKT: 0
Parameter 2	87	WF	0	0	0	0	← FX →			FX: 7 Character field width = 8 WF: 1 Two frame AC Drive
Parameter 3	07	0	0	0	0	← FY →				FY: 7 Character field height = 8
Parameter 4	1D	← C/R →								C/R: 29d Characters per row = 30
Parameter 5	4A	← T C/R →								T C/R: 74d Timing characters per row = 75d fOSC = 6 MHz; Frame Freq. = 70 Hz
Parameter 6	7F	← L/F →								L/F: 127 Number of lines per screen = 128
Parameter 7	1E	← APL →								APL: 30d Address pitch = C/R + 1
Parameter 8	00	← APH →								APH: 00H
SCROLL	44	0	1	0	0	0	1	0	0	Set display starting address and display area
Parameter 1	00	← SAD1L →								Screen1 start address (low) = 00H
Parameter 2	00	← SAD1H →								Screen1 start address (high) = 00H
Parameter 3	7F	← SL1 →								SL1: 127d Number of lines in Screen 1 = 128d
Parameter 4	00	← SAD2L →								Screen2 start address (low) = 00H
Parameter 5	05	← SAD2H →								Screen2 start address (high) = 05H
Parameter 6	7F	← SL2 →								SL2: 127d Number of lines in Screen 2 = 128d
CSRDIR	4C	0	1	0	0	1	1	CD1	CD2	Set cursor movement direction CD1, CD2: 0 0 Shift direction = Right
HDOT SCR	5A	0	1	0	1	1	0	1	0	Set horizontal scroll position
Parameter 1	00	0	0	0	0	0	← CD1 →			CD1: 0d Don't scroll display horizontally
CSRW	46	0	1	0	0	0	1	1	0	Set cursor address
Parameter 1	00	← CSRL →								Cursor address (low) = 00
Parameter 2	00	← CSRH →								Cursor address (high) = 00
MWRITE	42	0	1	0	0	0	0	1	0	Write data to display memory
Parameter 1 ~ n	--	← Character codes →								Write n characters to the display memory
OVLAY	5B	0	1	0	1	1	0	1	1	Set overlay format
Parameter 1	01	0	0	0	OV	DM2	DM1	MX1	MX0	MX1, MX0: 01 L1 exOR L2 DM2, DM1: 00 1st and 3rd screens in character mode OV: 0 Two layer synthesis
DISP ON/OFF	59	0	1	0	1	1	0	0	D	Display blinking and blanking D: 1 Entire display active
Parameter 1	04	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0	FC1, FC0: 00 Cursor display OFF FP1, FP0: 01 1st screen ON FP3, FP2: 00 2nd screen OFF FP5, FP4: 00 3rd screen OFF

Note: d: decimal notation, H: hex notation

Table 2.2(6).4 Initialization example for G321D

Command	Code (HEX)	Function								Description
		D7	D6	D5	D4	D3	D2	D1	D0	
SYSTEM SET	40	0	1	0	0	0	0	0	0	System and display initialization command
Parameter 1	30	PKT	0	IV	1	W/S	M2	M1	M0	M0: 0 Internal CGROM M1: 0 CGRAM 32 characters Max M2: 0 Character height = 8 pixels W/S: 0 Single screen display I/V: 1 Character offset disabled PKT: 0
Parameter 2	87	WF	0	0	0	0	← FX →			FX: 7 Character field width = 8 WF: 1 Two frame AC Drive
Parameter 3	07	0	0	0	0	← FY →				FY: 7 Character field height = 8
Parameter 4	27	← C/R →								C/R: 39d Characters per row = 40
Parameter 5	2F	← T C/R →								T C/R: 47d Timing characters per row = 48d fOSC = 6 MHz; Frame Freq. = 70 Hz
Parameter 6	C7	← L/F →								L/F: 199d Number of lines per screen = 200
Parameter 7	28	← APL →								APL: 40d Address pitch = C/R + 1
Parameter 8	00	← APH →								APH: 00H
SCROLL	44	0	1	0	0	0	1	0	0	Set display starting address and display area
Parameter 1	00	← SAD1L →								Screen1 start address (low) = 00H
Parameter 2	00	← SAD1H →								Screen1 start address (high) = 00H
Parameter 3	C7	← SL1 →								SL1: 199d Number of lines in Screen 1 = 200d
Parameter 4	00	← SAD2L →								Screen2 start address (low) = 00H
Parameter 5	05	← SAD2H →								Screen2 start address (high) = 05H
Parameter 6	C7	← SL2 →								SL2: 199d Number of lines in Screen 2 = 200d
CSRDIR	4C	0	1	0	0	1	1	CD1	CD2	Set cursor movement direction CD1, CD2: 0 0 Shift direction = Right
HDOT SCR	5A	0	1	0	1	1	0	1	0	Set horizontal scroll position
Parameter 1	00	0	0	0	0	0	← CD1 →			CD1: 0d Don't scroll display horizontally
CSRW	46	0	1	0	0	0	1	1	0	Set cursor address
Parameter 1	00	← CSRL →								Cursor address (low) = 00
Parameter 2	00	← CSRH →								Cursor address (high) = 00
MWRITE	42	0	1	0	0	0	0	1	0	Write data to display memory
Parameter 1 ~ n	--	← Character codes →								Write n characters to the display memory
OVLAY	5B	0	1	0	1	1	0	1	1	Set overlay format
Parameter 1	01	0	0	0	OV	DM2	DM1	MX1	MX0	MX1, MX0: 01 L1 exOR L2 DM2, DM1: 00 1st and 3rd screens in character mode OV: 0 Two layer synthesis
DISP ON/OFF	59	0	1	0	1	1	0	0	D	Display blinking and blanking D: 1 Entire display active
Parameter 1	04	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0	FC1, FC0: 00 Cursor display OFF FP1, FP0: 01 1st screen ON FP3, FP2: 00 2nd screen OFF FP5, FP4: 00 3rd screen OFF

Note: d: decimal notation, H: hex notation

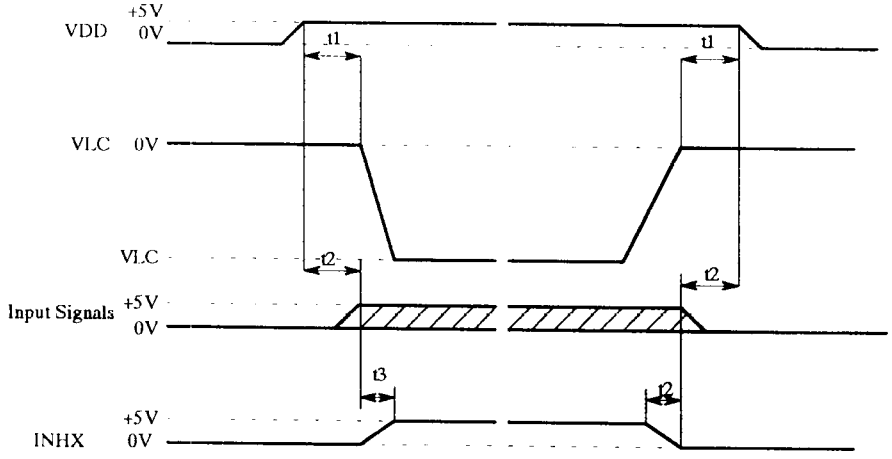
2.3 Timing characteristics

2.3.1 Power ON/OFF and signal input timing

Power ON/OFF and signal input timing should be performed according to the timing charts shown below.

Figure 2.3.1.1 shows the timing for the G321D without controller.

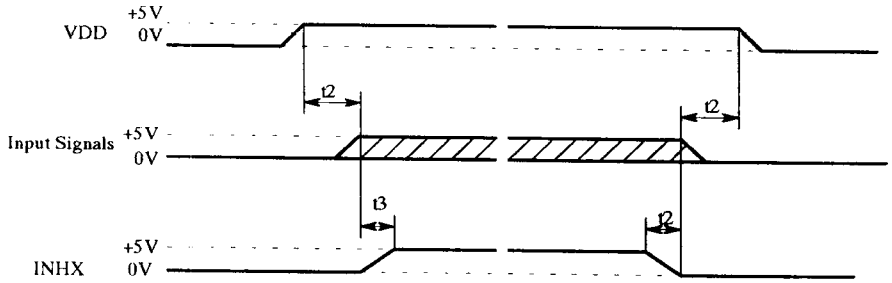
Figure 2.3.1.1



±t1 ≥ 0 ms
t2 ≥ 0 ms
t3 ≥ 20 ms

Figure 2.3.1.2 shows the timing for the G242C and the G2446 without controller.

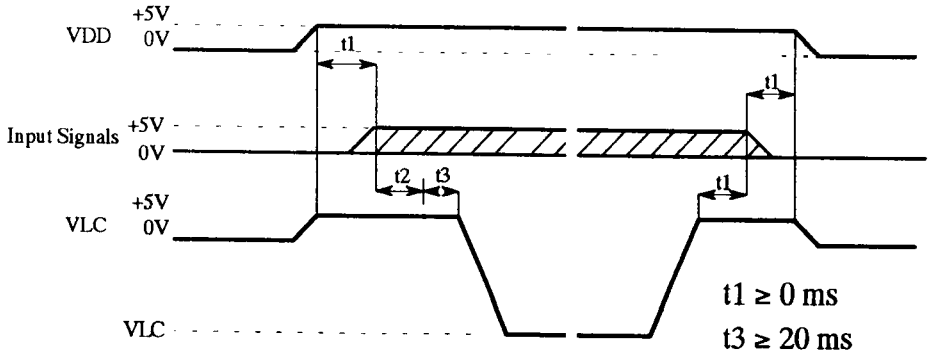
Figure 2.3.1.2



t2 ≥ 0 ms
t3 ≥ 20 ms

Figure 2.3.1.3 shows the timing for the G321D with controller.

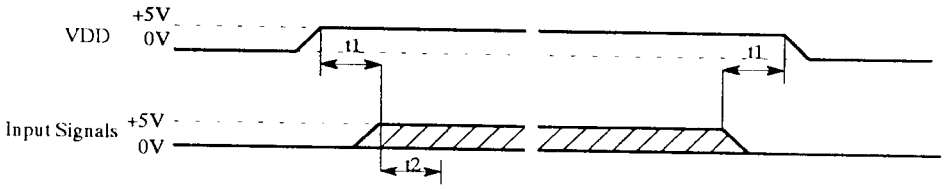
Figure 2.3.1.3



t1 ≥ 0 ms
t3 ≥ 20 ms
t2: controller initialization time

Figure 2.3.1.4 shows the timing for the G242C and the G2446 with controller.

Figure 2.3.1.4



t1 ≥ 0 ms
t2: controller initialization time

NOTE: The controller must be initialized immediately after the power supply goes to 5V

2.3.2 Timing characteristics (without controller)

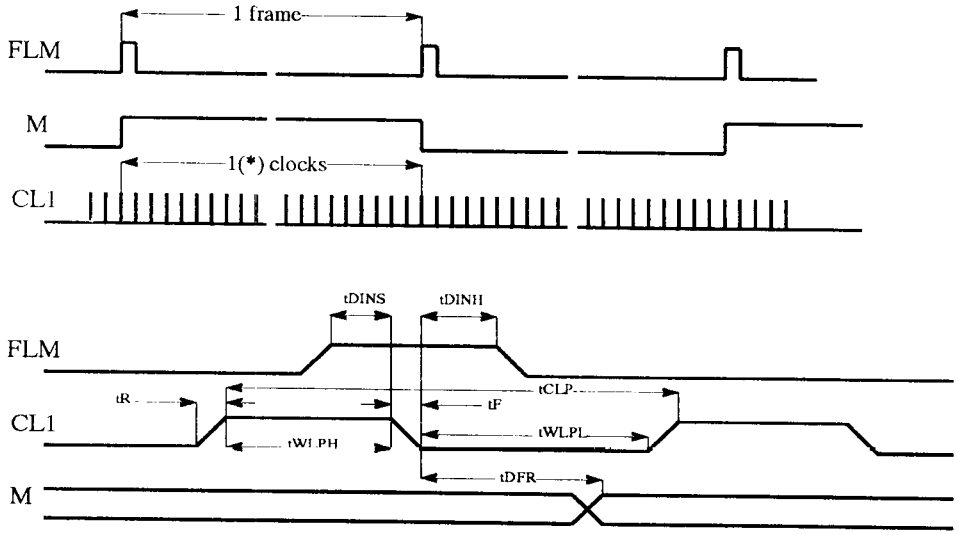
Table 2.3.2 Timing characteristics

Ta = 0°C to 50 °C, VDD = 5V ± 5%, VSS = 0V

Item	Symbol	Min.	Max.	Unit
CL1 period	t_{CLP}	1000	-	ns
CL1 "H" pulse width	t_{WLPH}	125	-	ns
CL1 "L" pulse width	t_{WLPL}	-	-	ns
FLM setup time	t_{DINS}	100		ns
FLM hold time	t_{DINH}	100		ns
Allowable M delay time	t_{DFR}	-	300	ns
Input signal rise time	t_{R}	-	50	ns
Input signal fall time	t_{F}	-	50	ns
CL2 period	t_{CXSCL}	334	-	ns
CL2 "H" pulse width	t_{WXSCLH}	125	-	ns
CL2 "L" pulse width	t_{WXSCLL}	125	-	ns
Data setup time	t_{DS}	100	-	ns
Data hold time	t_{DH}	100	-	ns
CL2 rise to CL1 rise time	t_{LD}	63	-	ns
CL2 fall to CL1 fall time	t_{SL}	125	-	ns
CL1 rise to CL2 rise time	t_{LS}	125	-	ns
CL1 fall to CL2 fall time	t_{LH}	63	-	ns

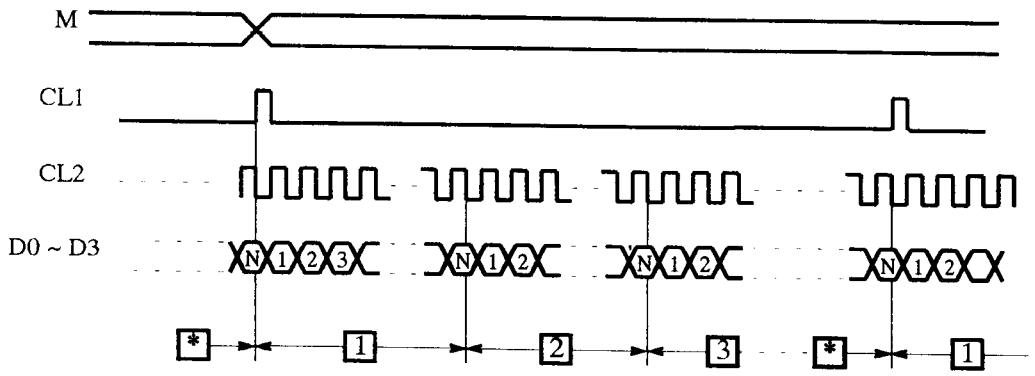
Timing charts

Timing chart 1: Timing of signal input into common driver



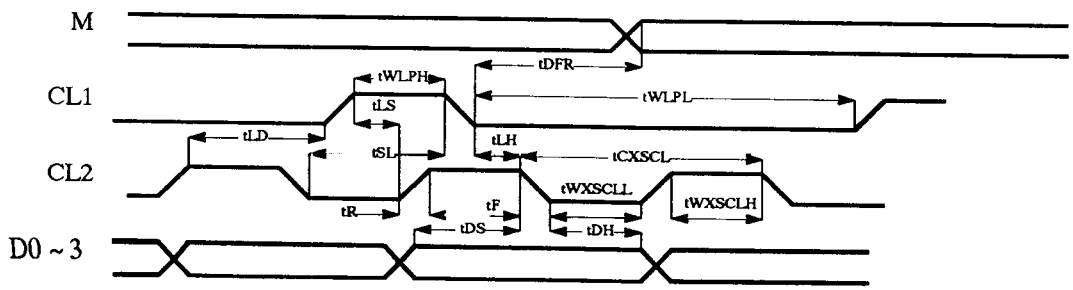
1(*) - G2446:64 clocks
- G242C:128 clocks
- G321D:200 clocks

Timing chart 2: Timing of signal input into segment driver



* G2446, G242C N = 20 [1] [3] Cascade number of the segment driver

G321D N = 20 [1] [4] Cascade number of the segment driver



2.3.3 Timing characteristics (with controller)

Table 2.3.3 Timing characteristics

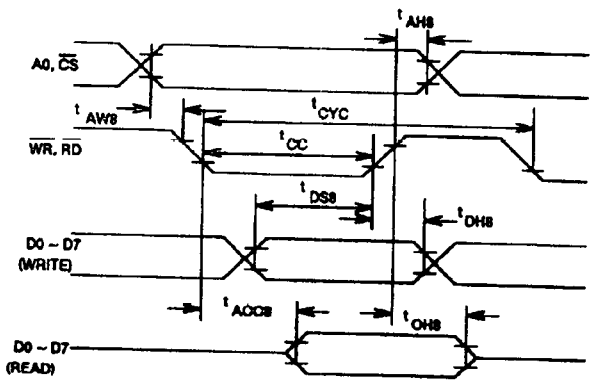
Signal		Symbol	Item	Min.	Max.	Unit
80 series timing	WR,RD	t_{CYC}	System cycle time	(1)	-	ns
		t_{CC}	Control pulse width	220	-	ns
68 series timing	A0,CS,R/W,E	t_{CYC}	System cycle time	(2)	-	ns
		t_{EW}	Enable pulse width	220	-	ns
80 and 68 series timing	A0,CS	t_{AH}	Address hold time	10	-	ns
		t_{AW}	Address setup time	30	-	ns
	D0~D7	t_{DS}	Data setup time	120	-	ns
		t_{DH}	Data hold time	10	-	ns
		t_{ACC}	RD access time	-	120	ns
		t_{OH}	Output disable time	10	50	ns

(1) For memory control and cursor movement control:
$t_{CYC} = 2_{tC} + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$
For all other commands:
$t_{CYC} = 4t_C + t_{CC} + 30$

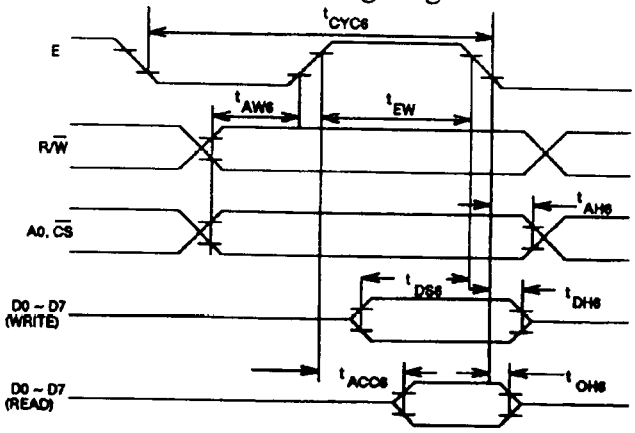
(2) For memory control and cursor movement control:
$t_{CYC} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$
For all other commands:
$t_{CYC} = 4t_C + t_{EW} + 30$

Figure 2.3.3

80 series timing diagram



68 series timing diagram



3. FL BACKLIGHTING

The G2446,G242C and G321D have a built in side edge type of FL (cold cathode fluorescent lamp) backlight.

FL inverter is not built in. Plaese use recommended FL inverter.

3.1 Absolute maximum ratings

3.1.1 G2446 , G242C

Item	Symbol	Rating	Unit
Circuit voltage	Vs	1300 max	Vrms
Lamp current	I_{FL}	10 max	mArm
Frequency	f_{FL}	50 max	kHz

3.1.2 G321D

Item	Symbol	Rating	Unit
Circuit voltage	Vs	1500 max	Vrms
Lamp current	I_{FL}	10 max	mArm
Frequency	f_{FL}	50 max	kHz

3.2 Electrical characteristics

3.2.1 G2446 , G242C

FL inverter V_{FL}=220 Vrms , f_{FL}=35 kHZ

Item	Symbol	Condition	Min	Typ	Max	Unit
Lamp voltage	V_{FL}	Ta=25°C	190	220	250	Vrms
Discharge start volatage	Vs	Ta=0°C	850	-	-	Vrms
Lamp current	I_{FL}	Ta=25°C	4.5	5	5.5	mArm

3.2.2 G321D

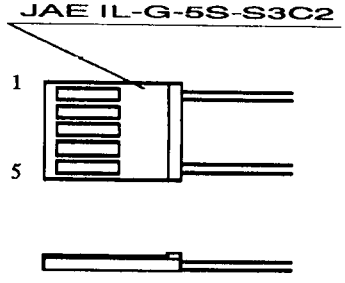
FL inverter V_{FL}=260 Vrms , f_{FL}=30 kHZ

Item	Symbol	Condition	Min	Typ	Max	Unit
Lamp voltage	V_{FL}	Ta=25°C	230	260	290	Vrms
Discharge start volatage	Vs	Ta=0°C	1000	-	-	Vrms
Lamp current	I_{FL}	Ta=25°C	4.0	4.5	5.0	mArm

3.3 Connector for FL backlight

Connector for FL backlight : IL-G-5S-S3C2 (JAE)

No.	Signal	Function
1	AC out	Ground : 0V
2	NC	NC
3	NC	NC
4	NC	NC
5	AC out	FL backlight driving voltage



3.4 Brightness

Item	Symbol	Condition	Min	Typ	Max	Unit
Brightness* (At the center of the LCD surface)	Bp	25°C 30~85%RH	60	70	80	nit

* FL inverter

Item	G2446	G242C	G321D
Inverter type	ILP-325-INV (ENPLAS)	ILP-324-INV (ENPLAS)	ILP-323-INV (ENPLAS)
FL driving conditions	V_{FL}=220V_{rms},f_{FL}=35KHz	V_{FL}=220V_{rms},f_{FL}=35KHz	V_{FL}=260V_{rms},f_{FL}=30KHz
LCD driving conditions	V_{opr}=12.8V,FLM=70KHz	V_{opr}=17.0V,FLM=70KHz	V_{opr}=22.0V,FLM=70KHz
LCD display pattern	All ON display (all data "H")	All ON display (all data "H")	All ON display (all data "H")
Measurement equipment	LS100 (MINOLTA)	LS100 (MINOLTA)	LS100 (MINOLTA)

3.5 Service Life

Item	Condition	Rating	Unit
Scrvice life*	Ta=25°C±3°C	10,000min	hrs

* Time until the intensity decrease to half of the initial brightness, or time until "no lit" because of increase in FL discharge start voltage.
FL driving condition
-G2446 : I_{FL}=5.0 mArms
-G242C : I_{FL}=5.0 mAmrs
-G321D : I_{FL}=4.5 mAmrs

3.6 Recommended FL inverter

3.6.1 G2446

(1) Model name
ILP-325-INV
(2) Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Input voltage	Vin	Ta=25°C	6 Vmax	Vdc
Input current	Iin		450 max	mA
Operating temperature	Ta		0~+50	°C
Storage temperature	Ts		-30~+70	°C

(3) Electrical characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Input voltage	Vin	Ta=25°C	4.5	5.0	5.5	Vdc
Circuit voltage	Vo	Vin=5.0V Ta=25°C	850	-	1200	Vrms
Output current	Io		4.5	5.0	5.5	mArm
Oscillation frequency	FL		25	35	45	KHz

3.5.2 G242C

(1) Model name

ILP-324-INV

(2) Absolute maximum ratings

Item	Symbol	Condition	Rating	Unit
Input voltage	Vin	Ta=25°C	6 Vmax	Vdc
Input current	Iin		700 max	mA
Operating temperature	Ta		0-50	°C
Storage temperature	Ts		-30-70	°C

(3) Electrical characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Input voltage	Vin	Ta=25°C	4.5	5.0	5.5	Vdc
Circuit voltage	Vo	Vin=5.0V Ta=25°C	850	-	1300	Vrms
Output current	Io		4.5	5.0	5.5	mArm
Oscillation frequency	FL		25	35	45	KHz

3.5.3 G321D

(1) Model name

ILP-323-INV

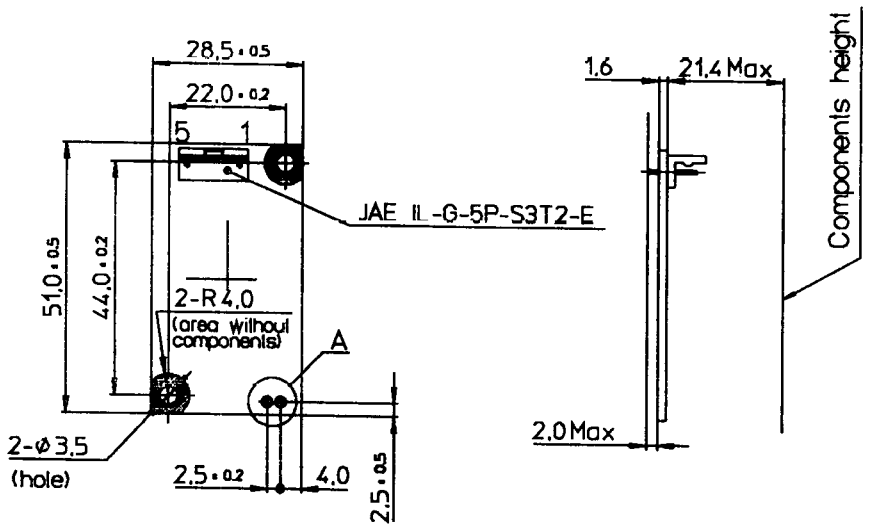
(2) Absolute maximum ratings

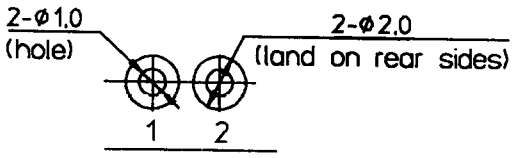
Item	Symbol	Condition	Rating	Unit
Input voltage	Vin	Ta=25°C	6 Vmax	Vdc
Input current	Iin		700 max	mA
Operating temperature	Ta		0-50	°C
Storage temperature	Ts		-30-70	°C

(3) Electrical characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Input voltage	Vin	Ta=25°C	4.5	5.0	5.5	Vdc
Circuit voltage	Vo	Vin=5.0V Ta=25°C	1000	-	1500	Vrms
Output current	Io		4.0	4.5	5.0	mArm
Oscillation frequency	FL		20	30	40	KHz

3.7 Dimensions





A detail (5:1)

CN1

PIN No	SIGNAL
1	Vcc
2	GND

CN2

PIN No	SIGNAL
1	AC out
2	NC
3	NC
4	NC
5	AC out

Material UL approved 94V-0

4. NOTES

Safety

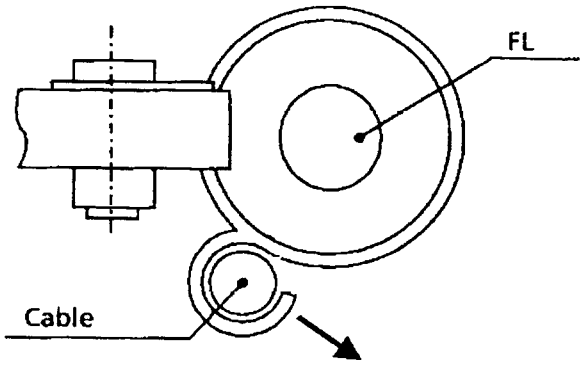
- If the LCD panel brakes, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is made of plate glass; do not hit or press against it.
- Do not remove the panel or frame from the module.
- The polarizer on the display is fragile; handle it very carefully.

Mounting and Design

- Mount the module in the specified installation section and holes.
- To protect the module from external pressure, put a plate of transparent material such as acrylic or glass over the display surface, frame , and polarizer. Leave a small gap between the transparent plate and the module.
- When the LCD panel is put antiglare type of polarizer, the module can be not necessary to put a protection plate because it is put also hard coating layer what has some resistance of scratch.
- Keep the module dry. Condensation can damage the transparent electrodes.
- The inverter output is very high voltage. To prevent electric shock, do not touch the wiring while the power is on.
- Do not pull the cable of the FL backlight in the direction shown below. The cable may be displaced if pulled in that direction.



Storage

- Store the module in a dark place where the temperature is 25C+10C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module or its components.

Cleaning

- Do not wipe the polarizer with a dry cloth, as it may scratch the surface.
- Wipe the module gently with a soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents(ketone and acetone) or aromatic solvents(toluene and xylene), as they may damage the polarizer.
- Use flon or isopropyl alcohol to clean antiglear type of polarizer.