

PHP225

Dual P-channel intermediate level FET

Rev. 03 — 4 January 2011

Product data sheet

1. Product profile

1.1 General description

Dual intermediate level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using vertical D-MOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- Motor and actuator drivers
- Synchronized rectification
- Power management

1.4 Quick reference data

Table 1. Quick reference data

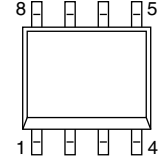
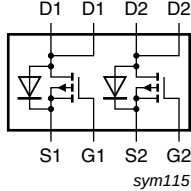
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-	-30	V
I_D	drain current	$T_{sp} \leq 80\text{ °C}$	-	-	-2.3	A
P_{tot}	total power dissipation	$T_{sp} = 80\text{ °C}$	[1]	-	2	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$; $I_D = -1\text{ A}$; $T_j = 25\text{ °C}$	-	0.22	0.25	Ω
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = -10\text{ V}$; $I_D = -2.3\text{ A}$; $V_{DS} = -15\text{ V}$; $T_j = 25\text{ °C}$	-	3	-	nC

[1] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 SOT96-1 (SO8)	 sym115
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHP225	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	-30	V
V_{GS}	gate-source voltage		-	-	V
V_{GSO}	gate-source voltage	open drain	-20	20	V
I_D	drain current	$T_{sp} \leq 80\text{ °C}$	-	-2.3	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; pulsed	[1]	-10	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	1	W
		$T_{sp} = 80\text{ °C}$	[3]	2	W
		$T_{amb} = 25\text{ °C}$	[4]	1.3	W
			[5]	2	W
T_{stg}	storage temperature		-65	150	°C
T_j	junction temperature		-	150	°C
Source-drain diode					
I_S	source current	$T_{sp} \leq 80\text{ °C}$	-	-1.25	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; pulsed	[1]	-5	A

- [1] Pulse width and duty cycle limited by maximum junction temperature.
- [2] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 90 K/W.
- [3] Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 2 W at the same time.
- [4] Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 90 K/W.
- [5] Maximum permissible dissipation per MOS transistor. Device mounted on printed-circuit board with a thermal resistance from ambient to tie-point of 27.5 K/W.

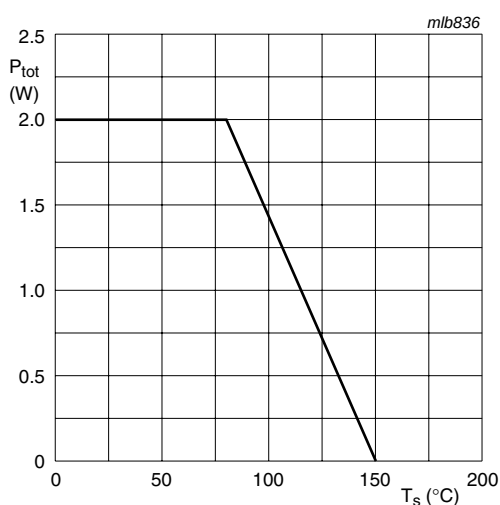


Fig 1. Power derating curve

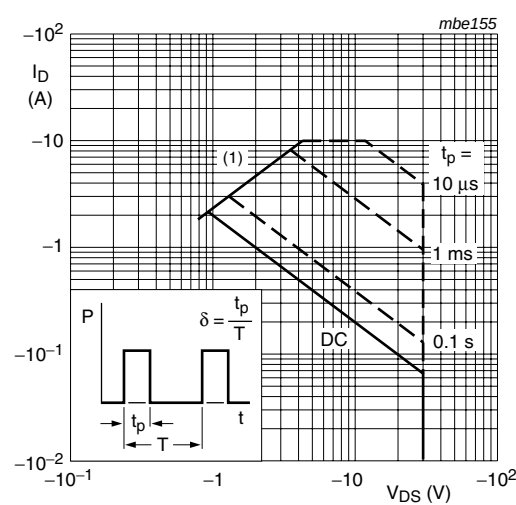


Fig 2. SOAR; P-channel

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	35	K/W

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -10 μA; V _{GS} = 0 V; T _j = 25 °C	-30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = -1 mA; V _{DS} = V _{GS} ; T _j = 25 °C	-1	-	-2.8	V
I _{DSS}	drain leakage current	V _{DS} = -24 V; V _{GS} = 0 V; T _j = 25 °C	-	-	-100	nA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -1 A; T _j = 25 °C	-	0.22	0.25	Ω
		V _{GS} = -4.5 V; I _D = -0.5 A; T _j = 25 °C	-	0.33	0.4	Ω
I _{DSon}	on-state drain current	V _{DS} = -1 V; V _{GS} = -10 V	-2.3	-	-	A
		V _{DS} = -5 V; V _{GS} = -4.5 V	-1	-	-	A
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = -2.3 A; V _{DS} = -15 V; V _{GS} = -10 V; T _j = 25 °C	-	10	25	nC
Q _{GS}	gate-source charge		-	1	-	nC
Q _{GD}	gate-drain charge		-	3	-	nC
C _{iss}	input capacitance	V _{DS} = -20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C	-	250	-	pF
C _{oss}	output capacitance		-	140	-	pF
C _{rss}	reverse transfer capacitance		-	50	-	pF
g _{fs}	transfer conductance	V _{DS} = -20 V; I _D = -1 A; T _j = 25 °C	1	2	-	S
t _{off}	turn-off time	V _{DS} = -20 V; V _{GS} = -10 V; R _{G(ext)} = 4.7 Ω; R _L = 20 Ω; T _j = 25 °C; I _D = -1 A	-	50	140	ns
t _{on}	turn-on time		-	20	80	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = -1.25 A; V _{GS} = 0 V; T _j = 25 °C	-	-	-1.6	V
t _{rr}	reverse recovery time	I _S = -1.25 A; dI _S /dt = 100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _j = 25 °C	-	150	200	ns

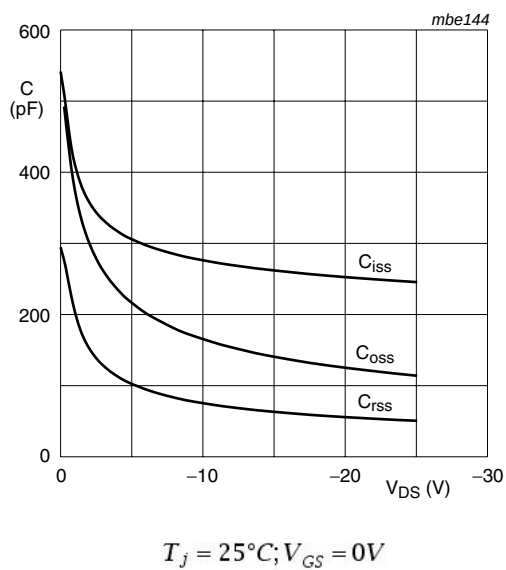


Fig 3. Capacitance as a function of drain-source voltage; P-channel; typical values

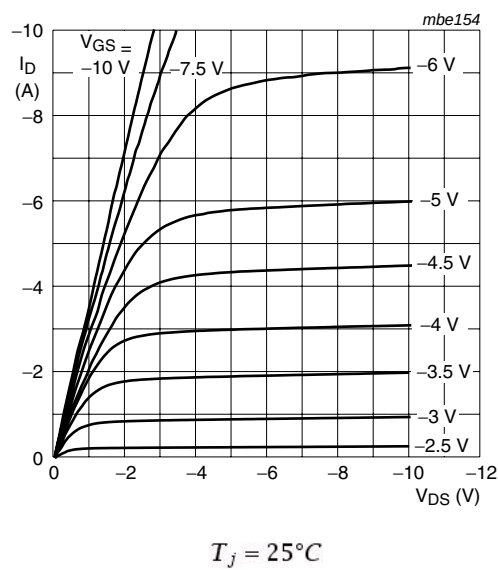


Fig 4. Output characteristics: drain current as a function of drain-source voltage; P-channel; typical values

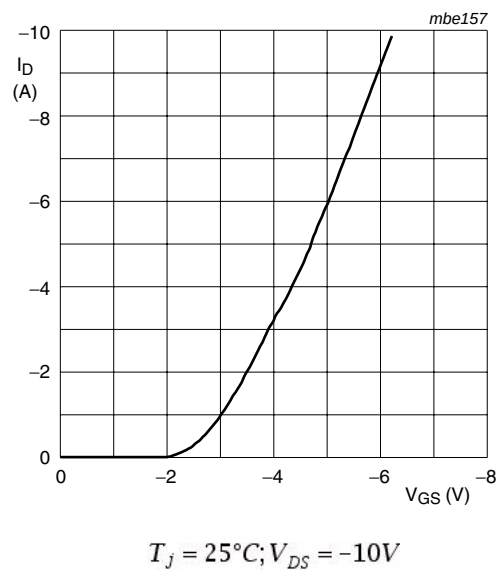


Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; P-channel; typical values

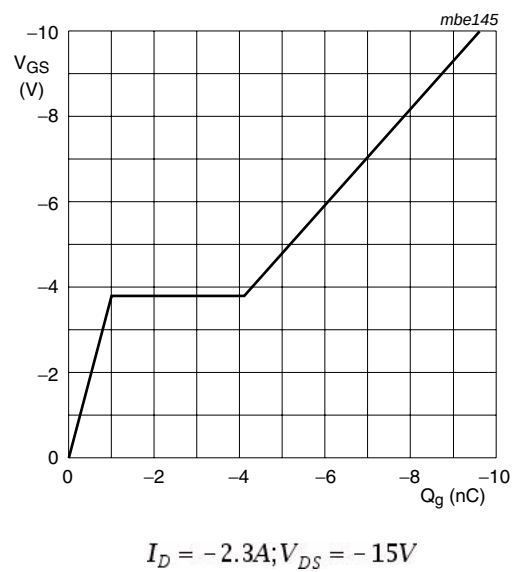


Fig 6. Gate-source voltage as a function of gate charge; P-channel; typical values

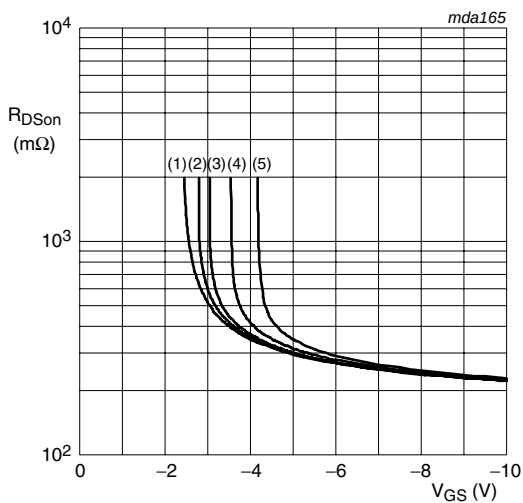


Fig 7. Drain-source on-state resistance as a function of drain current; P-channel; typical values

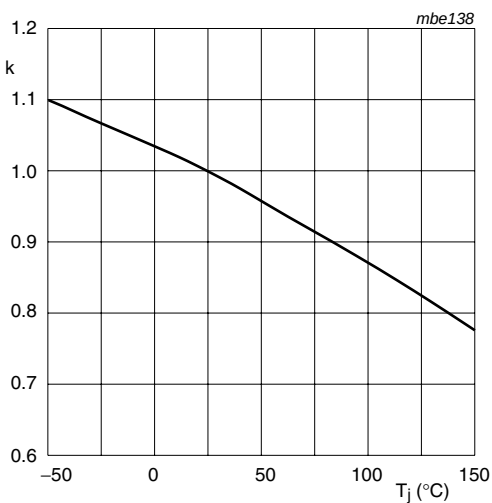


Fig 8. Temperature coefficient of gate-source threshold voltage

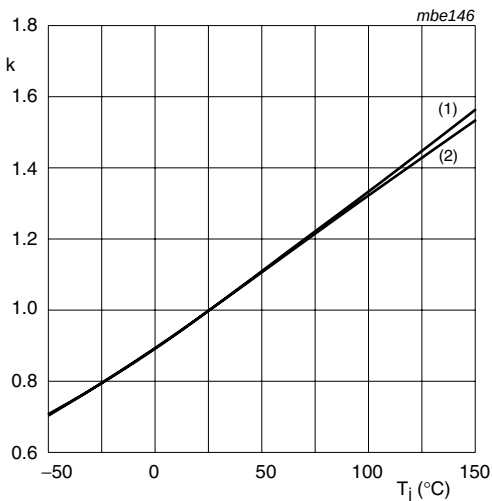
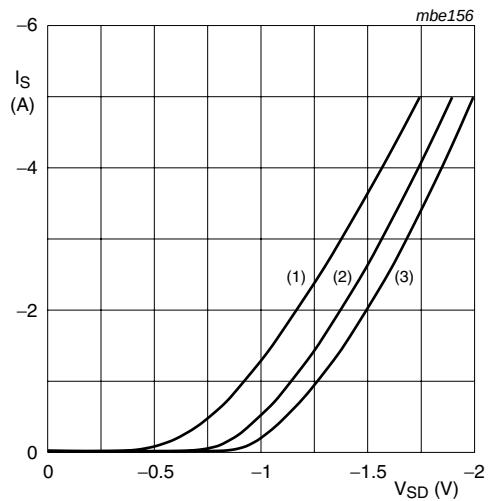


Fig 9. Temperature coefficient of drain-source on-state resistance; P-channel



$V_{GD} = 0V$ (1) $T_j = 150^{\circ}C$ (2) $T_j = 25^{\circ}C$ (3) $T_j = -55^{\circ}C$

Fig 10. Source current as a function of source-drain voltage

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

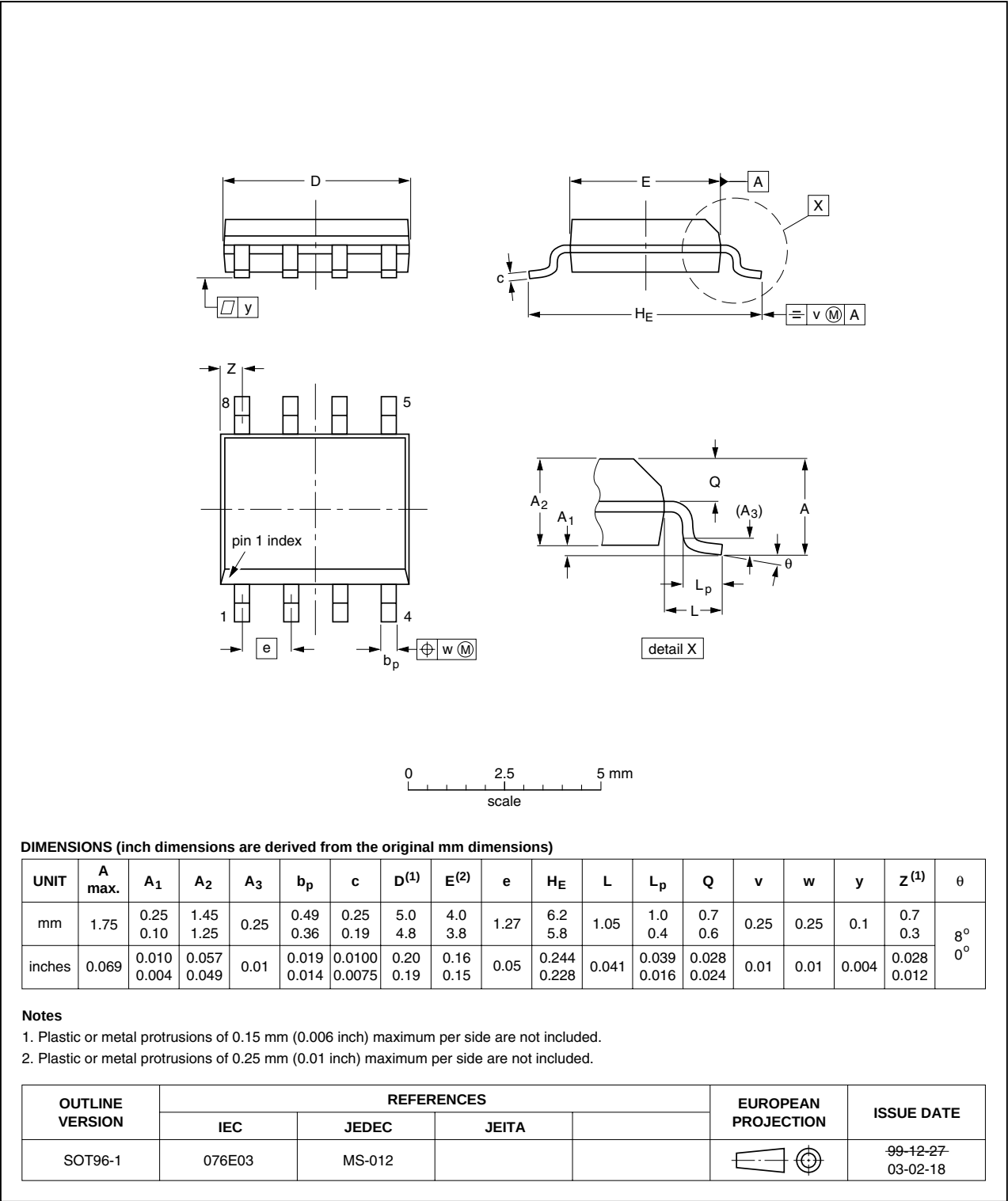


Fig 11. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHP225 v.3	20110104	Product data sheet	-	PHP225 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PHP225 v.2	19970620	Product specification	-	PHP225 v.1

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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