National Semiconductor

December 1994

LP265/LP365 Micropower Programmable Quad Comparator

General Description

The LP365 consists of four independent voltage comparators. The comparators can be programmed, four at the same time, for various supply currents, input currents, response times and output current drives. This is accomplished by connecting a single resistor between the V_{CC} and I_{SET} pins.

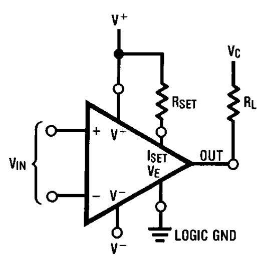
These comparators can be operated from split power supplies or from a single power supply over a wide range of voltages. The input can sense signals at ground level even with single supply operation. The unique output NPN transistor stages are uncommitted to either power supply. They can be connected directly to various logic system supplies so that they are highly flexible to interface with various logic families.

Application areas include battery power circuits, threshold detectors, zero crossing detectors, simple serial A/D converters, VCO, multivibrators, voltage converters, power sequencers, and high performance V/F converters, and RTD linearization.

Features

- Single programming resistor to tailor power consumption, input current, speed and output current drive capability
- Wide single supply voltage range or dual supplies (4 V_{DC} to 36 V_{DC} or ± 2.0 V_{DC} to ± 18 V_{DC})
- Low supply current drain (10 μA) and low power consumption (10 μW/comparator) @ $I_{SET} = 0.5$ μA $V_{CC} = 5_{VDC}$
- Uncommitted output stage—selectable output levels
- Output directly compatible with DTL, TTL, CMOS, MOS or other special logic families
- Input common-mode range includes ground
- Differential input voltage equal to the power supply voltage

Typical Connection



TL/H/5023–1

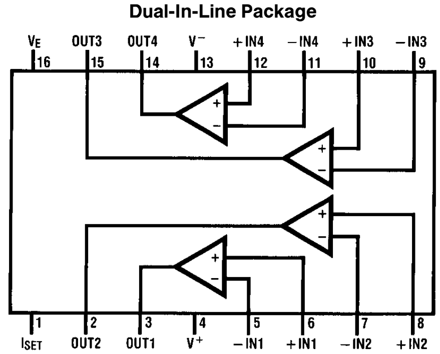
Programming Equation

$$I_{SET} = \frac{(V^+) - (V^-) - 1.3V}{R_{SET}}$$

$$I_{SUPPLY} \approx 22 \times I_{SET}$$

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/H/5023–2

Order Number LP365M, LP365AN or LP365N
See NS Package Numbers M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ± 18 V_{DC}
Differential Input Voltage	± 36 V_{DC}
Input Voltage (Note 1)	−0.3V to +36 V_{DC}
Output Short Circuit to V_E (Note 2)	Continuous
V_{OUT} with Respect to V_E	$V_E - 7V \leq V_{OUT} \leq V_E + 36V$
ESD Tolerance (Note 10)	2000V

	M Package	N Package
Power Dissipation (Note 3)	500 mW	500 mW
T_j Max	115°C	115°C
θ_{jA}	115°C/W	90°C/W
Lead Temp.		
(Soldering—10 sec.)		260°C
(Vapor Phase—60 sec.)	215°C	
(Infrared—15 sec.)	220°C	
Operating Temp. Range LP365:	$0°C \leq T_A \leq +70°C$	
Storage Temp. Range	$-40°C \leq T_A \leq +150°C$	

Electrical Characteristics (Note 4) Low power $V_S = 5V$, $I_{SET} = 10\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$	2	20	**50**	4	25	**75**	nA (Max)
		LP265				4	25	**150**	
I_B	Input Bias Current	$V_{CM} = 0V$	10	50	**125**	15	75	**200**	nA (Max)
		LP265				15	75	**300**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 100k$	500	50	**50**	300	25	**25**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			0	**0**		0	**0**	V (Max)
				3	**3**		3	**3**	V (Min)
CMRR	Common-Mode Rejection Ratio	$0 \leq V_{CM} \leq 3V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 2.5V \leq V_S \leq \pm 3.5V$	75	65	**65**	70	65	**65**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$	215	250	**300**	225	275	**300**	μA (Max)
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	2.4	1.2	**0.6**	2.0	0.8	**0.4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 5V$, $V_E = 0V$	2	50	**5000**	2	100	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10\ pF$ (Note 7)	4			4			μs

Electrical Characteristics (Continued) (Note 8) High power $V_S = \pm 15V$, $I_{SET} = 100\ \mu A$

Symbol	Parameter	Conditions	LP365A			LP365			Units (Limit)
			Typ	Tested Limit (Note 5)	Design Limit (Note 6)	Typ	Tested Limit (Note 5)	Design Limit (Note 6)	
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$, $R_S = 100$	1	3	**6**	3	6	**9**	mV (Max)
I_{OS}	Input Offset Current	$V_{CM} = 0V$	5	50	**100**	10	90	**200**	nA (Max)
		LP265				10	90	**500**	
I_B	Input Bias Current	$V_{CM} = 0V$	60	200	**500**	80	300	**500**	nA (Max)
		LP265				80	300	**800**	
A_{VOL}	Large Signal Voltage Gain	$R_L = 15k$	500	100	**100**	500	100	**100**	V/mV (Min)
V_{CM}	Input Common-Mode Voltage Range			−15	**−15**		−15	**−15**	V (Max)
				13	**13**		13	**13**	V (Min)
CMRR	Common-Mode Rejection Ratio	$-15V \leq V_{CM} \leq 13V$	85	75	**70**	80	75	**70**	dB (Min)
PSRR	Supply Voltage Rejection Ratio	$\pm 10V \leq V_S \leq \pm 15V$	80	70	**70**	75	70	**70**	dB (Min)
I_S	Supply Current	All Inputs = 0V, $R_L = \infty$	2.6	3	**3.3**	2.8	3.5	**3.7**	mA (Max)
		LP265				2.8	3.5	**4.3**	
V_{OH}	Output Voltage High	$V_C = 5V$, $V_E = 0V$, $R_L = 100k$		4.9	**4.5**		4.9	**4.5**	V (Min)
V_{OL}	Output Voltage Low	$V_E = 0V$		0.4	**0.4**		0.4	**0.4**	V (Max)
I_{SINK}	Output Sink Current	$V_E = 0V$, $V_O = 0.4V$	10	8	**5.5**	7.5	6	**4**	mA (Min)
I_{LEAK}	Output Leakage Current	$V_C = 15V$, $V_E = -15V$	5	50	**5000**	5	50	**5000**	nA (Max)
t_R	Response Time	$V_{CC} = 5V$, $V_E = 0V$, $R_L = 5k$, $C_L = 10$ pF (Note 7)	1.0			1.0			μs

Note 1: The input voltage is not allowed to go 0.3V above V^+ or −0.3V below V^- as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 2: Short circuits from the output to V^+ may cause excessive heating and eventual destruction. The current in the output leads and the V_E lead should not be allowed to exceed 30 mA. The output should not be shorted to V^- if $V_E \leq (V^-) + 7V$.

Note 3: For operating at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{jA} and T_j max. $T_j = T_A + \theta_{jA} P_D$.

Note 4: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = 5V$, $V^- = 0V$, $I_{SET} = 10\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 5: Guaranteed and 100% production tested.

Note 6: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate out-going quality levels.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive.

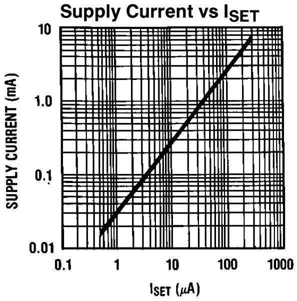
Note 8: Boldface numbers apply at temperature extremes. All other numbers apply at $T_A = T_j = 25°C$. $V^+ = +15V$, $V^- = -15V$, $I_{SET} = 100\ \mu A$, $R_L = 100k$, and $V_C = 5V$ as shown in the Typical Connection diagram.

Note 9: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

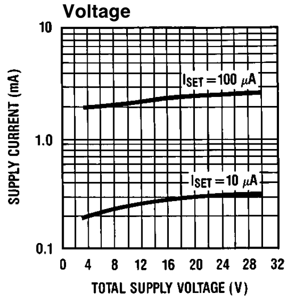
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

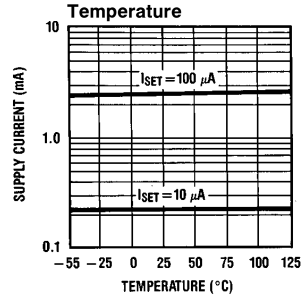
Supply Current vs I_{SET}



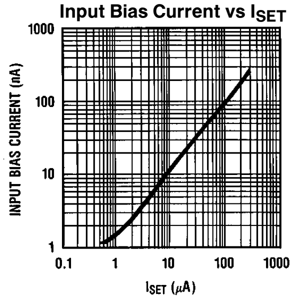
Supply Current vs Supply Voltage



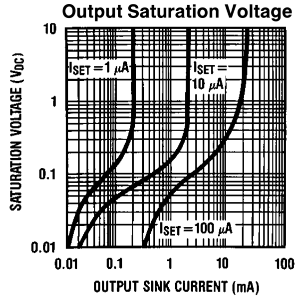
Supply Current vs Temperature



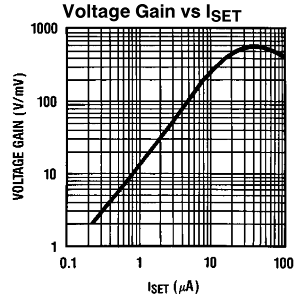
Input Bias Current vs I_{SET}



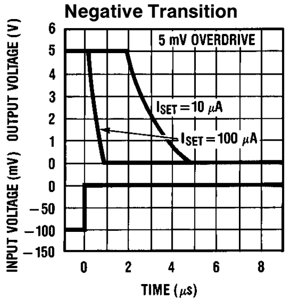
Output Saturation Voltage



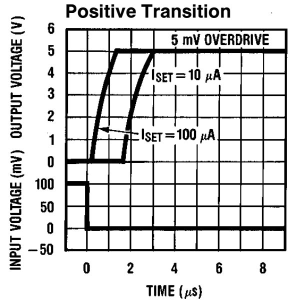
Voltage Gain vs I_{SET}



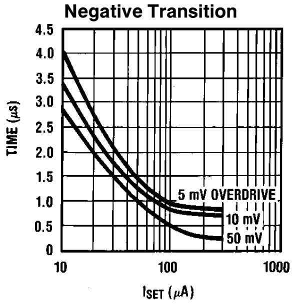
Response Time Negative Transition



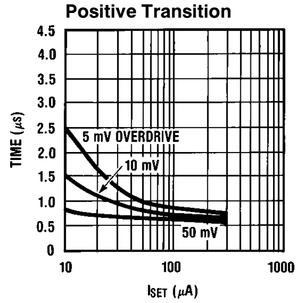
Response Time Positive Transition



Response Time Negative Transition



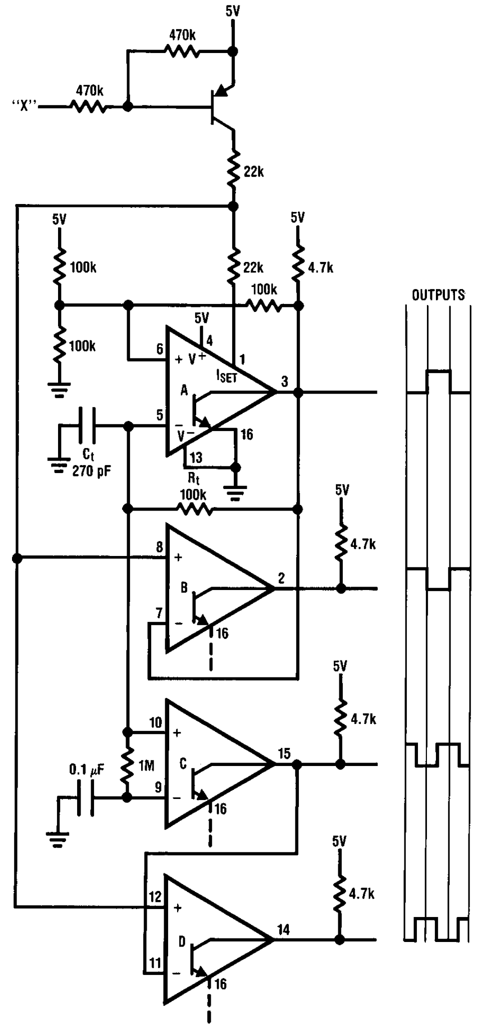
Response Time Positive Transition



TL/H/5023–3

Typical Applications

Gated 4-Phase Oscillator



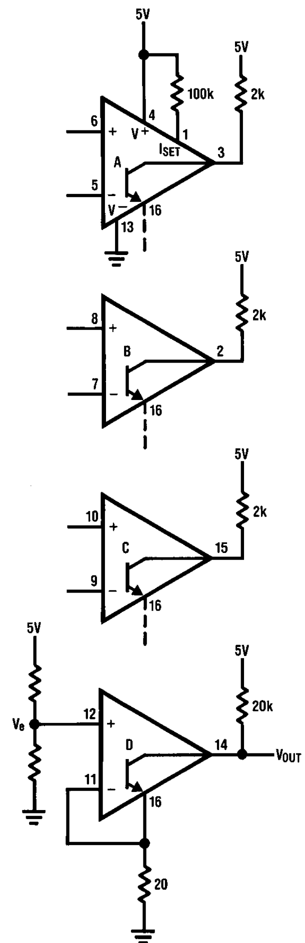
TL/H/5023–4

f = 20 kHz

$$f = \frac{1}{1.6 \bullet R_t \bullet C_t}$$

All four phases run when X is low. When X is high, oscillation stops and power drain is zero.

"Voting" Comparator

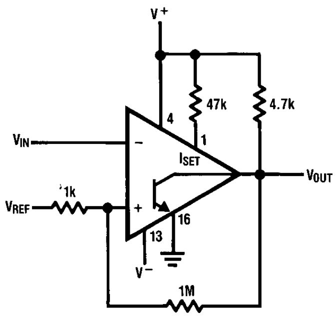


TL/H/5023–5

If V_E = 0.25V, then V_{OUT} will be low if 1 of the 3 other outputs are low. Choice of V_E = 0.50V causes V_{OUT} to be low if 2 of the 3 other outputs are low; V_E = 0.75V will cause V_{OUT} to be low if all 3 other outputs are low.

Typical Applications (Continued)

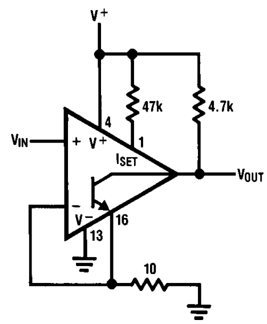
Ordinary Hysteresis



TL/H/5023–6

It is a good practice to add a few millivolts of positive feedback to prevent oscillation when the input voltage is near the threshold.

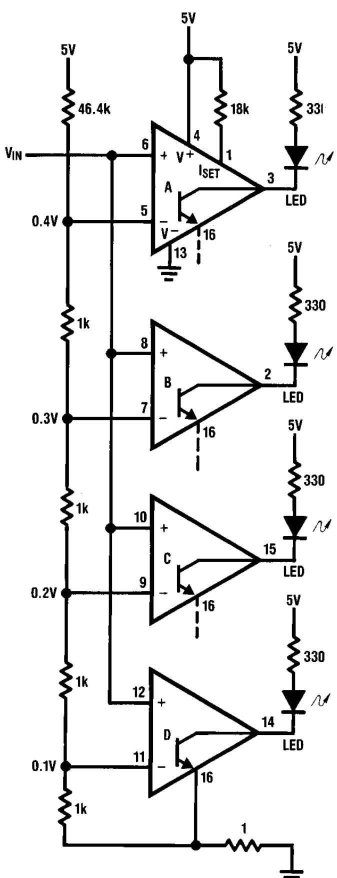
Hysteresis from Emitter



TL/H/5023–7

Positive feedback from the emitter can also prevent oscillations when V_{IN} is near the threshold.

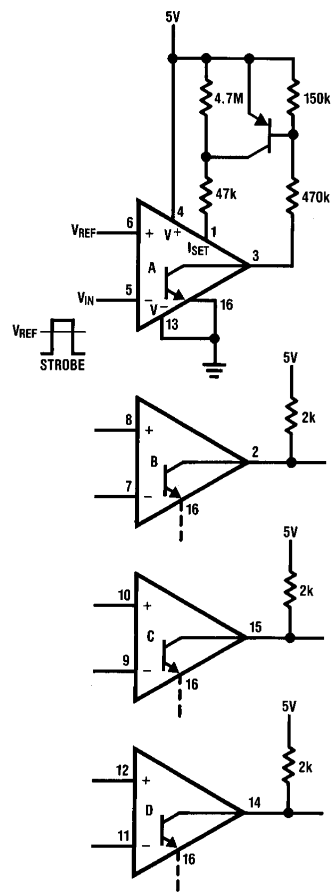
Bar-Graph Display



TL/H/5023–8

The positive feedback from pin 16 provides hysteresis.

Level-Sensitive Strobe

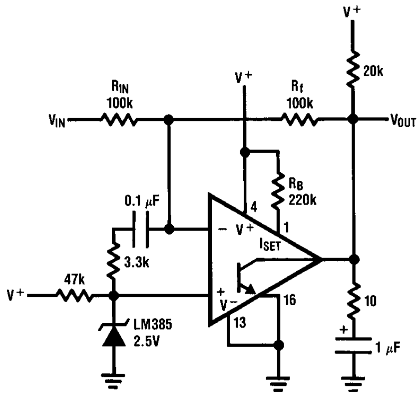


TL/H/5023–9

Comparators B, C, and D do not respond until activated by the signal applied to comparator A.

Typical Applications (Continued)

Slow Op Amp (Inverter)

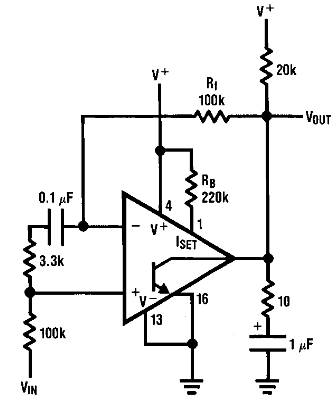


TL/H/5023–10

$R_B = V^+/20\ \mu A$

Unlike most comparators, the LP365 can be used as an op amp, if suitable R-C damping networks are used.

Slow Op Amp (Unity-Gain Follower)

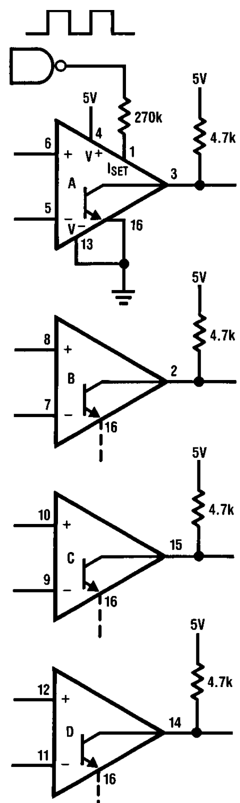


TL/H/5023–11

$R_B = V^+/20\ \mu A$

The LP365 can also be used as a high-input-impedance follower-amplifier with the damping components shown.

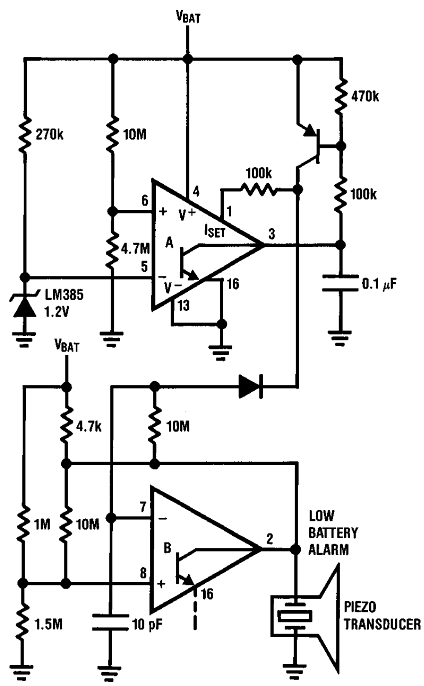
Chopping Outputs



TL/H/5023–12

Chopping the outputs by modulating the I_{SET} current allows data to be transmitted via opto-couplers, transformers, etc.

Low Battery Detector



TL/H/5023–13

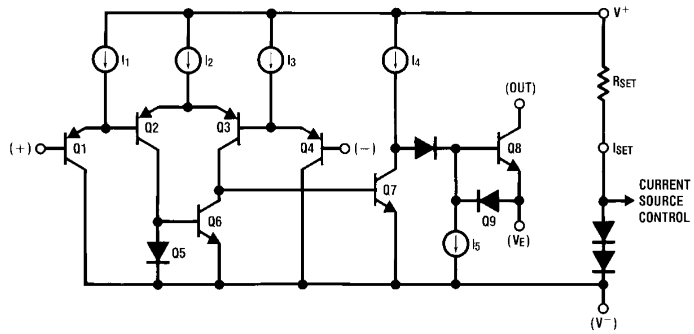
I_S @ 6V = 45 μA

I_S @ 3.8V = 1 μA

f = 3 kHz

Comparator A detects when the supply voltage drops to 4V and enables comparator B to drive a piezoelectric alarm.

Simplified Schematic

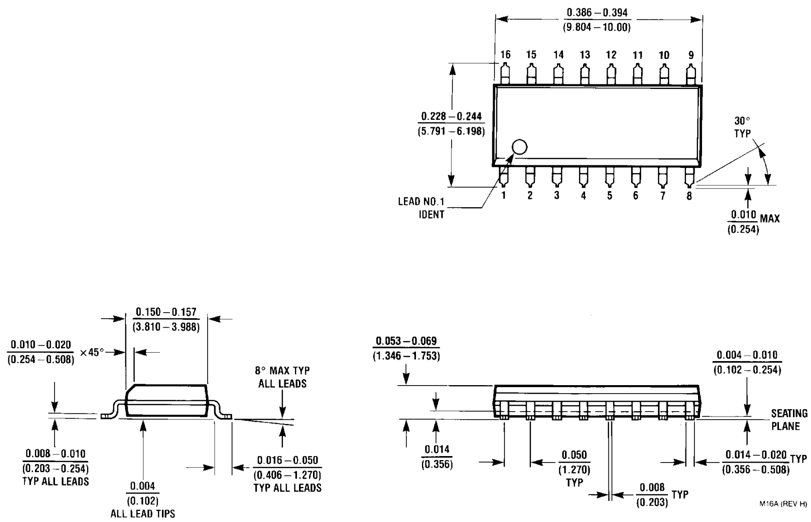


TL/H/5023–14

Current sources are programmed by I_{SET}

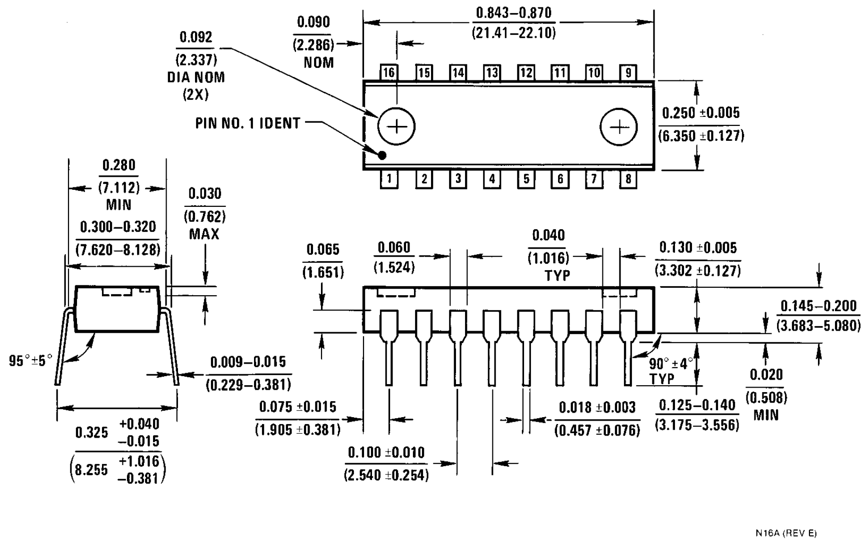
V_E is common to all 4 comparators

Physical Dimensions inches (millimeters)



Plastic Surface-Mount Package (M)
Order Number LP365M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LP365AN or LP365N
NS Package Number N16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408