HITACHI MICROPROCESSOR/PERIPHERAL CROSS REFERENCE

Hitachi is in the process of converting many microprocessor part numbers to "industry standard" generic part numbers. A complete list showing both the "old" and "new" part numbers is shown in figure 1. The use of industry standard part numbers will greatly simplify the interface between Hitachi and our customers.

Beginning JULY 1, 1981, all orders should be entered using the "new" part numbers only.

Note that during the conversion process, product shipped by Hitachi will be marked 1 of 2 ways (see figure 2).

1) marked with the "old" Hitachi part number...

or

2) marked with a dual number ("old" and "new")

At the completion of the conversion (approximately JANUARY 1, 1982) all product will be shipped with the dual marking (2 above).

If this conversion plan poses problems, or you have any questions, please contact Hitachi Microprocessor Marketing.

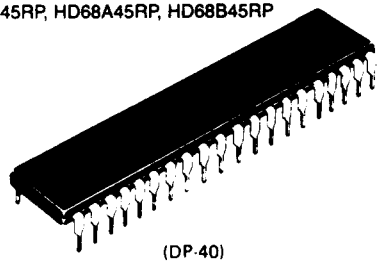
Description	"old" HITACHI number	"new" HITACHI number	MOTOROLA number
16/32 bit microprocessing unit, 8 mhz	————	**HD68000-8**	MC68000L
16/32 bit microprocessing unit, 6 mhz	————	**HD68000-6**	MC68000L6
16/32 bit microprocessing unit, 4 mhz	————	**HD68000-4**	MC68000L4
8/16 bit microprocessing unit, 1mhz	HD6809P	**HD6809P**	MC6809P
8/16 bit microprocessing unit, 1.5mhz	HD68A09P	**HD68A09P**	MC68A09P
8/16 bit microprocessing unit, 2mhz	HD68B09P	**HD68B09P**	MC68B09P
8 bit microprocessing unit, 1mhz	HD46800DP	**HD6800P**	MC6800P
8 bit microprocessing unit, 1.5mhz	HD468A00P	**HD68A00P**	MC68A00P
8 bit microprocessing unit, 2mhz	HD468B00P	**HD68B00P**	MC68B00P
8 bit microprocessing unit, 1mhz with clock and 128 bytes RAM	HD46802SP	**HD6802SP**	MC6802P
8 bit microprocessing unit, 1mhz with clock and 256 bytes RAM	————	**HD6802WP**	————
128 x 8 static RAM, 450ns access time	HM46810P	**HD6810P**	MC6810P
128 x 8 static RAM, 360ns access time	HM468A10P	**HD68A10P**	MC68A10P
Peripheral interface adapter, 1mhz	HD46821P	**HD6821P**	MC6821P
Peripheral interface adapter, 1.5mhz	HD468A21P	**HD68A21P**	MC68A21P
Peripheral interface adapter, 2mhz	HD468B21P	**HD68B21P**	MC68B21P
Programmable timer module, 1mhz	————	**HD6840P**	MC6840P
Programmable timer module, 1.5mhz	————	**HD68A40P**	MC68A40P
Programmable timer module, 2mhz	————	**HD68B40P**	MC68B40P
Floppy disk controller, 1mhz	HD46503SP	**HD6843SP**	MC6843P
Floppy disk controller, 1.5mhz	HD46503SP-1	**HD68A43SP**	MC68A43P
8 bit DMA controller, 1mhz	HD46504RP	**HD6844P**	MC6844P
8 bit DMA controller, 1.5mhz	HD46504RP-1	**HD68A44P**	MC68A44P
8 bit DMA controller, 2mhz	HD46504RP-2	**HD68B44P**	MC68B44P
CRT controller, 1mhz	HD46505RP	**HD6845RP**	MC6845P
CRT controller, 1.5mhz	HD46505RP-1	**HD68A45RP**	MC68A45P
CRT controller, 2mhz	HD46505RP-2	**HD68B45RP**	MC68B45P
CRT controller (enhanced), 1 mhz	HD46505SP	**HD6845SP**	————
CRT controller (enhanced), 1.5mhz	HD46505SP-1	**HD68A45SP**	————
CRT controller (enhanced), 2mhz	HD46505SP-2	**HD68B45SP**	————
ROM, I/O, Timer combo, 1mhz	————	**HD6846P**	MC6846P
Asynchronous comm interface, 1mhz	HD46850P	**HD6850P**	MC6850P
Asynchronous comm interface, 1.5mhz	HD468A50P	**HD68A50P**	MC68A50P
Synchronous comm interface, 1mhz	HD46852P	**HD6852P**	MC6852P
Synchronous comm interface, 1.5mhz	HD468A52P	**HD68A52P**	MC68A52P
Analog data acquisition unit, 1mhz	HD46508P	**HD46508P**	————
Analog data acquisition unit, 1.5mhz	HD46508P-1	**HD46508P-1**	————
Analog data acquisition unit, 1mhz (enhanced)	HD46508PA	**HD46508PA**	————
Analog data acquisition unit, 1.5mhz (enhanced)	HD46508PA-1	**HD46508PA-1**	————

Figure 1. Hitachi Microprocessor/Peripheral Cross Reference

HD6845R/HD6845S
CRT Controller (CRTC)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HD6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

HD6845SP, HD68A45SP, HD68B45SP
HD6845RP, HD68A45RP, HD68B45RP

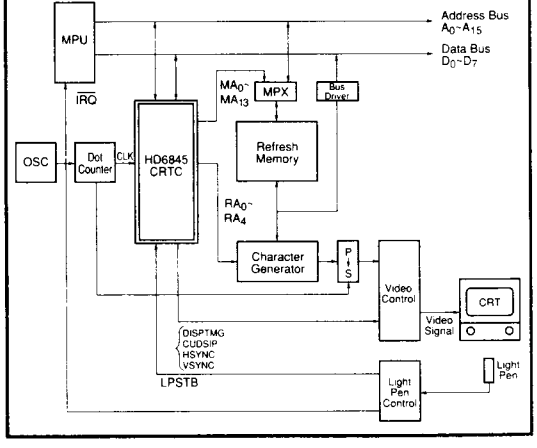


(DP-40)

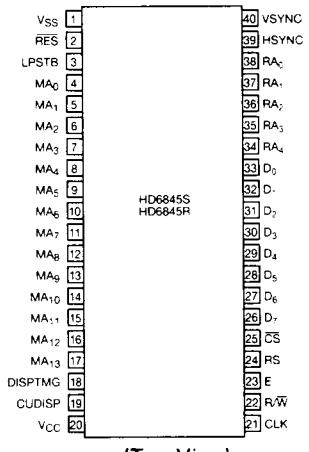
■ FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation (HD6845S)
- 3.0 MHz High Speed Display Operation (HD6845R)
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interface/Non-interface Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply

■ SYSTEM BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

CRTC	Bus Timing	CRT Display Timing
HD6845S	1.0 MHz	3.7 MHz max.
HD68A45S	1.5 MHz	
HD68B45S	2.0 MHz	
HD6845R	1.0 MHz	3.0 MHz max.
HD68A45R	1.5 MHz	
HD68B45R	2.0 MHz	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	-0.3 ~ +7.0	V
Input Voltage	V_{in} *	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	- 20 ~ + 75	°C
Storage Temperature	T_{stg}	- 55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

2

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC} *	4.75	5.0	5.25	V
Input Voltage	V_{IL} *	-0.3	–	0.8	V
	V_{IH} *	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	- 20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = -20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition		min	typ*	max	Unit
Input "High" Voltage	V_{IH}			2.0	–	V_{CC}	V
Input "Low" Voltage	V_{IL}			-0.3	–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 ~ 5.25V (Except D_0~D_7)		-2.5	–	2.5	μA
Three-State Input Current (off-state)	I_{TSI}	V_{in} = 0.4 ~ 2.4V V_{CC} = 5.25V (D_0~ D_7)		- 10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = -205 μA (D_0~ D_7)		2.4	–	–	V
		I_{LOAD} = -100 μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6 mA		–	–	0.4	V
Input Capacitance	C_{in}	V_{in} = 0 Ta = 25°C f = 1.0 MHz	D_0 ~ D_7	–	–	12.5	pF
			Other Inputs	–	–	10.0	pF
Output Capacitance	C_{out}	V_{in} = 0V, Ta = 25°C, f = 1.0 MHz		–	–	10.0	pF
Power Dissipation	P_D			–	600	1000	mW

* Ta = 25°C, V_{CC} = 5.0V

- **AC Characteristics**
  (V_{CC} = 5V ± 5%, T_a = −20 ~ +75°C, unless otherwise noted.)

1. TIMING OF CRTC SIGNAL

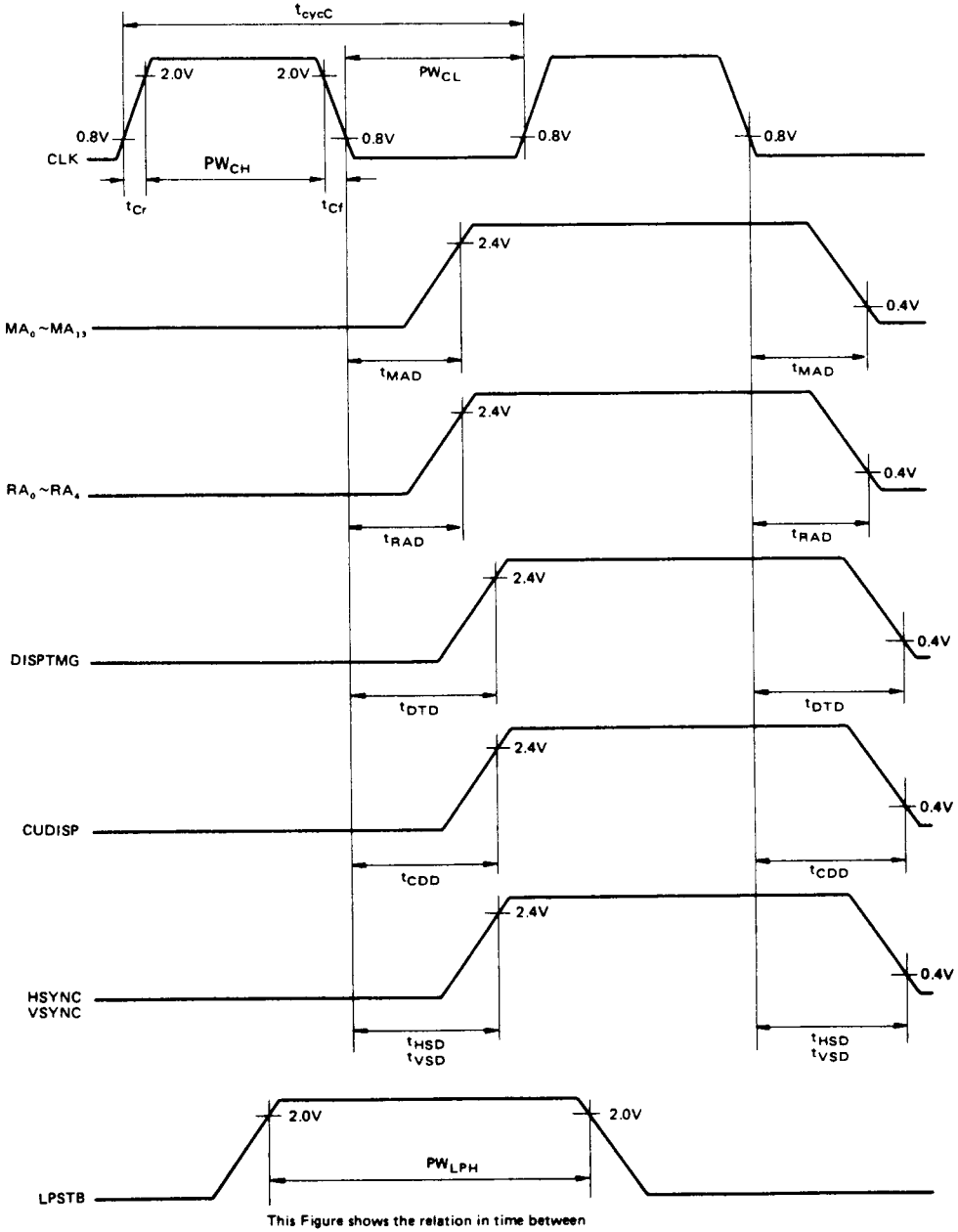
No.	Item	Symbol	Test Condition	HD6845R min	HD6845R typ	HD6845R max	HD6845S min	HD6845S typ	HD6845S max	Unit
1	Clock Cycle Time	t_{cycC}	Fig. 1	330	—	—	270	—	—	ns
2	Clock "High" Pulse Width	PW_{CH}		150	—	—	130	—	—	ns
3	Clock "Low" Pulse Width	PW_{CL}		150	—	—	130	—	—	ns
4	Rise and Fall Time for Clock Input	T_{Cr}, t_{Cf}		—	—	15	—	—	20	ns
5	Horizontal Sync Delay Time	t_{HSD}		—	—	250	—	—	200	ns
6	Light Pen Strobe Pulse Width	PW_{LPH}		80	—	—	60	—	—	ns
7	Light Pen Strobe Uncertain Time of Acceptance	t_{LPD1}	Fig. 2	—	—	80	—	—	70	ns
		t_{LPD2}		—	—	10	—	—	0	ns
8	Memory Address Delay Time	t_{MAD}	Fig. 1	—	—	160	—	—	160	ns
9	Raster Address Delay Time	t_{RAD}		—	—	160	—	—	160	ns
10	DISPTMG Delay Time	t_{DTD}		—	—	250	—	—	250	ns
11	CUDISP Delay Time	t_{CDD}		—	—	250	—	—	250	ns
12	Vertical Sync Delay Time	t_{VSD}		—	—	250	—	—	250	ns

2. MPU READ TIMING

Item	Symbol	Test Condition	HD6845R HD6845S min	HD6845R HD6845S typ	HD6845R HD6845S max	HD68A45R HD68A45S min	HD68A45R HD68A45S typ	HD68A45R HD68A45S max	HD68B45R HD68B45S min	HD68B45R HD68B45S typ	HD68B45R HD68B45S max	Unit
Enable Cycle Time	t_{cycE}	Fig. 3	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.28	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.28	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}		–	–	320	–	–	220	–	–	180	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}		–	–	460	–	–	360	–	–	250	ns

3. MPU WRITE TIMING

Item	Symbol	Test Condition	HD6845R HD6845S min	HD6845R HD6845S typ	HD6845R HD6845S max	HD68A45R HD68A45S min	HD68A45R HD68A45S typ	HD68A45R HD68A45S max	HD68B45R HD68B45S min	HD68B45R HD68B45S typ	HD68B45R HD68B45S max	Unit
Enable Cycle Time	t_{cycE}	Fig. 4	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.28	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.28	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Set Up Time	t_{DSW}		195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns



This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 10~15.

Figure 1 Time Chart of the CRTC

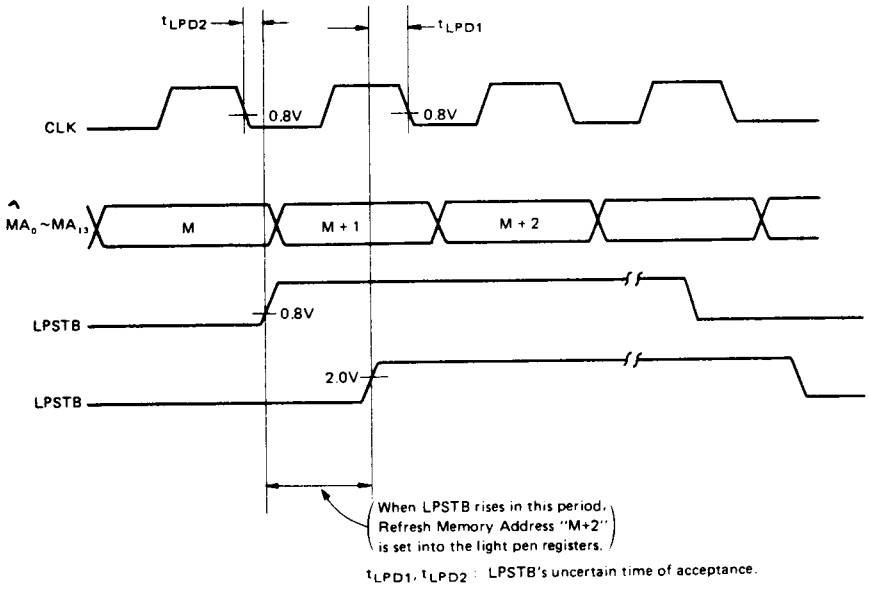


Figure 2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen registers.

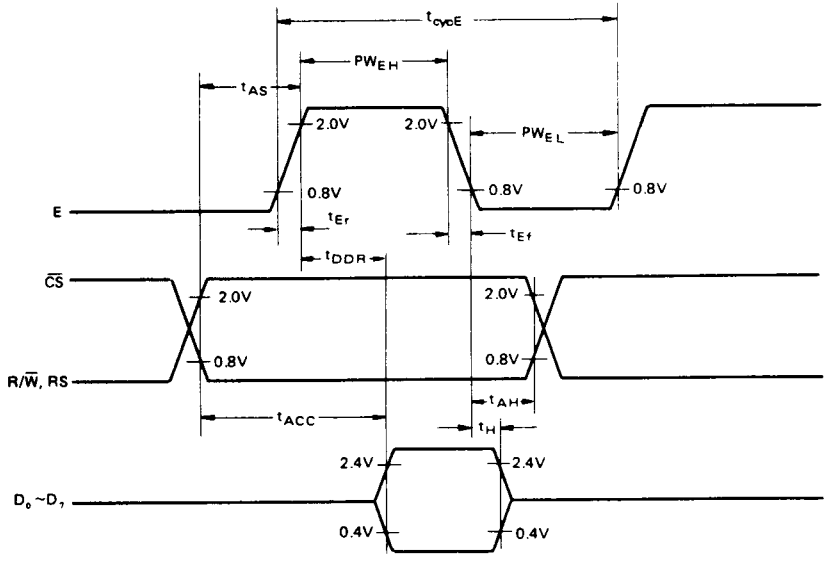


Figure 3 Read Sequence

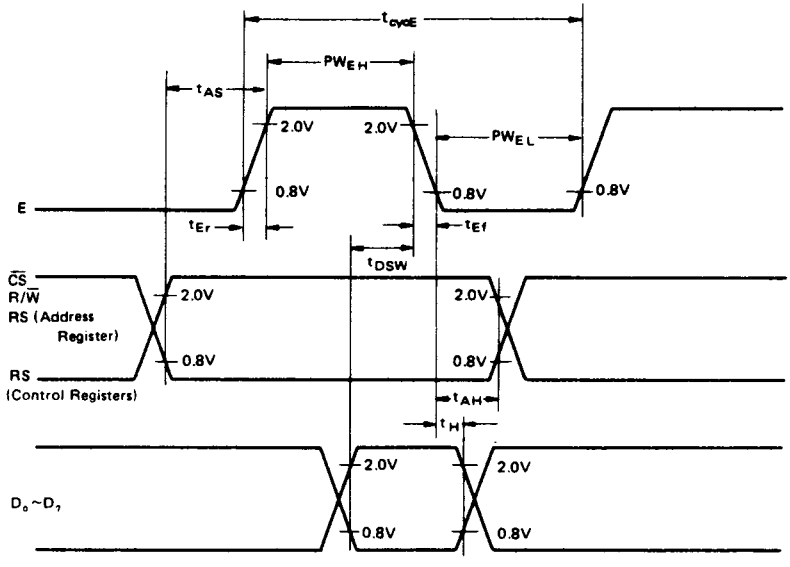
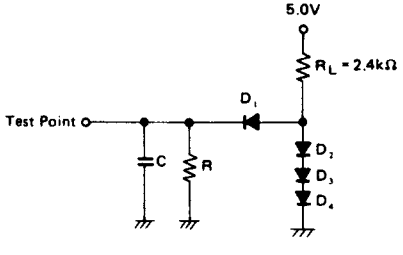


Figure 4 Write Sequence



C = 130pF (D_0~D_7)
= 30pF (Output signals except D_0~D_7)
R = 11kΩ (D_0~D_7)
= 24kΩ (Output signals except D_0~D_7)
D_1~D_4 are 1S2074Ⓗ or equivalent.

Figure 5 Test Loads

■ SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate RA_0~RA_4, DISPTMG, HSYNC, and VSYNC. RA_0~RA_4 are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit.

Linear address generator generates refresh memory address MA_0 ~MA_{13} to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16k words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

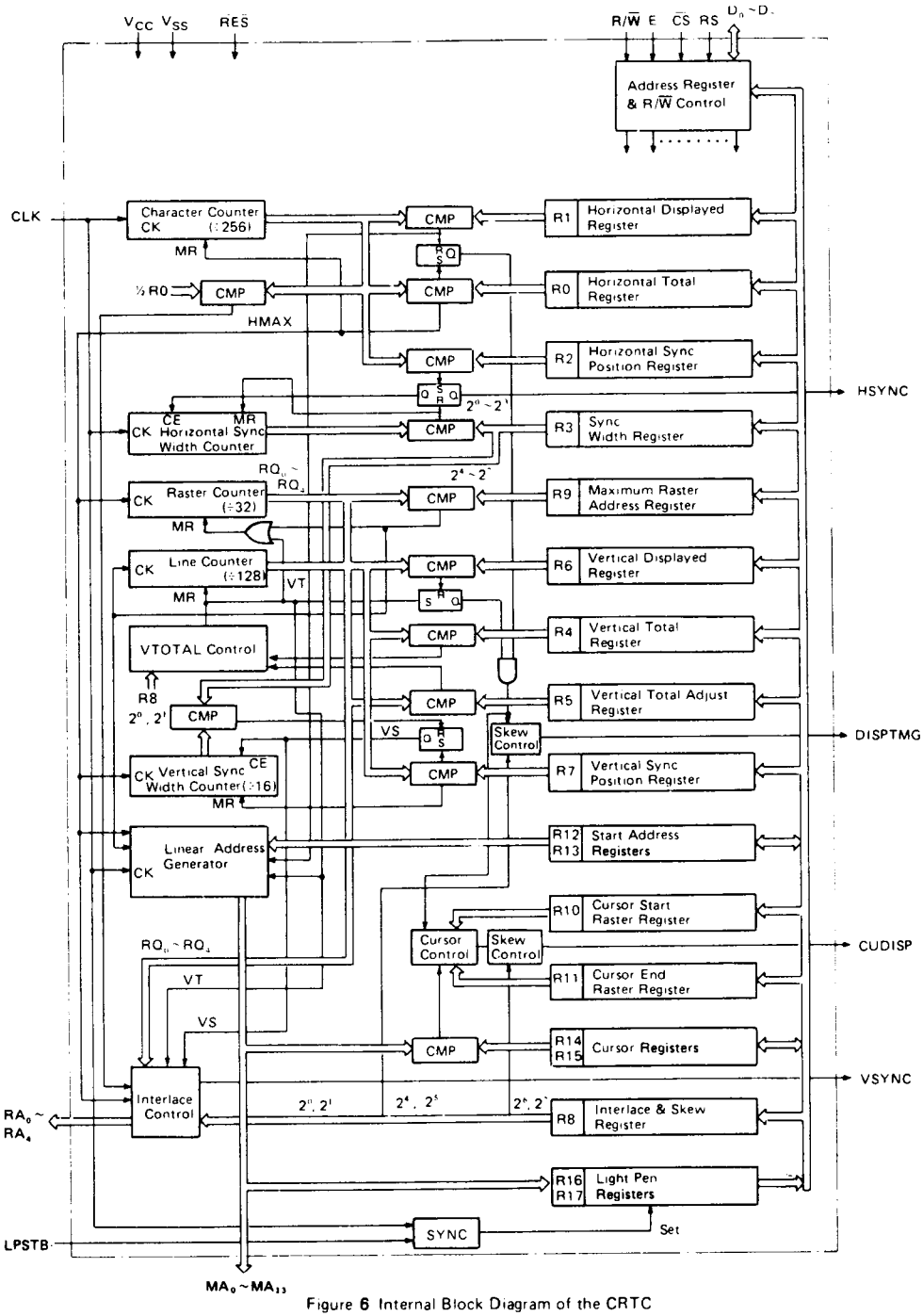


Figure 6 Internal Block Diagram of the CRTC

■ FUNCTION OF SIGNAL LINE

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

• Interface Signals to MPU

Bi-directional Data Bus ($D_0 \sim D_7$)

I/O Pin No. 33 ~ 26

Bi-directional data bus ($D_0 \sim D_7$) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain the high-impedance state except when MPU performs a CRTC read operation.

Read/Write (R/$\overline{W}$)

Input Pin No. 22

Read/Write signal (R/$\overline{W}$) controls the direction of data transfer between the CRTC and MPU. When R/$\overline{W}$ is at "High" level, data of CRTC is transferred to MPU. When R/$\overline{W}$ is at "Low" level, data of MPU is transferred to CRTC.

Chip Select ($\overline{CS}$)

Input Pin No. 25

Chip Select signal ($\overline{CS}$) is used to address the CRTC. When $\overline{CS}$ is at "Low" level, it enables Read/Write operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA of MPU is at "High" level.

Register Select (RS)

Input Pin No. 24

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A0) of MPU address bus.

Enable (E)

Input Pin No. 23

Enable signal (E) is used as strobe signal in MPU Read/Write operation with the CRTC internal registers. This signal is normally a derivative of the HD6800 System ϕ, clock.

Reset ($\overline{RES}$)

Input Pin No. 2

Reset signal ($\overline{RES}$) is an input signal used to reset the CRTC. When $\overline{RES}$ is at "Low" level, it forces the CRTC into the following status.

1) All the counters in the CRTC are cleared and the device stops the display operation.
2) All the outputs go down to "Low" level.
3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HD6800 family LSIs in the following functions and has restrictions for usage.

1) $\overline{RES}$ has capability of reset function only when LPSTB is at "Low" level.
2) The CRTC starts the display operation immediately after $\overline{RES}$ goes "High" level.

• Interface Signals to CRT Display Device

Character Clock (CLK)

Input Pin No. 21

CLK is a standard clock input signal which defines character timing for the CRTC display operation. CLK is normally derived from the external high-speed dot timing logic.

Horizontal Sync (HSYNC)

Output Pin No. 39

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

Vertical Sync (VSYNC)

Output Pin No. 40

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

Display Timing (DISPTMG)

Output Pin No. 18

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

Refresh Memory Address ($MA_0 \sim MA_{13}$)

Output Pin No. 4 ~ 17)

$MA_0 \sim MA_{13}$ are refresh memory address signals which are used to access to refresh memory is order to refresh the CRT screen periodically. These outputs enables 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

Raster Address ($RA_0 \sim RA_4$)

Output Pin No. 38 ~ 34)

$RA_0 \sim RA_4$ are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

Cursor Display (CUDISP)

Output Pin No. 19

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

Light Pen Strobe (LPSTB)

Input Pin No. 3

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address ($MA_0 \sim MA_{13}$) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

■ REGISTER DESCRIPTION

Table 1 Internal Registers Assignment

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	×	×	×	×	×	×			–	–	–								
0	0	×	×	×	×	×	AR	Address Register	–	×	○								
0	1	0	0	0	0	0	R0	Horizontal Total *	Character	×	○								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Character	×	○								
0	1	0	0	0	1	0	R2	Horizontal Sync* Position	Character	×	○								
0	1	0	0	0	1	1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	○	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0	0	1	0	0	R4	Vertical Total *	Line	×	○								
0	1	0	0	1	0	1	R5	Vertical Total Adjust	Raster	×	○								
0	1	0	0	1	1	0	R6	Vertical Displayed	Line	×	○								
0	1	0	0	1	1	1	R7	Vertical Sync * Position	Line	×	○								
0	1	0	1	0	0	0	R8	Interlace & Skew	–	×	○	C1	C0	D1	D0			V	S
0	1	0	1	0	0	1	R9	Maximum Raster Address	Raster	×	○								
0	1	0	1	0	1	0	R10	Cursor Start Raster	Raster	×	○		B	P					
0	1	0	1	0	1	1	R11	Cursor End Raster	Raster	×	○								
0	1	0	1	1	0	0	R12	Start Address(H)	–	○	○								
0	1	0	1	1	0	1	R13	Start Address(L)	–	○	○								
0	1	0	1	1	1	0	R14	Cursor(H)	–	○	○								
0	1	0	1	1	1	1	R15	Cursor (L)	–	○	○								
0	1	1	0	0	0	0	R16	Light Pen(H)	–	○	×								
0	1	1	0	0	0	1	R17	Light Pen(L)	–	○	×								

[NOTE] 1. The Registers marked *: (Written Value) = (Specified Value) – 1
2. Written Value of R9 is mentioned below.
   1) Non-interlace Mode / Interlace Sync Mode } (Written Value) = (Specified Value) – 1
   2) Interlace Sync & Video Mode
      (Written Value) = (Specified Value) –2
3. C0 and C1 specify skew of CUDISP.
   D0 and D1 specify skew of DISPTMG.
   When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of Vertical Sync Signal.
   wh0~wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. ○; Yes, ×; No

■ FUNCTION OF INTERNAL REGISTERS

• Address Register (AR)

This is a 5-bit register used to select 18 internal control registers (R0~R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0~R17 requires, first of all, to write the address of corresponding control register into this register. When RS and $\overline{CS}$ are at "Low" level, this register is selected.

• Horizontal Total Register (R0)

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, M-1 shall be programmed to this register. When programming for interlace mode, M must be even.

• Horizontal Displayed Register (R1)

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

• Horizontal Sync Position Register (R2)

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, H-1 shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

• Sync Width Register (R3)

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" can't be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

• Vertical Total Register (R4)

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, N-1 shall be programmed to this register.

• Vertical Total Adjust Register (R5)

This is a register used to program the optimum number to adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

• Vertical Displayed Register (R6)

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

VSW				Pulse Width
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H; Raster period

Table 3 Pulse Width of Horizontal Sync Signal

HSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	– (Note)
0	0	0	1	1 CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH; Character clock period
(Note) HSW = "0" can't be used.

2

- **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, V-1 shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

- **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP and DISPTMG.

Raster Scan Mode Program Bit (V, S)

Raster scan mode is programmed in the V, S bit.

Table 4 Raster Scan Mode (2^1, 2^0)

V	S	Raster Scan Mode
0	0	Non-interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync & video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

Skew Program Bit (C1, C0, D1, D0)

These are used to program the skew (delay) of CUDISP and DISPTMG.

Skew of these two kinds of signals are programmed separately.

Table 5 DISPTMG Skew Bit (2^5, 2^4)

D1	D0	DISPTMG
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Table 6 CUDISP Skew Bit (2^7, 2^6)

C1	C0	CUDISP
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew function is used to delay the output timing of CUDISP and DISPTMG in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

- **Maximum Raster Address Register (R9)***

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including line space. This register is programmed as follows.

Non-interlace Mode, Interlace Sync Mode

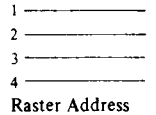
When total number of rasters is RN, RN-1 shall be programmed.

Interlace Sync & Video Mode

When total number of rasters is RN, RN-2 shall be programmed.

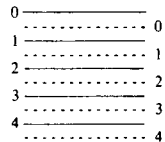
This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

Non-interlace Mode



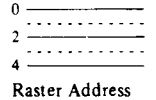
Total Number of Rasters:5
Programmed Value: Nr = 4
(The same as displayed total number of rasters)

Interlace Sync Mode



Total Number of Rasters:5
Programmed Value: Nr = 4
(In the interlace sync mode, total number of rasters in both the even and odd fields is ten. On programming, the half of it is defined as total number of rasters.)

Interlace Sync & Video Mode



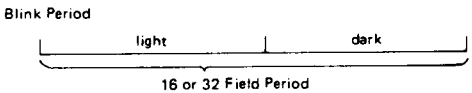
Total Number of Rasters:5
Programmed Value: Nr = 3
(Total number of rasters displayed in the even field and the odd field.)

- **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit (2^0~2^4) and the cursor display mode by higher 2-bit (2^5, 2^6).

Table 7 Cursor Display Mode (2^6, 2^5)

B	P	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink 16 Field Period
1	1	Blink 32 Field Period



*See Comparison of HD6845S and HD6845R on page 40.

- **Cursor End Raster Register (R11)**
  This is register used to program the cursor end raster address.

- **Start Address Register (R12, R13)**
  These are used to program the first address of refresh memory to read out.
  Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit (2^6, 2^7) of R12 are always "0".

- **Cursor Register (R14, R15)**
  These two read/write registers stores the cursor location. The higher 2-bit (2^6, 2^7) of R14 are always "0".

- **Light Pen Register (R16, R17)**
  These read only registers are used to catch the detection address of the light pen. The higher 2-bit (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

Restriction on Programming Internal Register

1) $0 < Nhd < Nht + 1 \leqq 256$
2) $0 < Nvd < Nvt + 1 \leqq 128$
3) $0 \leqq Nhsp \leqq Nht$
4) $0 \leqq Nvsp \leqq Nvt$*
5) $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr$ (Non-interlace, Interlace sync mode)
   $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr + 1$ (Interlace sync & video mode)
6) $2 \leqq Nr \leqq 30$ (Interlace Sync & Video mode)
7) $3 \leqq Nht$ (Except non-interlace mode)
   $5 \leqq Nht$ (Non-interlace mode only)

* In the interlace mode, pulse width is changed ±½ raster time when vertical sync signal extends over two fields.

Notes for Use

The method of directly using the value programmed in the internal registers of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asynchronously with the display operation.

Cursor Register

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

Start Address Register

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

■ OPERATION OF THE CRTC

- **Time Chart of CRT Interface Signals**
  The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 7 shows the CRT screen format. Fig. 10 shows the time chart of signals output from the CRTC.

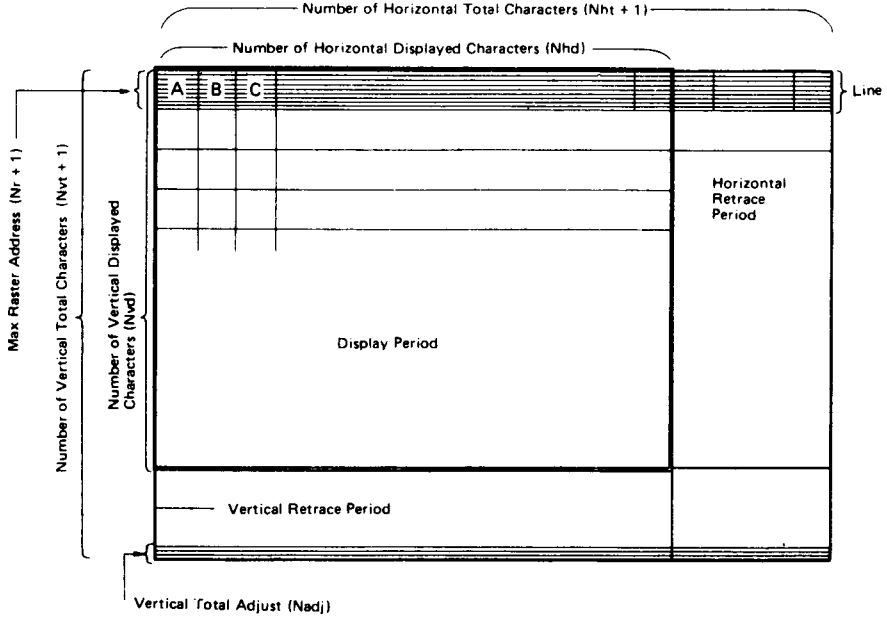


Figure 7 CRT Screen Format

Table 8 Programmed Values into the Registers

Register	Register Name	Value	Register	Register Name	Value
R0	Horizontal Total	Nht	R9	Max Raster Address	Nr
R1	Horizontal Displayed	Nhd	R10	Cursor Start Raster	
R2	Horizontal Sync Position	Nhsp	R11	Cursor End Raster	
R3	Sync Width	Nvsw, Nhsw	R12	Start Address (H)	0
R4	Vertical Total	Nvt	R13	Start Address (L)	0
R5	Vertical Total Adjust	Nadj	R14	Cursor (H)	
R6	Vertical Displayed	Nvd	R15	Cursor (L)	
R7	Vertical Sync Position	Nvsp	R16	Light Pen (H)	
R8	Interlace & Skew		R17	Light Pen (L)	

[NOTE] Nhd<Nht, Nvd<Nvt

The relation between values of Refresh Memory Address ($MA_0 \sim MA_{13}$) and Raster Address ($RA_0 \sim RA_4$) and the display position on the screen is shown in Fig. 16. Fig. 16 shows the case where the value of Start Address is 0.

- **Interlace Control**

Fig. 8 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and interlace sync & video mode.

Non-interlace Mode Control

In non-interlace mode, each field is scanned duplicatedly. The values of raster addresses ($RA_0 \sim RA_4$) are counted up one from 0.

Interlace Sync Mode Control

In the interlace sync mode, raster addressed in the even field and the odd field are the same as addressed in the non-interlace mode. One character pattern is displayed mutually and its displayed position in the odd field is set at 1/2 raster space down from that in the even field.

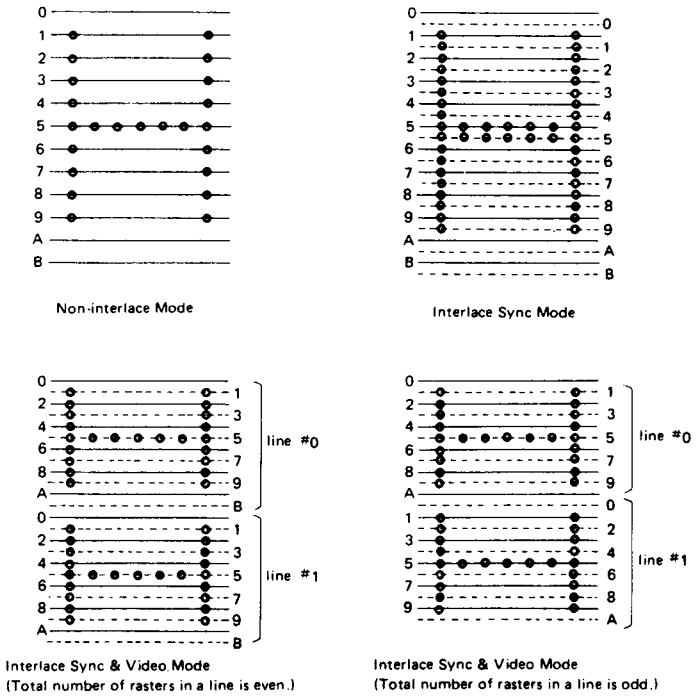


Figure 8 Example of Raster Scan Display

Interlace Sync & Video Mode Control

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9 The Output of Raster Address in Interlace Sync & Video Mode

Total Number of Rasters in a Line \ Field		Even Field	Odd Field
Even		Even Address	Odd Address
Odd	Even Line*	Even Address	Odd Address
	Odd Line*	Odd Address	Even Address

* Internal line address begins from 0.

1) Total number of rasters in a line is even;

When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;

When total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller the case of 1). Then interlace can be displayed more stably.

[NOTE] The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields may be shifted. Characters appears distroting on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 13 shows fine chart in each mode when interlace is performed.

- **Cursor Control**

Fig. 9 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register ≦ Cursor End Raster Register ≦ Maximum Raster Address Register.

Time chart of CUDISP is shown in Fig. 14 and Fig. 15.

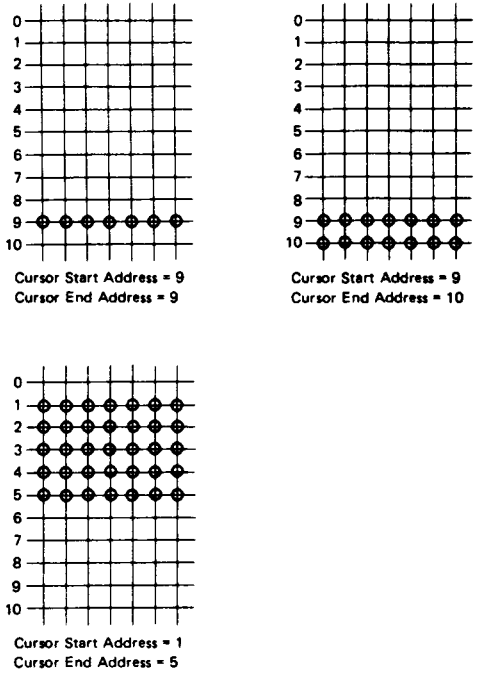


Figure 9 Cursor Control

2

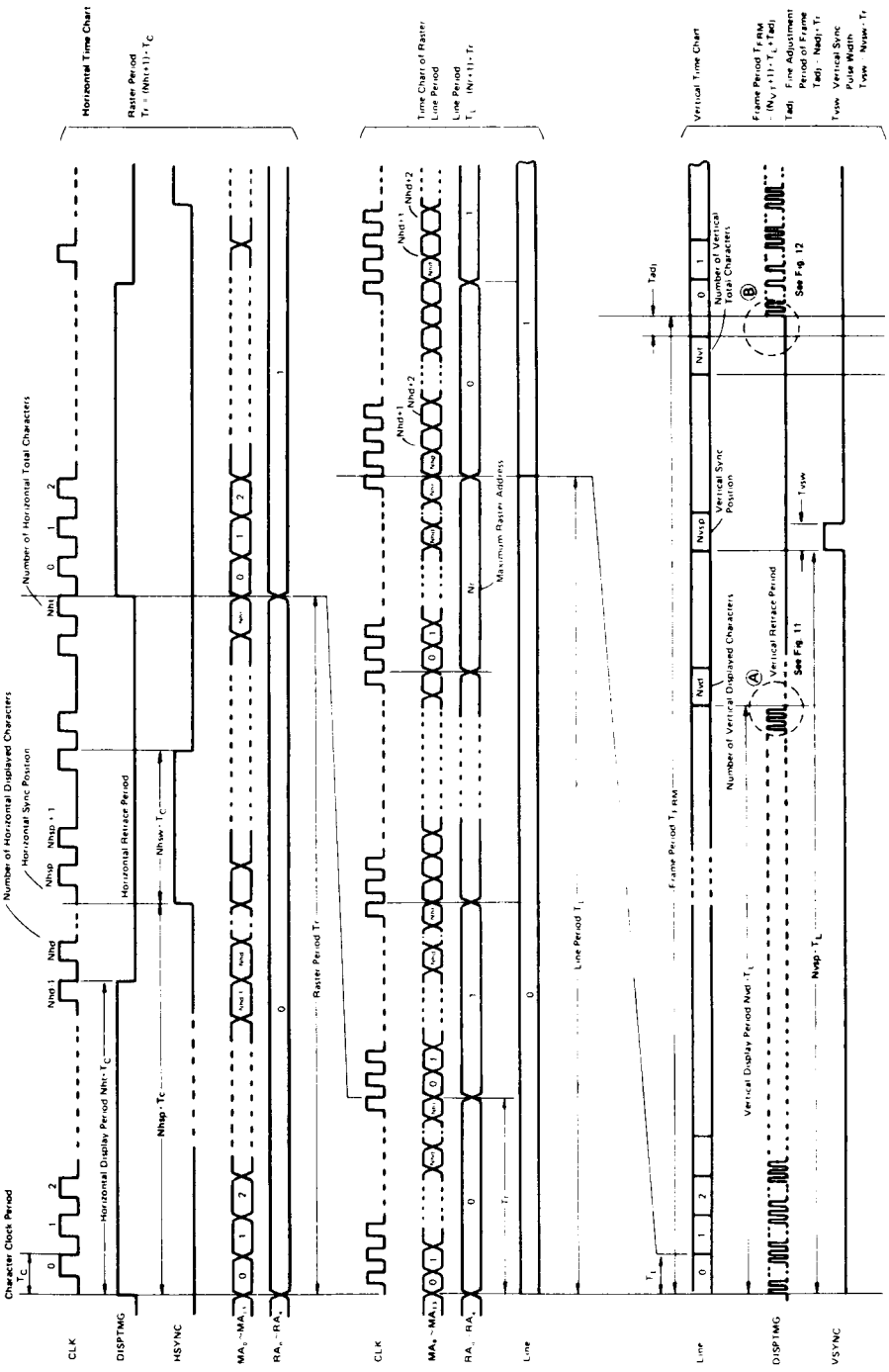


Figure 10 CRTC Time Chart

(Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.)

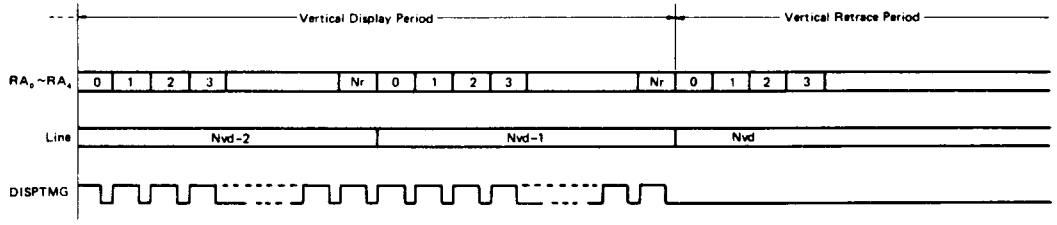


Figure 11 Switching from Vertical Display Period over to Vertical Retrace Period (Expansion of Fig. 10– Ⓐ)

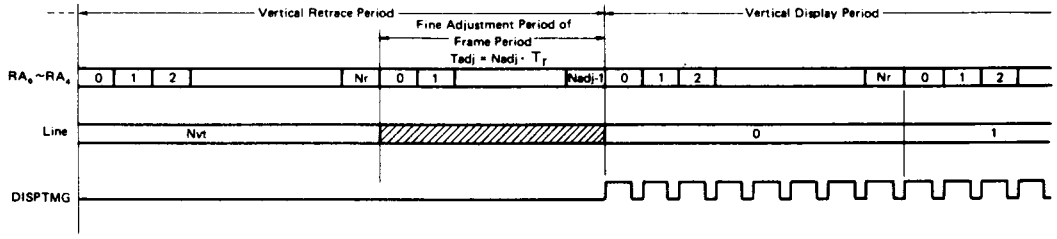


Figure 12 Fine Adjustment Period of Frame in Vertical Display
(Expansion of Fig. 10– Ⓑ)

2

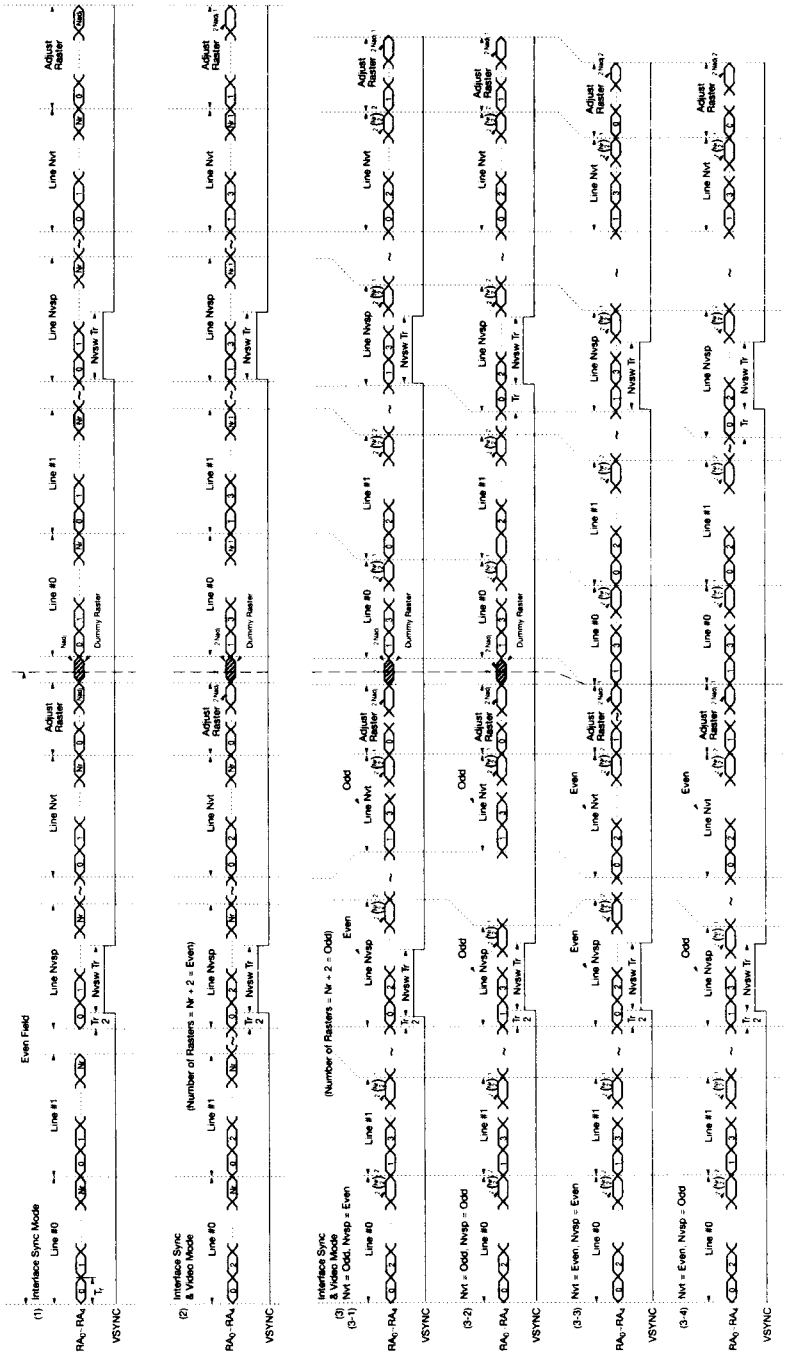


Figure 13 Interlace Control

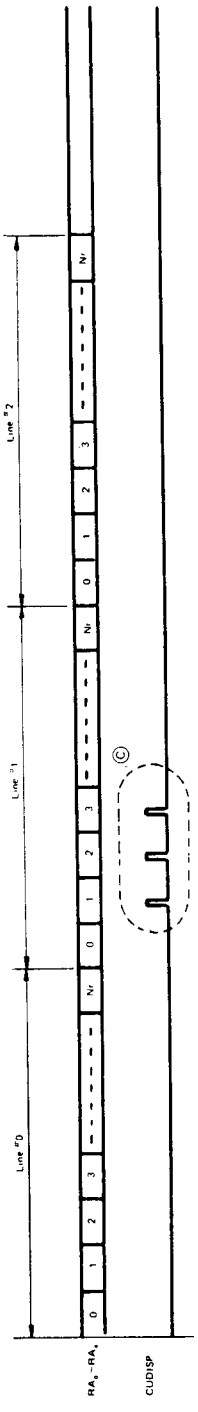


Figure 14 Relation between Line • Raster and CUDISP

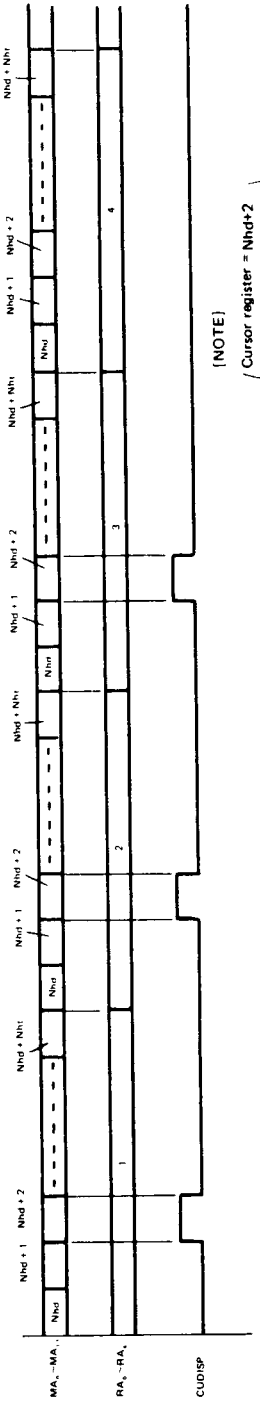


Figure 15 CUDISP Timing (Expansion of Fig. 14. ©)

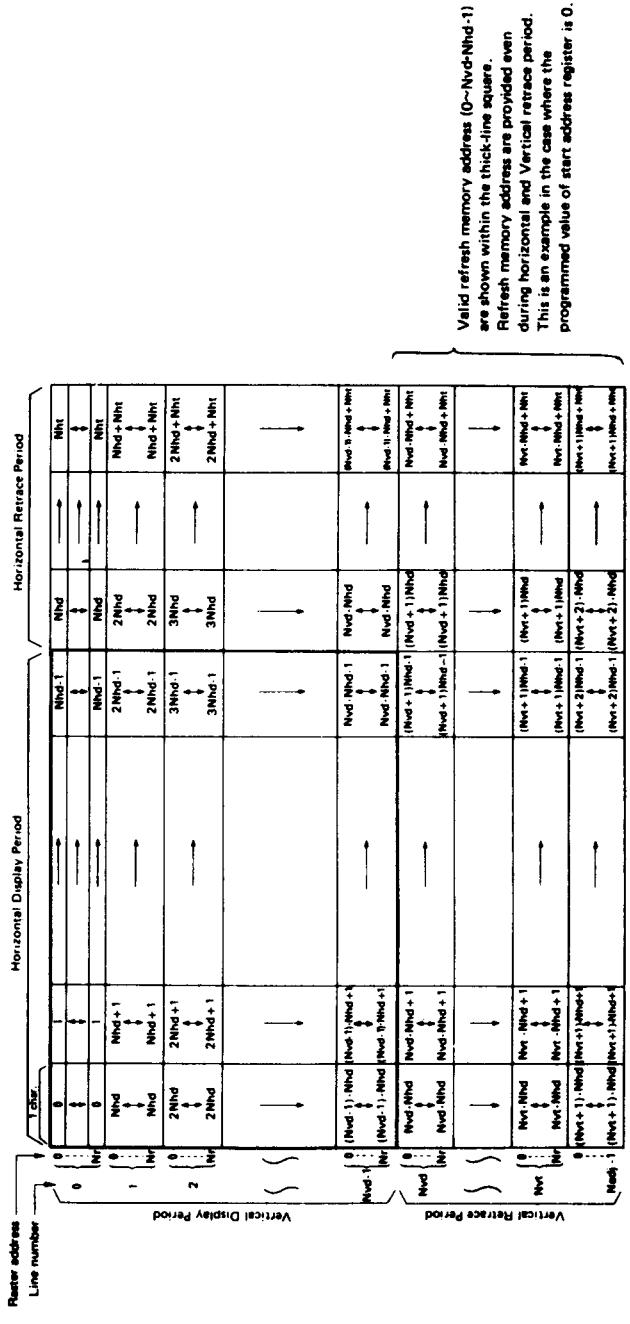


Figure 16 Refresh Memory Address (MA_0~MA_{13})

■ How to Use the CRTC

• Interface to MPU

As shown in Fig. 17, the CRTC is connected with the standard bus of MPU to control the data transfer between them. The CRTC address is determined by $\overline{CS}$ and RS, and the Read/Write operation is controlled by R/$\overline{W}$ and E. When $\overline{CS}$ is "Low" and RS is also "Low", the CRTC address register is selected. When $\overline{CS}$ is "Low" and RS is "High", one of 18 internal registers is selected.

$\overline{RES}$ is the system reset signal. When $\overline{RES}$ becomes "Low", the CRTC internal control logic is reset. But internal registers shown in Table 1 (R0~R17) are not affected by $\overline{RES}$ and remain unchanged.

The CRTC is designed so as to provide an interface to microcomputers, but adding some external circuits enables an interface to other data sources.

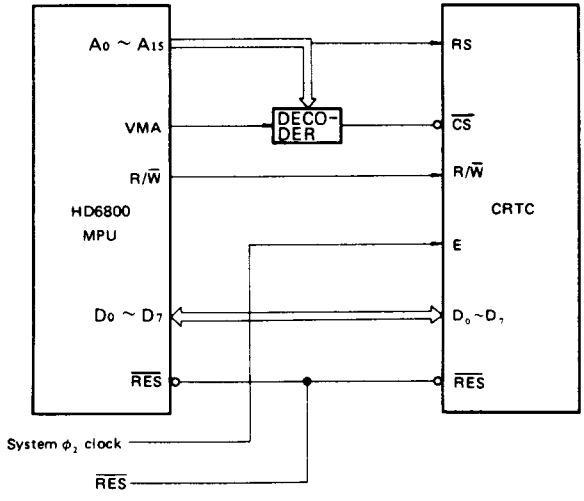


Figure 17 Interface to MPU

• Dot Timing Generating Circuit

CRTC's CLK input (21 pin) is provided with CLK which defines horizontal character time period from the outside. This CLK is generated by dot counter shown in Fig. 18. Fig. 18 shows a example of circuit where horizontal dot number of the character is "9". Fig. 19 shows the operation time chart of dot counter shown in Fig. 18. As this example shows explicitly, CLK is at "Low" level in the former half of horizontal character time and at "High" level in the latter half. It is necessary to be careful so as not to mistake this polarity.

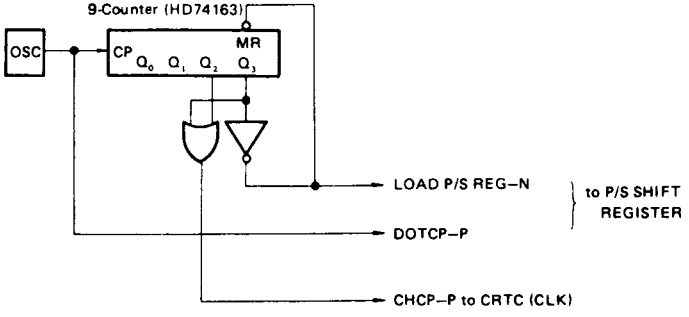


Figure 18 Example of Dot Counter

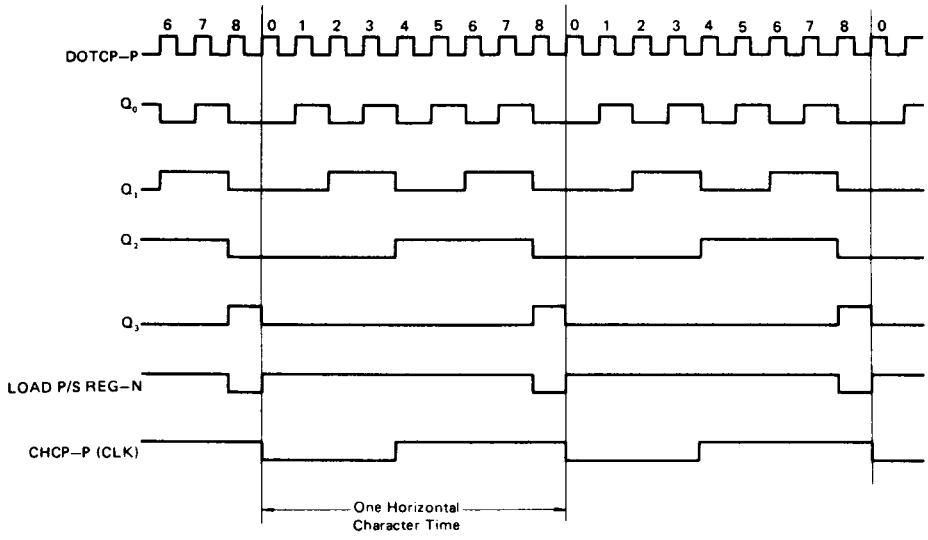


Figure 19 Time Chart of Dot Counter

■ INTERFACE TO DISPLAY CONTROL UNIT

Fig. 20 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC are sent out. DISPTMG is used to control the blank period of video signal. CUDISP is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 21 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG. CUDISP and DISPTMG should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG is AND-ed with character video signal, and CUDISP is Or-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 21 shows the example in the case that both refresh memory and Character Generator can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 24. This method is used when a few character needed to be displayed in horizontal direction on the screen.

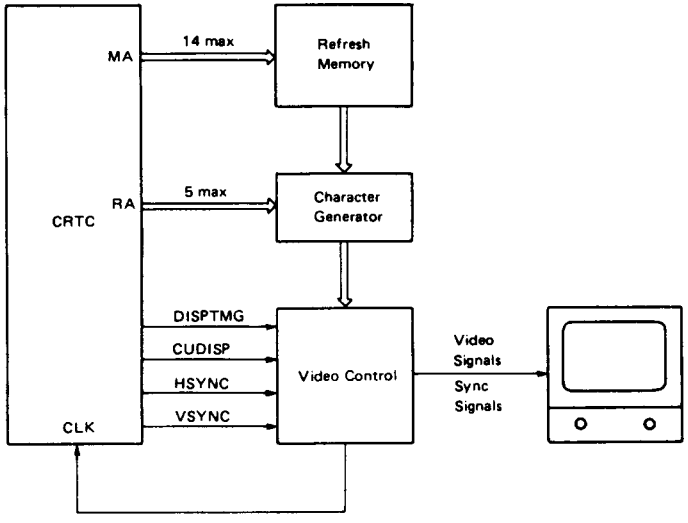


Figure 20 Interface to Display Control Unit

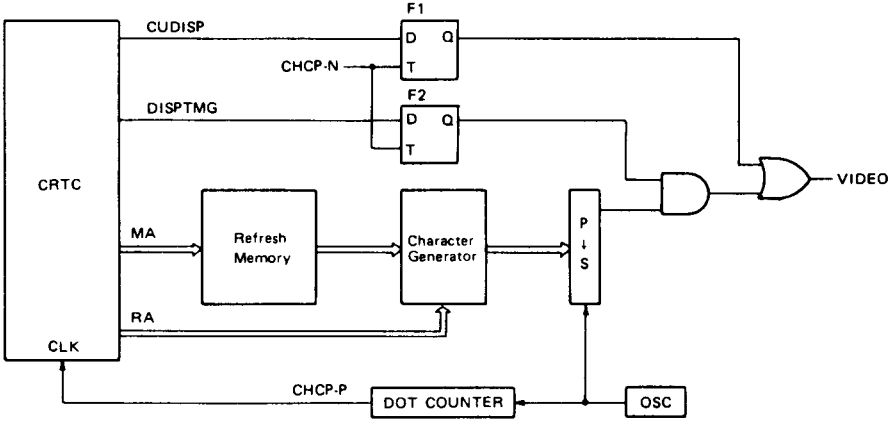


Figure 21 Display Control Unit (1)

When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and Character Generator cannot be accessed, the circuitry shown in Fig. 22 should be used. In this case refresh memory output shall be latched and Character Generator shall be accessed at the next cycle. The time chart in this case is shown in Fig. 25. CUDISP and DISPTMG should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig. 23 is adopted. The time chart in this case is shown in Fig. 26. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG by delaying for two-character time. Table 10 shows the circuitry selection standard of display units.

Table 10 Circuitry Standard of Display Control Unit

Case	Relation among t_{CH} Refresh Memory and Character Generator	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 21	0	0	0	0
2	RM Access + CG Access + $t_{MAD} \geqq t_{CH} >$ RM Access + t_{MAD}	Fig. 22	0	1	0	1
3	RM Access + $t_{MAD} \geqq t_{CH} >$ RM Access	Fig. 23	1	0	1	0

t_{CH} : CHCP Period; t_{MAD} : MA Delay
RM: Refresh Memory CG: Character Generator

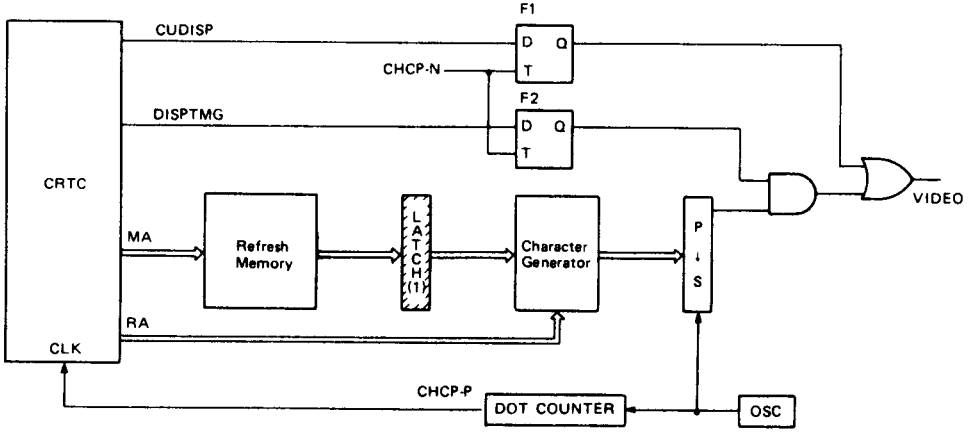


Figure 22 Display Control Unit (2)

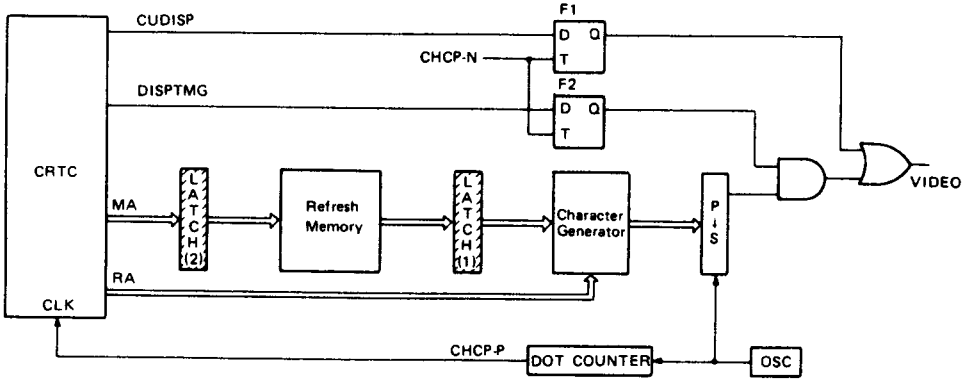


Figure 23 Display Control Unit (For high-speed display operation) (3)

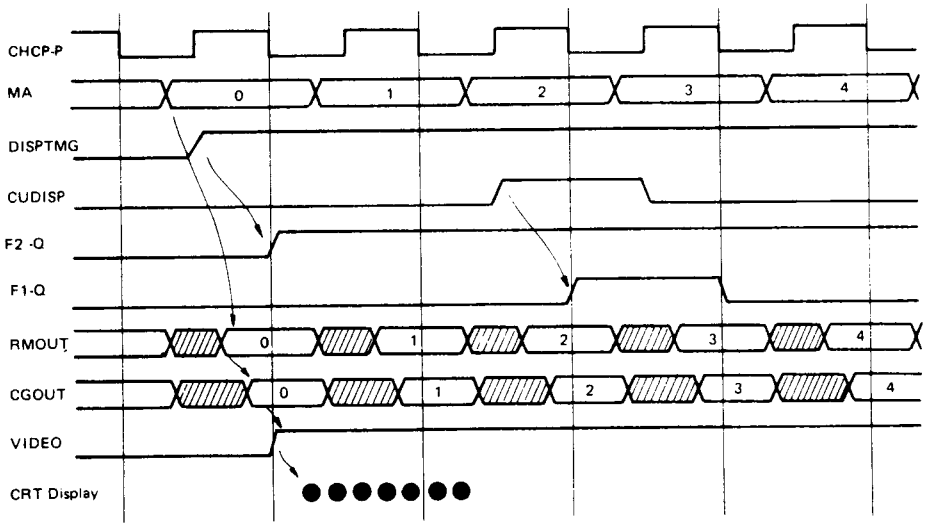


Figure 24 Time Chart of Display Control Unit (1)

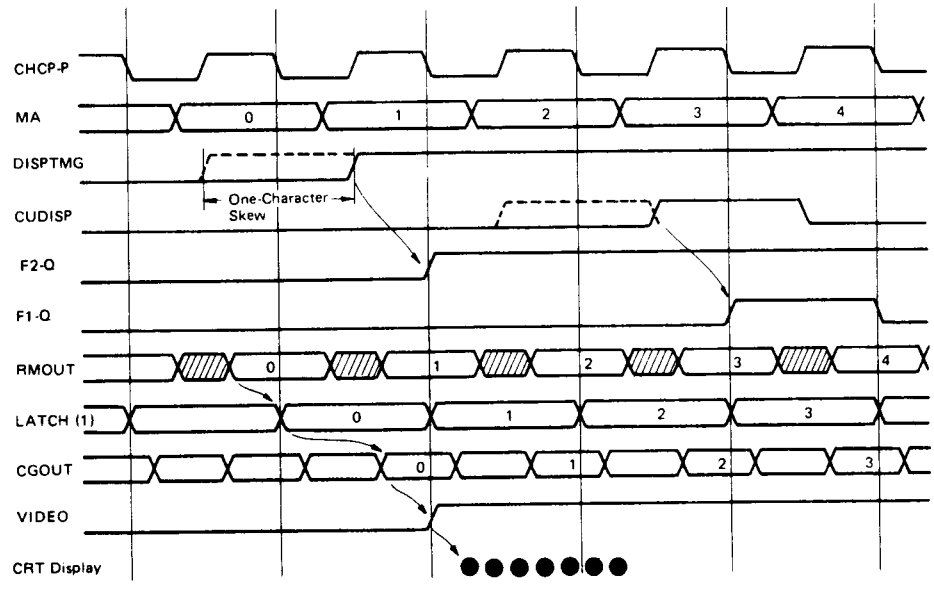


Figure 25 Time Chart of Display Control Unit (2)

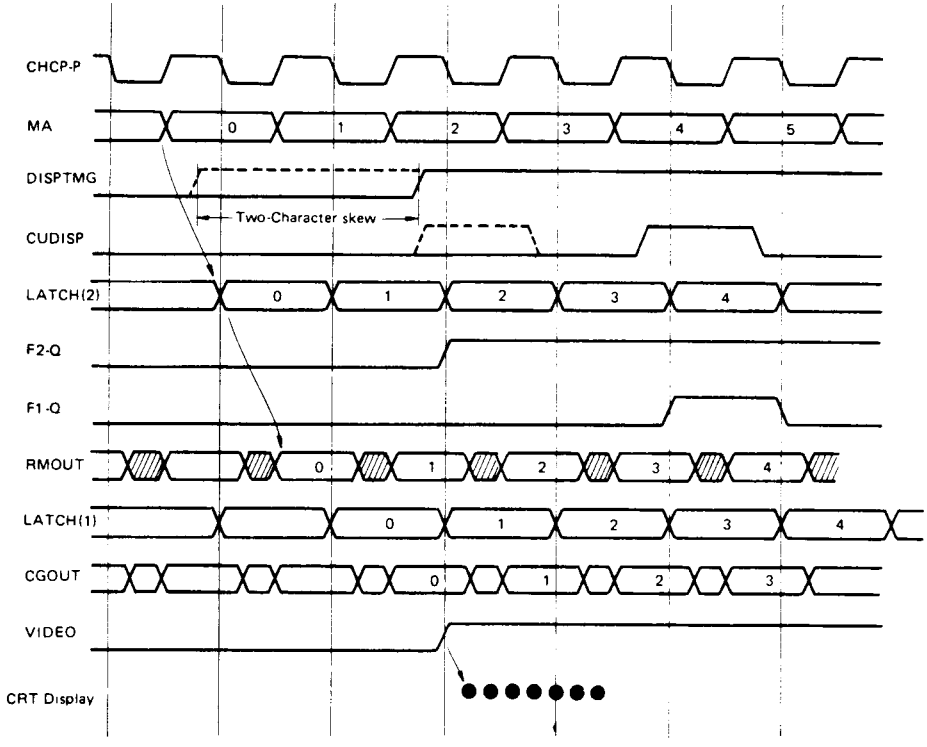


Figure 26 Time Chart of Display Unit (3)

Table 10A Parameter of Display

	Specification of CRT monitor	Display Configurations	CRTC Internal Register
Character Dot Size (Horizontal)		○	External Circuit
Character Dot Size (Vertical)		○	R9
Horizontal Total	○		R0
Horizontal Displayed	△	○	R1
Horizontal Sync Position	○		R2
Horizontal Sync Width	○		R3
Vertical Total	○		R4
Vertical Displayed	△	○	R6
Vertical Sync Width	○		F3
Interface mode		○	R8
Skew	△	○	R8
Cursor Size		○	R10, R110
Start Address		○	R12, R13
Cursor Address		○	R14, F15

△ This parameter is decided by specification of CRT monitor.

• HOW TO DECIDE PARAMETERS SET ON THE CRTC

• How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

Number of Horizontal Total Characters

Horizontal deflection frequency f_h is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$f_h = \frac{1}{t_C\,(N_{ht} + 1)}$$

where,

t_C : Cycle Time of CLK (Character Clock)
N_{ht} : Programmed Value of Horizontal Total Register (R0)

Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

1) Non-interlace Mode
$R_t = (N_{vt} + 1)(N_r + 1) + N_{adj}$
2) Interlace Sync Mode
$R_t = (N_{vt} + 1)(N_r + 1) + N_{adj} + 0.5$
3) Interlace Sync & Video Mode

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj}}{2} \quad \cdots\cdots\cdots\cdots \text{(a)}$$

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj} + 1}{2} \quad \cdots\cdots\cdots\cdots \text{(b)}$$

(a) is applied when both total numbers of vertical characters ($N_{vt} + 1$) and that of rasters in a line ($N_r + 2$) are odd.
(b) is applied when total number of rasters ($N_r + 2$) is even, or when ($N_r + 2$) is odd and total number of vertical characters ($N_{vt} + 1$) is even.

where,

R_t : Number of Total Rasters per frame (Including retrace period)
N_{vt} : Programmed Value of Vertical Total Register (R4)
N_r : Programmed Value of Maximum Raster Address Register (R9)
N_{adj} : Programmed Value of Vertical Total Adjust Register (R5)

Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to 15.

Horizontal Sync Position

As shown in Fig. 27, horizontal sync position is normally selected to be in the middle of horizontal retrace period. But there are some cases where is optimum sync position is not located in the middle of horizontal retrace period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

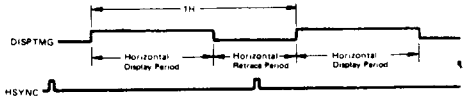


Figure 27 Time Chart of HSYNC

Vertical Sync Pulse Width

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of raster period. Programmed value can be selected within from 1 to 16.

Vertical Sync Position

As shown in Fig. 28, vertical sync position is normally selected to be in the middle of vertical retrace period. But there are some cases where its optimum sync position is not located in the middle of vertical retrace period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

• How to Decide Parameters Based on Screen Format

Dot Number of Characters (Horizontal)

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 29. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 30.

Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 29. Dot number of characters (vertical) is programmed to maximum raster address (R9) of CRTC.

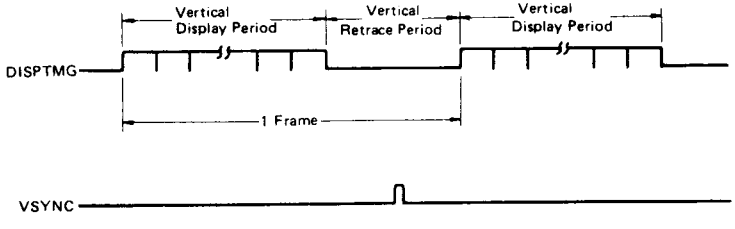


Figure 28 Time Chart of VSYNC

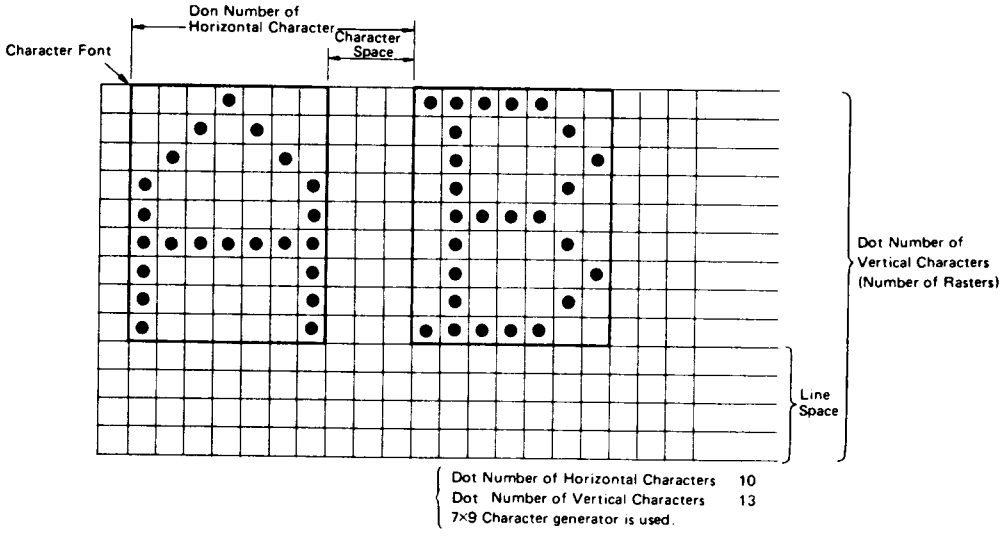


Figure 29 Dot Number of Horizontal and Vertical Characters

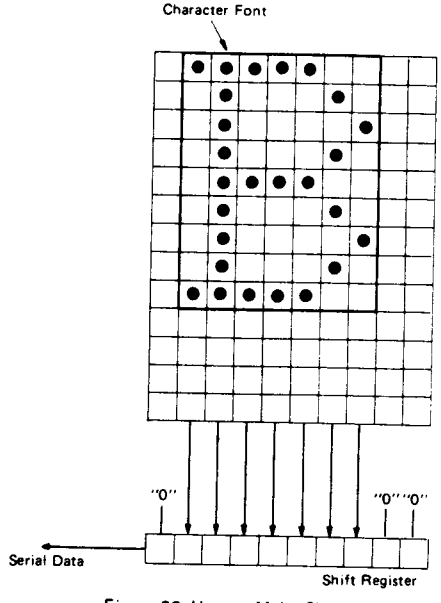


Figure 30 How to Make Character Space

Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (Rt) including vertical retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (Nadj) within specification of vertical deflection frequency.

Scan Mode

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 8.

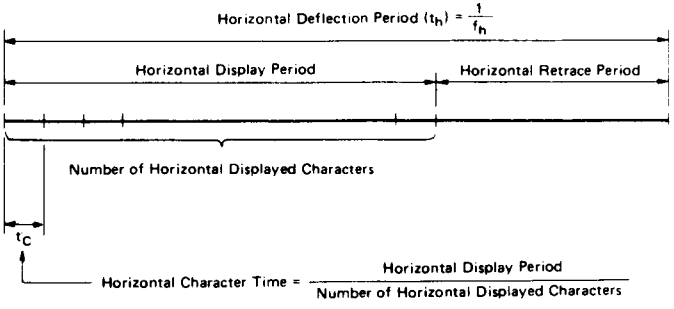


Figure 31 Number of Horizontal Displayed Characters

Table 11 Program of Scan Mode

V	S	Scan Mode	Main Usage
0	0	Non-interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-resolution CRT

[NOTE] In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

Cursor Display Method

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 9. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

Start Address

Start address resisters (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

Cursor Register

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

■ Applications of the CRTC

• Monochrome Character Display

Fig. 32 shows a system of monochrome character display. Character clock signal (CLK) is provided to the CRTC through OSC and dot counter. It is used as basic clock which drives internal control circuits. MPU is connected with the CRTC by standard bus and controls the CRTC initialization and read/write of internal registers.

Refresh memory is composed of RAM which has capacity of one frame at least and the data to be displayed is coded and stored. The data to refresh memory is changed through MPU

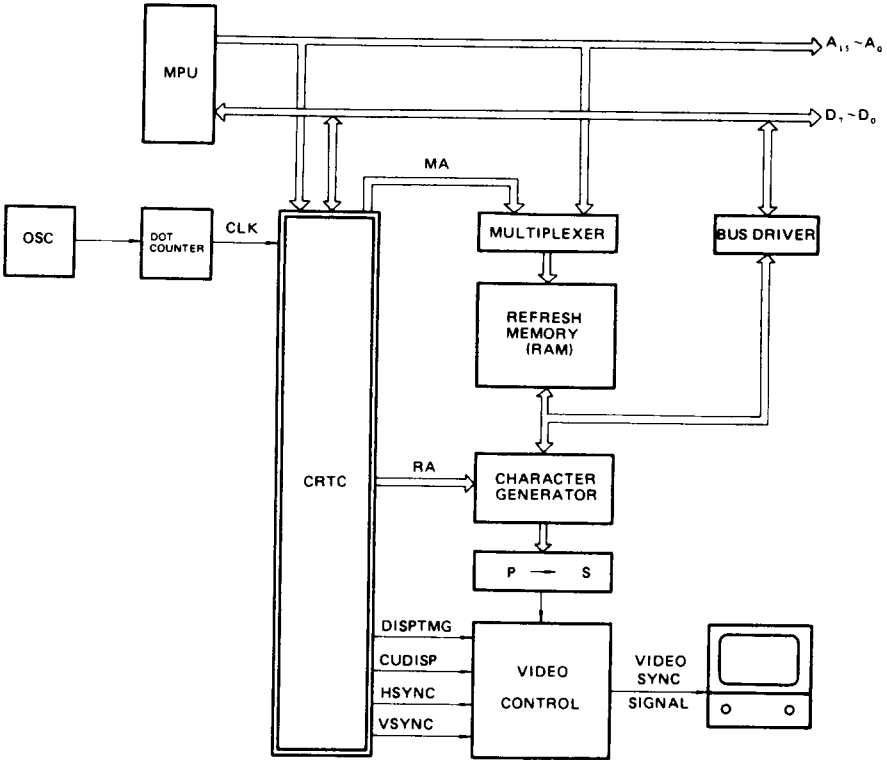


Figure 32 Monochrome Character Display

bus, while refresh memory is read out successively by the CRTC to display a static pattern on the screen. Refresh memory is accessed by both MPU and the CRTC, so it needs to change its address selectively by multiplexer. The CRTC has 14 MA (Memory Address output), but in fact some of them that are needed are used according to capacity of refresh memory.

Code output of refresh memory is provided to character generator. Character generator generates a dot pattern of a specified raster of a specified character in parallel according to code output from refresh memory and RA (Raster Address output) from the CRTC. Parallel-serial converter is normally composed of shift register to convert output of character generator into a serial dot pattern. Moreover, DISPTMG, CUDISP, HSYNC, and VSYNC are provided to video control circuit. It controls blanking for output of parallel-serial converter, mixes these signals with cursor video signal, and generates sync signals for an interface to monitor.

- **Color Character Display**

Fig. 33 shows a system of color character display. In this example, a 3-bit color control bit (R, G, B) is added to refresh memory in parallel with character code and provided to video control circuit. Video control circuit controls coloring as well as blanking and provides three primary color video signals (R, G, B signals) to CRT display device to display characters in seven kinds of color on the screen.

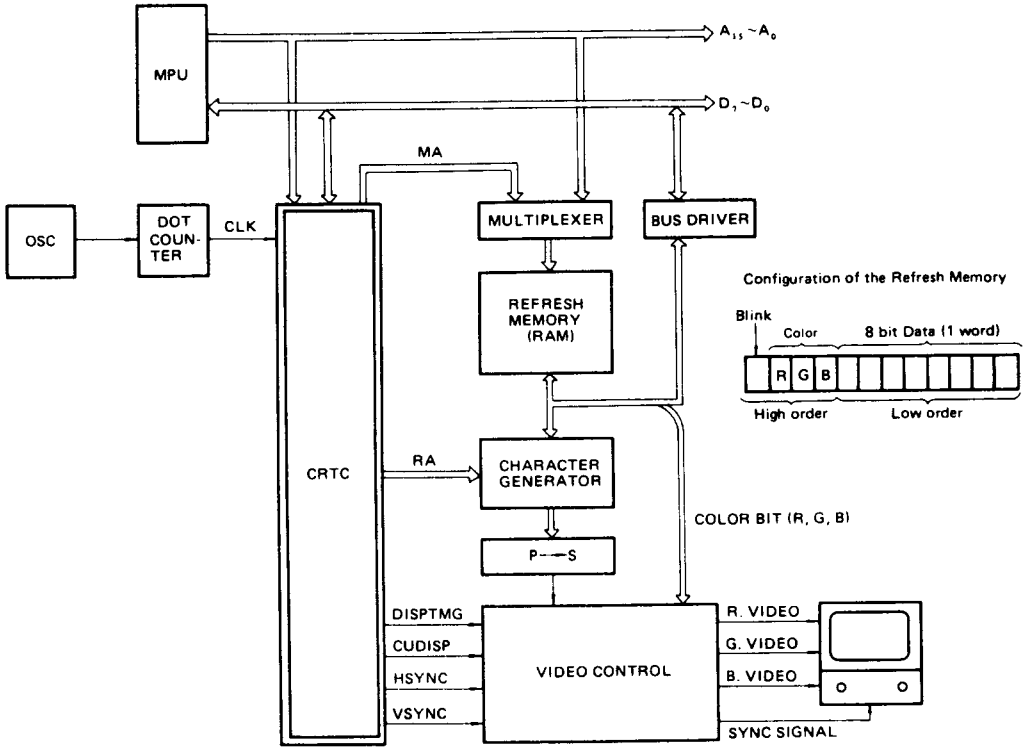


Figure 33 Color Character Display

- **Color limited Graphic Display**

Limited graphic display is to display simple figures as well as character display by combination of picture element which are defined in unit of one character.

As shown in Fig. 34, graphic pattern generator is set up in parallel with character generator and output of these generators are wire-ORed. Which generator is accessed depends on coded output of refresh memory.

In this example, graphic pattern generator adopts ROM, so only the combination of picture elements which are programmed to it is used for this graphic display system. Adopting RAM instead of ROM enables dynamically writable symbols in any combination on one display by changing the contents of them.

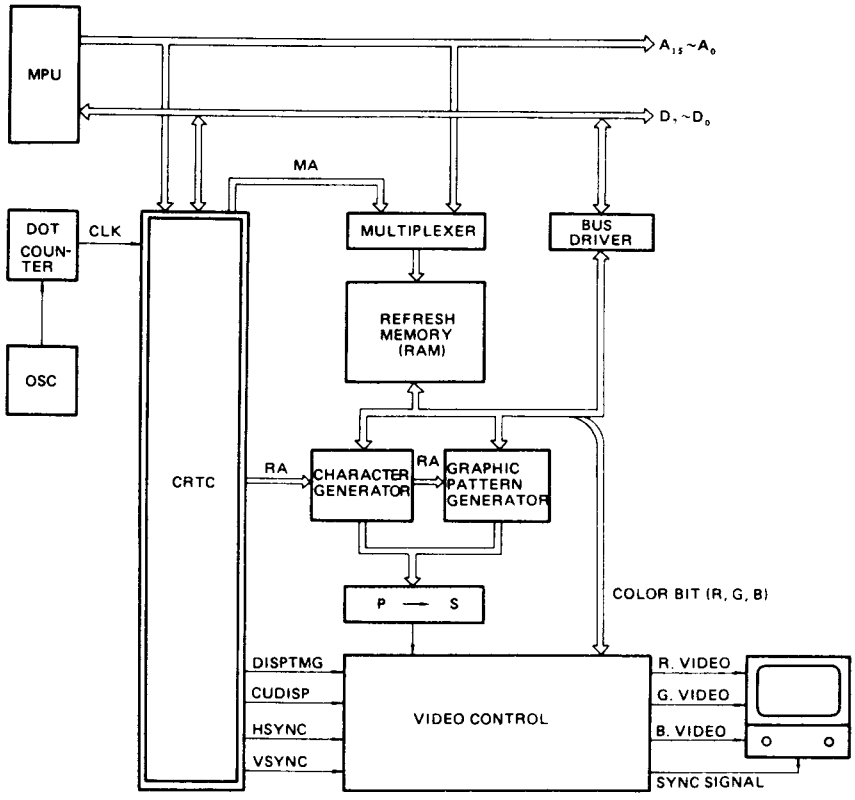


Figure 34 Color Limited Graphic Display

- **Monochrome Full Graphic Display**

Fig. 35 shows a system of monochrome full graphic display. While simple graphic display is figure display by combination of picture elements in unit of 1 picture elements, full graphic display is display of any figures in unit of 1 dot. In this case, refresh memory is dot memory that stores all the dot patterns, so its output is directly provided to parallel-serial converter to be displayed. Dot memory address to refresh the screen is set up by combination of MA and RA of CRTC.

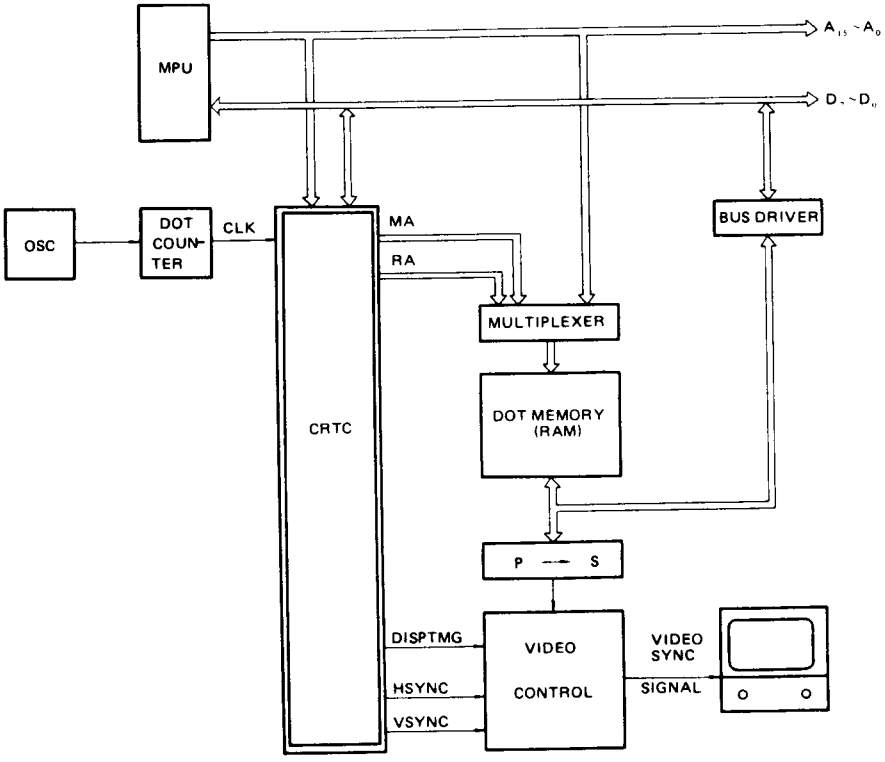


Figure 35 Monochrome Full Graphic Display

Fig. 36 shows an example of access to refresh memory by combination of MA and RA. Fig. 36 shows a refresh memory address method for full graphic display. Correspondence between dot on the CRT screen and refresh memory address is shown in Fig. 37.

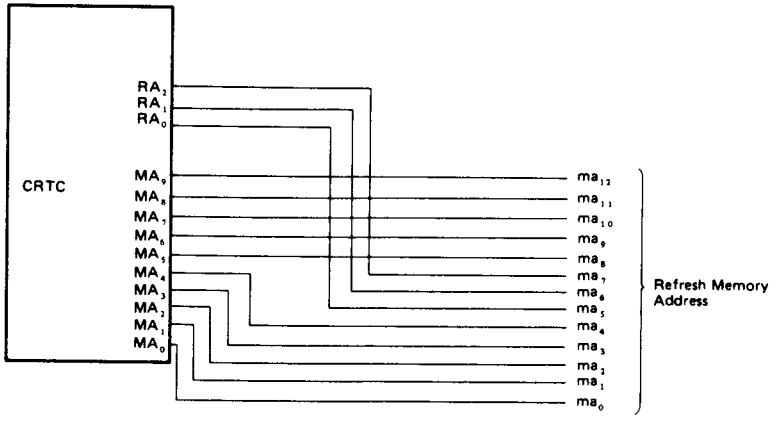


Figure 36 Refresh Memory Address Method for Full Graphic Display

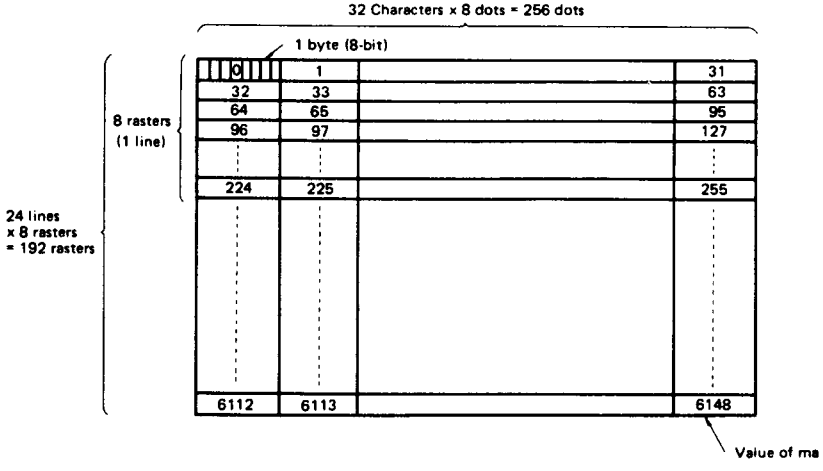


Figure 37 Memory Address and Dot Display Position on the Screen for Full Graphic Display

• Color Full Graphic Display

Fig. 38 shows a system of color full graphic display by 7-color display. Refresh memory is composed of three dot memories which are respectively used for red, green, and blue. These dot memories are read out in parallel at one time and their output is provided to three parallel-serial converters. Then video control circuit adds the blanking control to output of these converters and provides it to CRT display device as red, green, and blue video signals with sync signals.

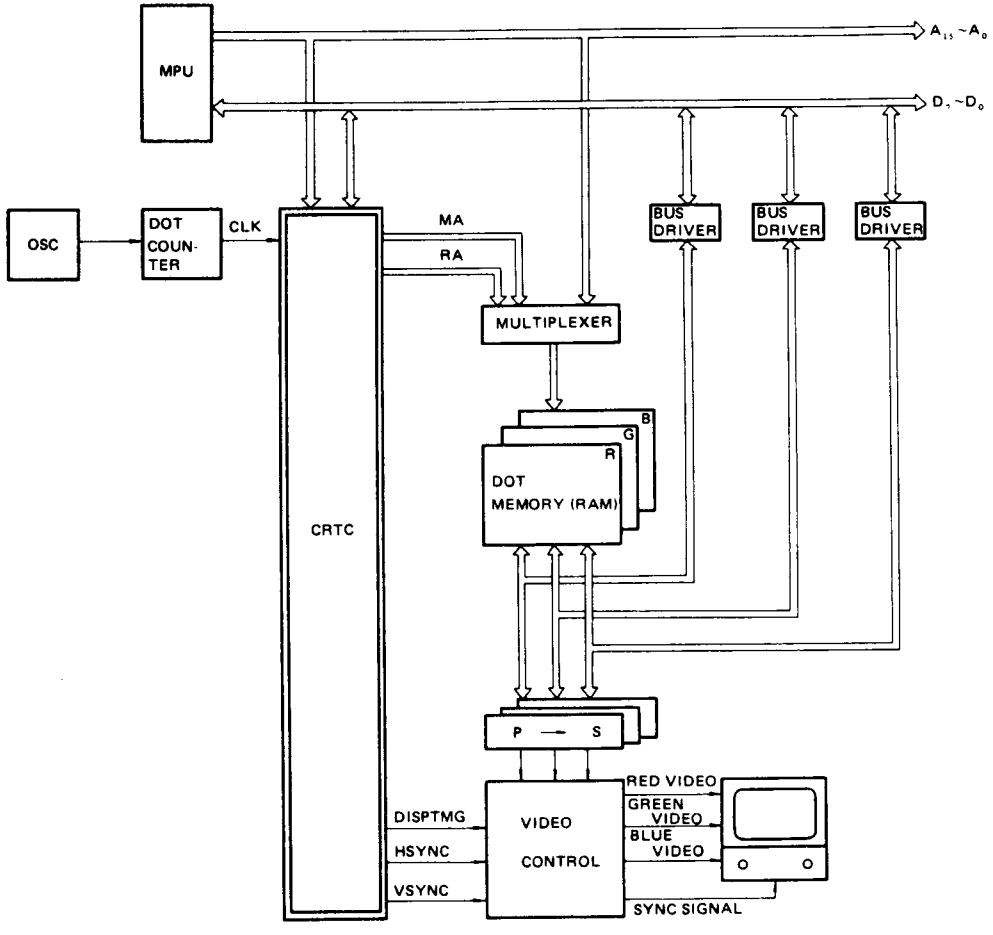


Figure 38 Color Full Graphic Display

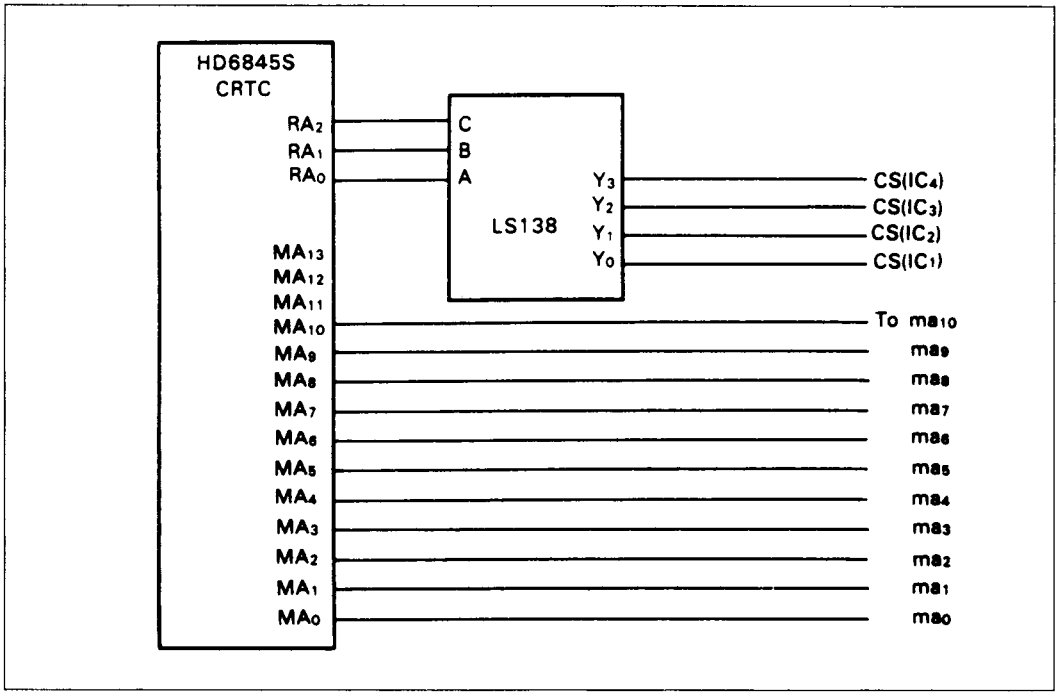


Figure 38-A Refresh Memory Address Method for Full Graphic Display

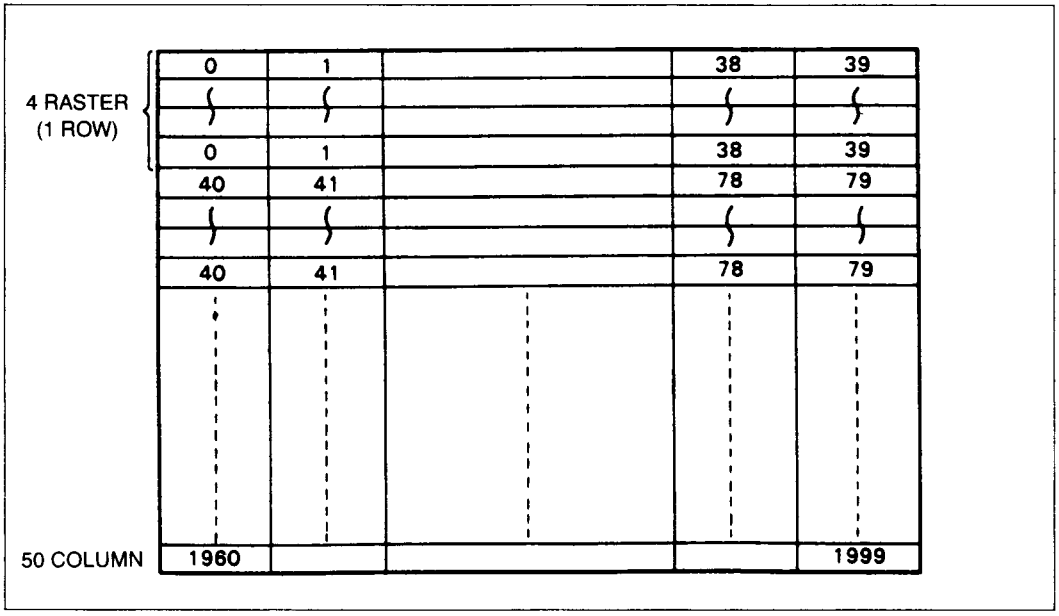


Figure 38-B Memory Address and Dot Display Position on the Screen for Full Graphic Display

- **Cluster Control of CRT Display**

The CRTC enables cluster control that is to control CRT display of plural devices by one CRTC. Fig. 39 shows a system of cluster control. Each display control unit has refresh memory, character generator, parallel-serial converter, and video control circuit separately, but these are controlled together by the CRTC.

In this system, it is possible for plural CRT display devices to have their own display separately.

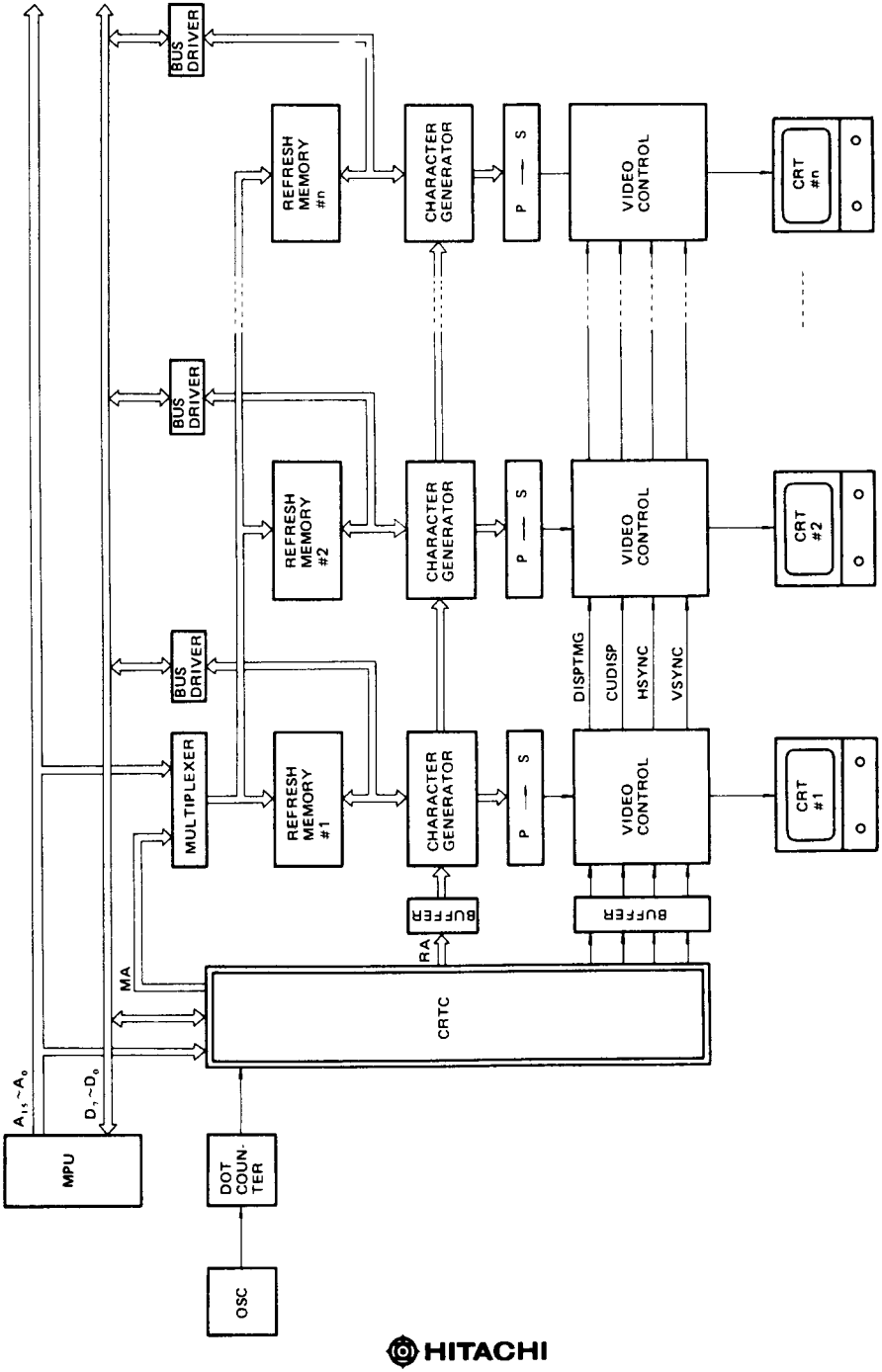


Figure 39 Cluster Control by the CRTC

■ EXAMPLES OF APPLIED CIRCUIT OF THE CRTC

Fig. 41 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table 12. Moreover, specification of CRT display unit is shown in Table 13 and initializing values for the CRTC are shown in Table 14.

Table 12 Specification of Applied Circuit

Item	Specification
Character Format	5 × 7 Dot
Character Space	Horizontal : 3 Dot Vertical : 5 Dot
One Character Time	1 μs
Number of Displayed Characters	40 characters × 16 lines = 640 characters
Access Method to Refresh Memory	Snychronous Method (DISPTMG Read)
Refresh Memory	640 B
Address Map	2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} Refresh Memory: 0 0 0 0 0 0 * * * * * * * * * * CRTC Address Register: 0 0 0 1 0 0 × × × × × × × × × 0 CRTC Control Register: 0 0 0 1 0 0 × × × × × × × × × 1 × · · · don't care, * · · · 0 or 1
Synchronization Method	HVSYNC Method

Table 13 Specification of Character Display

Item	Specification
Scan Mode	Non-interlace
Horizontal Deflection Frequency	15.625 kHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal × Vertical)	8 × 12 (Character Font 5 × 7)
Number of Displayed Characters (Row × Line)	40 × 16
HSYNC Width	4 μs
VSYNC Width	3 H
Cursor Display	Raster 9 ~ 10, Blink 16 Field Period
Paging, Scrolling	Not used

Table 14 Initializing Values for Character Display

Register	Name	Symbol	Initializing Value Hex (Decimal)	
R0	Horizontal Total	Nht	3F	(63)
R1	Horizontal Displayed	Nhd	28	(40)
R2	Horizontal Sync Position	Nhsp	34	(52)
R3	Sync Width	Nvsw, Nhsw	34	
R4	Vertical Total	Nvt	14	(20)
R5	Vertical Total Adjust	Nadj	08	(8)
R6	Vertical Displayed	Nvd	10	(16)
R7	Vertical Sync Position	Nvsp	13	(19)
R8	Interlace & Skew		00	
R9	Maximum Raster Address	Nr	0B	(11)
R10	Cursor Start Raster	B, P, NCSTART	49	
R11	Cursor End Raster	NCEND	0A	(10)
R12	Start Address (H)		00	(0)
R13	Start Address (L)		00	(0)
R14	Cursor (H)		00	(0)
R15	Cursor (L)		00	(0)

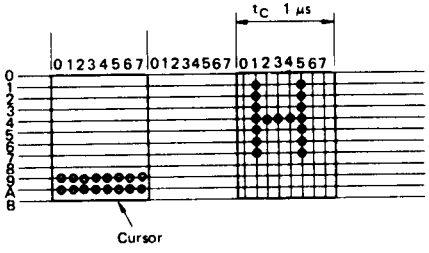


Figure 40 Non-interlace Display (Example)

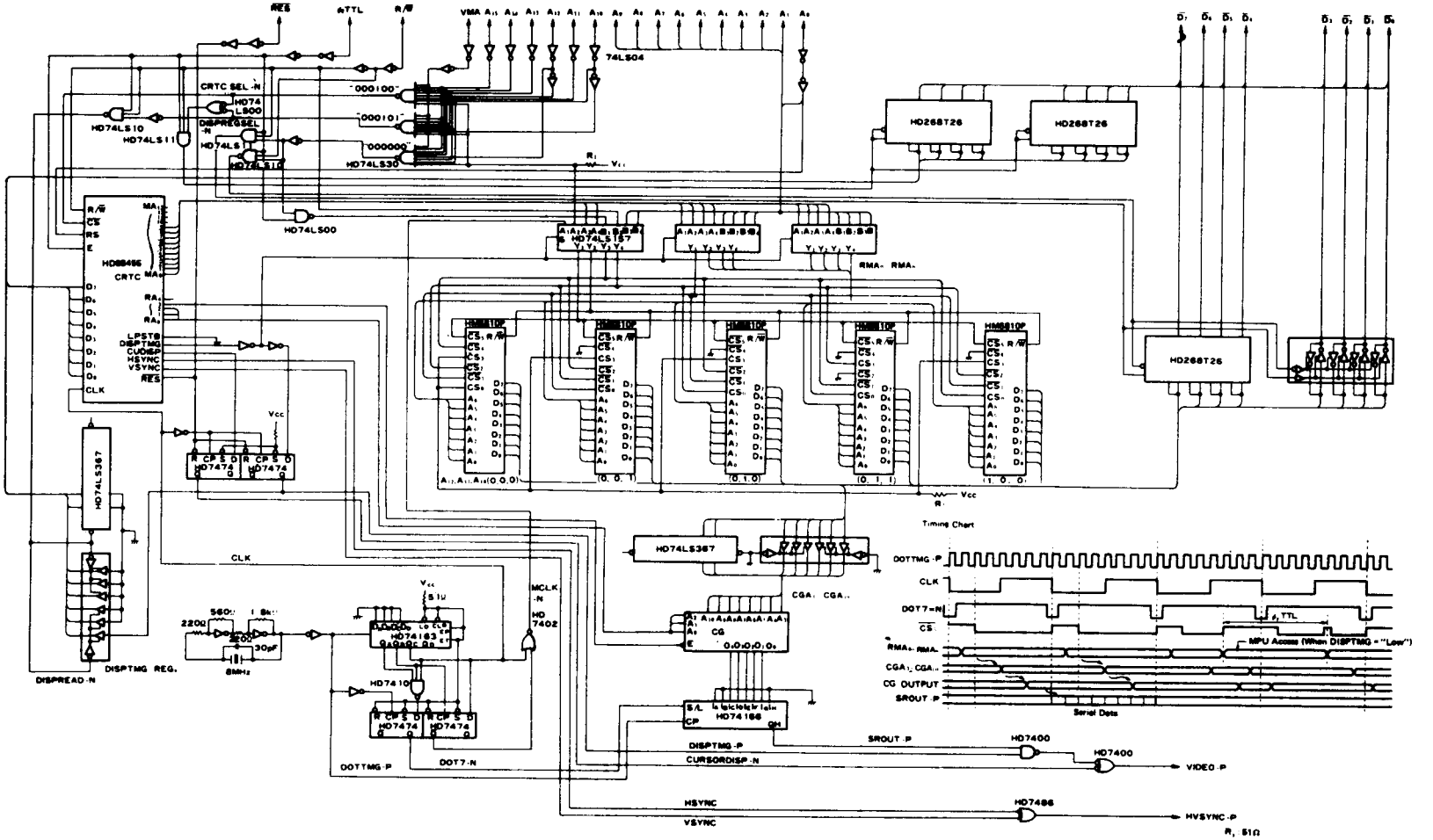


Figure 41 Example of Applied Circuit of the CRTC (Monochrome Character Display)

■ **DISPLAY SEQUENCE AFTER $\overline{RES}$ RELEASE OF HD6845S**

HD6845S starts the display operation immediately after the release of $\overline{RES}$. The operation at the first field is different from the normal subsequent display operation.

[Operation at the first field after the $\overline{RES}$ release]

(1) DISPTMG and CUDISP are not output. (They remain at "Low" level. The display is inhibited.)

(2) The data programmed in the start address register is not used. (MA and RA start at "0".)

(3) The sequences are shown in the following figures.

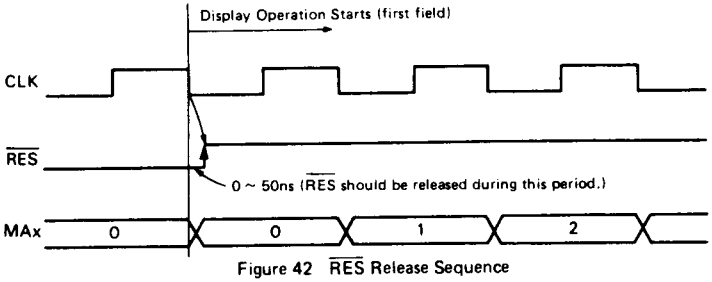


Figure 42 $\overline{RES}$ Release Sequence

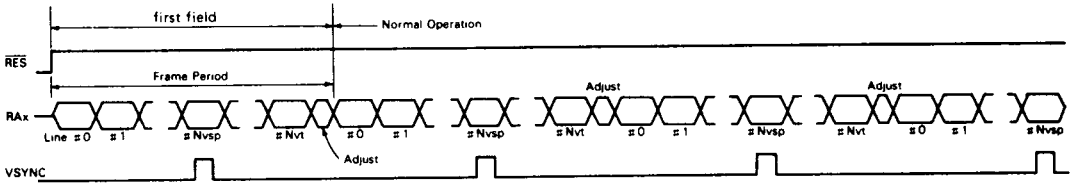
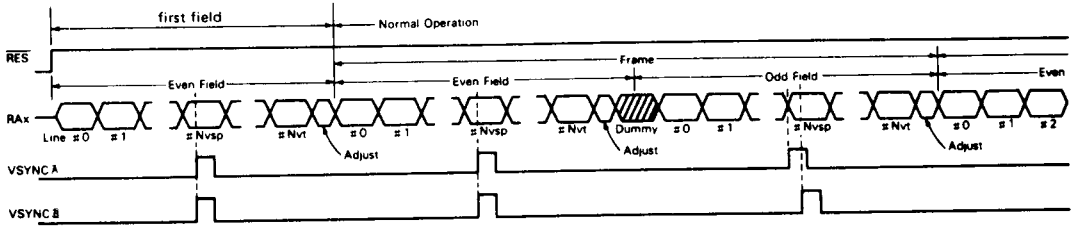
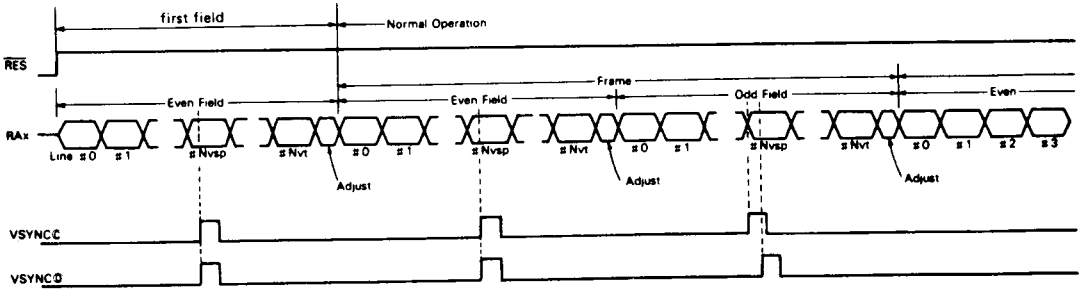


Figure 43 $\overline{RES}$ Release Sequence in The Non-interlace Mode



VSYNCⒶ : Interlace Sync Control
Interlace Sync & Video Control (Nr+2=Even)
Interlace Sync & Video Control (Nr+2=Odd, Nvt=Odd, Nvsp=Even)
VSYNCⒷ : Interlace Sync & Video Control (Nr+2=Odd, Nvt=Odd, Nvsp=Odd)

Figure 44 $\overline{RES}$ Release Sequence in The Interlace Mode (1)



VSYNCⒸ : Interlace Sync & Video Control (Nr+2=Odd, Nvt=Even, Nvsp=Even)
VSYNCⒹ : Interlace Sync & Video Control (Nr+2=Odd, Nvt=Even, Nvsp=Odd)

Figure 45 $\overline{RES}$ Release Sequence in The Interlace Mode (2)

■ ANOMALOUS OPERATIONS IN HD6845S CAUSED BY REWRITING REGISTERS DURING THE DISPLAY OPERATION*

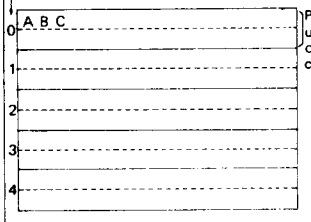
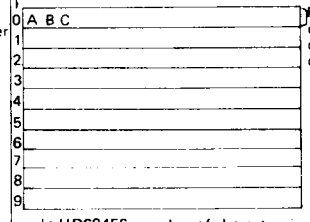
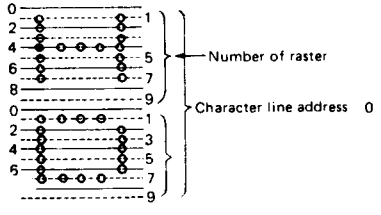
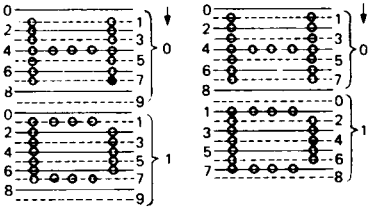
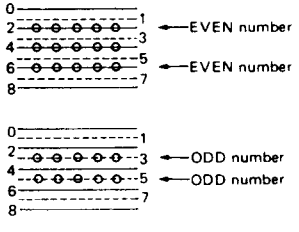
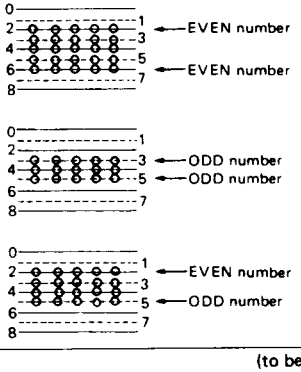
Register #	Register Name	Anomalous operations caused by rewriting registers & Conditions to avoid those operations	Rewriting** OK or NG
R0	Horizontal Total	The horizontal scan period is disturbed.	X
R1	Horizontal Displayed	There are some cases where the width of DISPTMG becomes shorter than the programmed value at the moment of a rewrite operation. An error operation occurs only during one raster period.	○
R2	Horizontal Sync Position	There are some cases where HSYNC is placed on the position different from the programmed value or the noise is output.	X
R3	Sync Width	When a rewrite operation is performed at a "High" level on HSYNC pulse or VSYNC pulse, there are some cases where the width pulse becomes shorter than the programmed value at the moment of a rewrite operation.	Δ
R4	Vertical Total	When a rewrite operation is performed during the last raster period in the line, there is a possibility that the disturbance occurs during the vertical scan period. There is no problem of a rewrite operation during raster period except this period.	Δ
R5	Vertical Total Adjust	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the numbers of Adjust Raster, specified by program, are not added. (Only during the adjust raster period)	Δ
R6	Vertical Displayed	After the moment of a rewrite operation, there are some cases where the Display is inhibited. However, the display according to the programmed value is performed from the next field.	○
R7	Vertical Sync Position	There are some cases where VSYNC is placed on the position different from the programmed value or the noise is output.	X
R8	Interlace & Skew	Neither scan mode bit nor skew bit is rewritten dynamically. Dynamic Rewrite into scan mode bit and skew bit is prohibited.	X
R9	Maximum Raster Address	The internal operation will be disordered by a rewrite operation.	X
R10	Cursor Start Raster	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the jitter occurs on the cursor raster or the cursor is not displayed correctly. There is also a possibility that the blink rate becomes temporally shorter than usual.	Δ
R11	Cursor End Raster	When a rewrite operation is performed in the last character time of the raster period, there are some cases where the jitter occurs on the cursor raster or the cursor is not displayed correctly. Moreover, there are also some cases where the blink rate becomes temporally shorter than normal operation.	Δ
R12	Start Address (H)	R12 and R13 are used in the last raster period of the field. A rewrite operation can be performed except during this period. However, when R12 and R13 are rewritten in each field separately, the display operation, whose start address is determined temporally by programming sequence, will be performed. A rewrite operation should be performed during the horizontal/vertical display period.	○
R13	Start Address (L)		○
R14	Cursor (H)	When a rewrite operation is performed during the display period, there are some cases where the cursor is temporally displayed at the address different from the programmed value. A rewrite operation should be performed during the horizontal/vertical retrace period. Also, when R14 and R15 are rewritten in each field separately, the cursor is displayed temporally at the temporal address determined by programming sequence.	○
R15	Cursor (L)		○

* . . . . . means temporary abnormal operations in rewriting the internal register during the display operation. Normally, after a rewrite operation, the LSI performs the specified display operation from the next field.
(The operations in this table are outside our guarantee and are regarded as materials for reference.)

** ○ . . . . . A rewrite operation is possible without affecting the screen in the display so much.
Δ . . . . . If conditions are satisfied, a rewrite operation is possible. If conditions are not satisfied, there are some cases where a flicker and so on occur temporally.
X . . . . . When a rewrite operation is performed, there are some cases where a flicker and so on occur temporally.

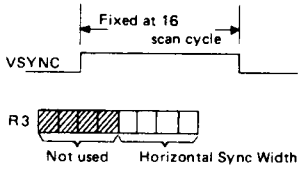
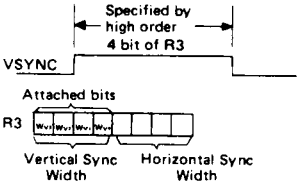
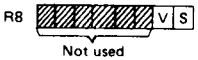
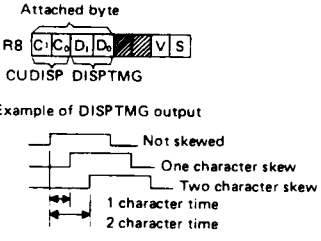
■ COMPARISON BETWEEN HD6845S AND HD6845R

• Comparison of function between HD6845S and HD6845R

No.	Functional Difference		HD6845R	HD6845S
1	Interlace Sync & Video Mode Display	Programming Method of Number of Vertical Characters	Character line address  In HD6845, number of characters is vertically programmed in unit of two lines, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 5	Character line address  In HD6845S, number of characters is vertically programmed in unit of one line, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 10
		Number of Rasters Per Character Line	Only even number can be specified.  Number of raster = 10 scan line (specified) However, number which is programmed into register is calculated at follows. Programmed number (Nr) = (Number specified) - 1	Both even number and odd number can be specified. Character line address  When number of raster per character line is EVEN. Number of raster = 10 scan line (specified) When number of raster per character line is ODD. Number of raster = 9 scan line (specified) However, number which is programmed into register is calculated as follows. Programmed number (Nr) = (Number specified) - 2
		Cursor Display	Cursor is displayed in either EVEN field or ODD field. 	Cursor is displayed in both EVEN field and ODD field. 

(to be continued)

2

No.	Functional Difference	HD6845R	HD6845S
2	Vertical Sync Pulse Width (VSYNC output)	Fixed at 16 raster scan cycle (16H) 	Programmable (1 ~ 16 raster scan cycle) 
3	SKEW Function	Not included 	SKEW function is newly included in DISPTMG, CUDISP signals. 
4	Start Address Register	Impossible to READ	Possible to READ
5	RESET Signal ($\overline{RES}$)	$MA_0 \sim MA_{13}$ Output, $RA_0 \sim RA_4$ Output ..... Synchronous reset Other Outputs ..... Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$, synchronizing with DLK "Low" level, go to "Low" level, after $\overline{RES}$ has gone to "Low" Other outputs go to "Low" immediately after $\overline{RES}$ has gone to "Low" level	$MA_0 \sim MA_{13}$ Output, $RA_0 \sim RA_4$ Output, Other Outputs ..... Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$ and others go to "Low" level immediately after $\overline{RES}$ has gone to "Low" level.

■ COMPATIBILITY OF HD6845S AND HD6845R

Non-interlace mode control
Interlace sync mode control
} Fully compatible with HD6845R* HD6845R can be directly replaced by HD6845S in these modes.

Interlace sync & Video mode control :
Not compatible with HD6845R in regard to programming and data for vertical direction need to be changed.

* The functions added to HD6845S utilize undefined bits of the Control Register in HD6845R. If "0" is programmed to the undefined bits in the initial set, it is possible to replace HD6845R with HD6845S without changing the parameters.

Note) The restriction on programming of HD6845S and HD6845R should be taken into consideration.