DDR SDRAM Data Sheet Addendum

MT46V128M4 – 32 Meg x 4 x 4 banks
MT46V64M8 – 16 Meg x 8 x 4 banks
MT48LC32M16 – 8 Meg x 16 x 4 banks

Features

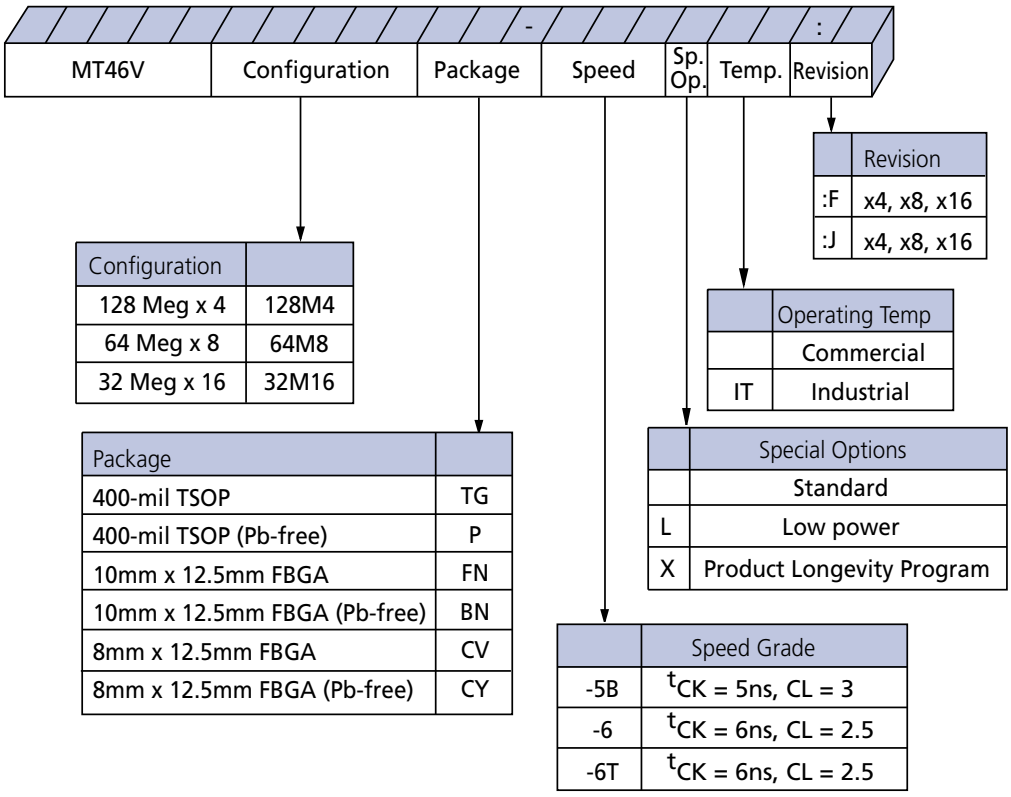
- V_{DD} = 2.5V ±0.2V, V_{DDQ} = 2.5V ±0.2V
  - V_{DD} = 2.6V ±0.1V, V_{DDQ} = 2.6V ±0.1V (DDR400)[1]
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh
  - 64ms, 8192-cycle
- Longer-lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL_2 compatible)
- Concurrent auto precharge option is supported
- ^{t}RAS lockout supported (^{t}RAP = ^{t}RCD)

Options	Marking
• Configuration	
– 128 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 64 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 32 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• Plastic package	
– 66-pin TSOP	TG
– 66-pin TSOP (Pb-free)	P
– 60-ball FBGA (10mm x 12.5mm)	FN[2]
– 60-ball FBGA (10mm x 12.5mm) (Pb-free)	BN[2]
– 60-ball FBGA (8mm x 12.5mm)	CV[3]
– 60-ball FBGA (8mm x 12.5mm) (Pb-free)	CY[3]
• Timing – cycle time	
– 5ns @ CL = 3 (DDR400)	-5B
– 6ns @ CL = 2.5 (DDR333) (FBGA only)	-6[2]
– 6ns @ CL = 2.5 (DDR333) (TSOP only)	-6T[2]
• Special Options	
– Product Longevity Program (PLP)	X
• Self refresh	
– Standard	None
– Low-power self refresh	L
• Temperature rating	
– Commercial (0°C to +70°C)	None
– Industrial (–40°C to +85°C)	IT
• Revision	
– x4, x8, x16	:F
– x4, x8, x16	:J

Notes:
1. DDR400 devices operating at < DDR333 conditions can use V_{DD}/V_{DDQ} = 2.5V +0.2V.
2. Only available on Revision F.
3. Only available on Revision J.

Figure 1: 512Mb DDR SDRAM Part Numbers

Example Part Number: MT46V32M16P-6T:F



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Revision History

Rev. C – 03/14

- Changed MPN from "MT48LC**16M16**A2" to "MT48LC**64M8**"

Rev. B – 03/14

- Changed "Premium Lifecycle Product" to "Product Longevity Program"

Rev. A – 11/13

- Initial release based on the 512Mb x4, x8, x16 DDR SDRAM, Rev. Q 07/11 data sheet

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.