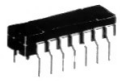
MC660 Series (−30 to +75°C)



L SUFFIX
CERAMIC PACKAGE
CASE 605C
TO-116

P SUFFIX
PLASTIC PACKAGE
CASE 605
(Formerly Case 93)
TO-116

MHTL integrated circuits are especially designed to meet the requirements of industrial applications. Because of the outstanding noise immunity. MHTL circuits provide error-free operation in high noise environments far beyond the tolerance of other integrated circuit families. Multifunction packages and broad operating temperature range further tailor this device family to the industrial designer's requirements.

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 15 V ±1.0 Vdc, T_A = 25°C)

Function	Type ③ Case 605C, 605 −30 to +75°C	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Power Dissipation mW typ/pkg
Expandable Dual 4-Input Gate (active pullup)	MC600L,P	10	110	88/26 ①
Expandable Dual 4-Input Gate (passive pullup)	MC661L,P	10	125	88/26 ①
Expandable Dual 4-Input Line Driver	MC662L,P	10	140	180/26 ①
Dual J-K Flip-Flop	MC663L,P	10	3.0 MHz ②	200
Master-Slave R-S Flip-Flop	MC664L,P	10	3.0 MHz ②	160
Triple Level Translator	MC665L,P	MDTL = 8 MTTL III = 5.5 MRTL = 5	40	83(DTL) 104(RTL)
Triple Level Translator	MC666L,P	10	75	105
Dual Monostable Multivibrator	MC667L,P	10	140	240
Quad 2-Input Gate (passive pullup)	MC668L,P	10	125	176/52 ①
Dual 4-Input Expander	MC669L,P	–	–	–
Triple 3-Input Gate (passive pullup)	MC670L,P	10	125	132/39 ①
Triple 3-Input Gate (active pullup)	MC671L,P	10	110	132/39 ①
Quad 2-Input Gate (active pullup)	MC672L,P	10	110	176/52 ①
Dual 2-Input AND-OR-INVERT Gate	MC673L,P	10	110	160/50 ①
Dual 2-Input AND-OR-INVERT Gate	MC674L,P	10	125	160/50 ①

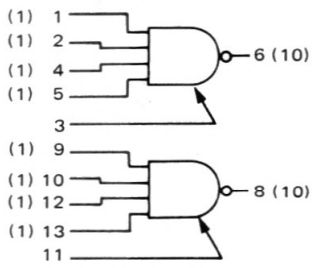
① Inputs High/Input Low ② f_{Tog} ③ L suffix denotes Ceramic Package, P suffix denotes Plastic Package.

MAXIMUM RATINGS (T_A = 25°C)

Rating		Symbol	Value	Unit
Power Supply Voltage	Continuous Pulsed, < 1.0 s	V_{CC}	18 20	Vdc
Input Voltage	MC665 MC666 DTL RTL MC669 All Others	V_{in}	−1.0 to +18 −1 to +6 −4 to +4 −1.0 to +18 −1.0 to +18	Vdc
Output Current (into outputs)	MC662 MC663 MC664 MC669 All Others	–	60 28 26 – 30	mAdc
Input Reverse Current @ 18 V		I_R	0.5	mAdc
Forward Current (Individual) MC669		I_F	30	mAdc
Operating Temperature Range		T_A	−30 to +75	°C
Storage Temperature Range		T_{stg}	−55 to +125	°C

GATES

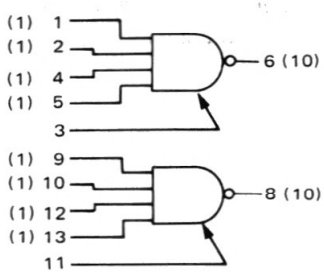
MC660
Expandable
Dual 4-Input NAND Gate
(active output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 110 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

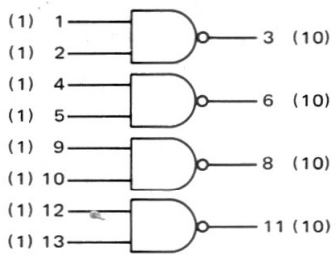
MC661
Expandable
Dual 4-Input NAND Gate
(passive output pullup)



$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 125 ns typ
P_D = 88 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

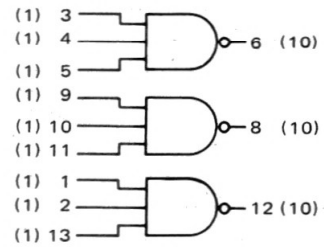
MC668
Quad 2-Input NAND Gate
(passive output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 125 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

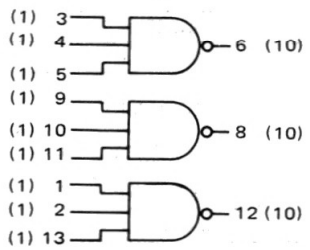
MC670
Triple 3-Input NAND Gate
(passive output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 125 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

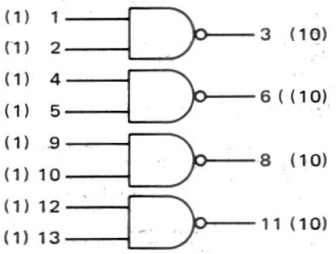
MC671
Triple 3-Input NAND Gate
(active output pullup)



$6 = \overline{3 \cdot 4 \cdot 5}$

t_{pd} = 110 ns typ
P_D = 132 mW typ/pkg (Inputs High)
39 mW typ/pkg (Input Low)

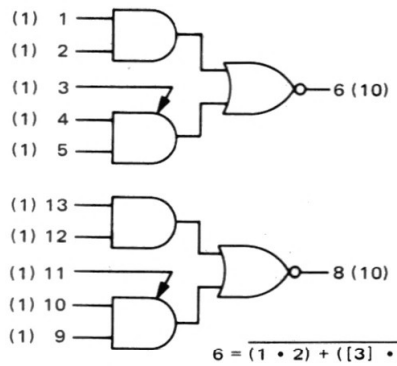
MC672
Quad 2-Input NAND Gate
(active output pullup)



$3 = \overline{1 \cdot 2}$

t_{pd} = 110 ns typ
P_D = 176 mW typ/pkg (Inputs High)
52 mW typ/pkg (Input Low)

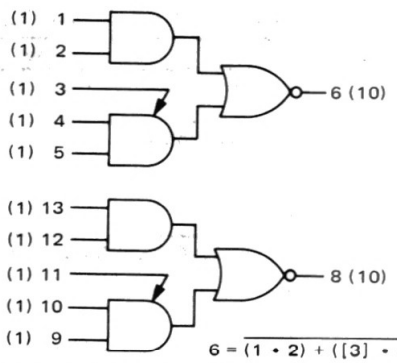
MC673
Expandable
Dual 2-Input AND-OR-INVERT Gate



$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

t_{pd} = 110 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

MC674
Expandable
Dual 2-Input AND-OR-INVERT Gate



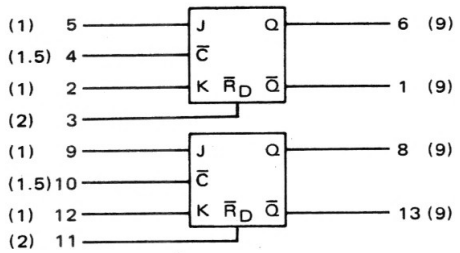
$6 = \overline{(1 \cdot 2) + ([3] \cdot 4 \cdot 5)}$

t_{pd} = 125 ns typ
P_D = 160 mW typ/pkg (Inputs High)
50 mW typ/pkg (Input Low)

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.
(V_{CC} = Pin 14, Gnd = Pin 7)

FLIP-FLOPS

MC663
Dual J-K Flip-Flop



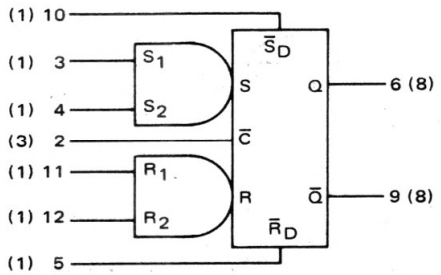
f_{Tog} = 3.0 MHz typ
P_D = 200 mW typ/pkg

TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	$\bar{Q}$
0	0	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
1	1	$\bar{Q}_n$	Q_n

Direct input ($\bar{R}_D$) must be high.
0 = low state
1 = high state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n
NOTE: A low state "0" at the direct reset $\bar{R}_D$ causes a low state "0" at the Q output and the complement at the $\bar{Q}$ output.

MC664
Master-Slave R-S Flip-Flop



f_{Tog} = 3.0 MHz typ
P_D = 160 mW typ/pkg

DIRECT INPUT OPERATION

$\bar{R}_D$	$\bar{S}_D$	Q	$\bar{Q}$
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	NA	NA

$\bar{C}$ must be Low
0 = low state
1 = high state
NC = No change
NA = Not allowed

CLOCKED OPERATION

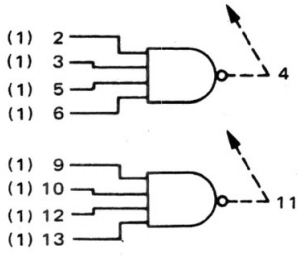
t_n				t_{n+1}
S_1	S_2	R_1	R_2	Q
0	X	0	X	Q_n
0	X	X	0	Q_n
X	0	0	X	Q_n
X	0	X	0	Q_n
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	U

Direct inputs ($\bar{R}_D$, $\bar{S}_D$) must be hign.

X = state of input does not affect state of the circuit
U = indeterminate state
t_n = time period prior to negative transition of clock pulse
t_{n+1} = time period subsequent to negative transition of clock pulse
Q_n = state of Q output in time period t_n

EXPANDER

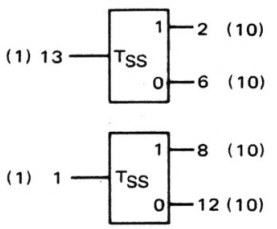
MC669
Dual 4-Input Expander



$4 = \overline{2 \cdot 3 \cdot 5 \cdot 6}$

MULTIVIBRATOR

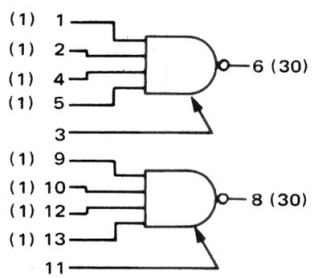
MC667
Dual Monostable Multivibrator



t_{pd} = 140 ns typ
P_D = 240 mW typ/pkg

DRIVER

MC662
Expandable
Dual 4-Input Line Driver
(active output pullup)



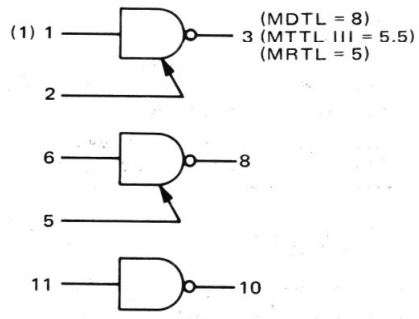
$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5 \cdot [3]}$

t_{pd} = 140 ns typ
P_D = 180 mW typ/pkg (Inputs High)
26 mW typ/pkg (Input Low)

MHTL LOGIC DIAGRAMS

TRANSLATORS

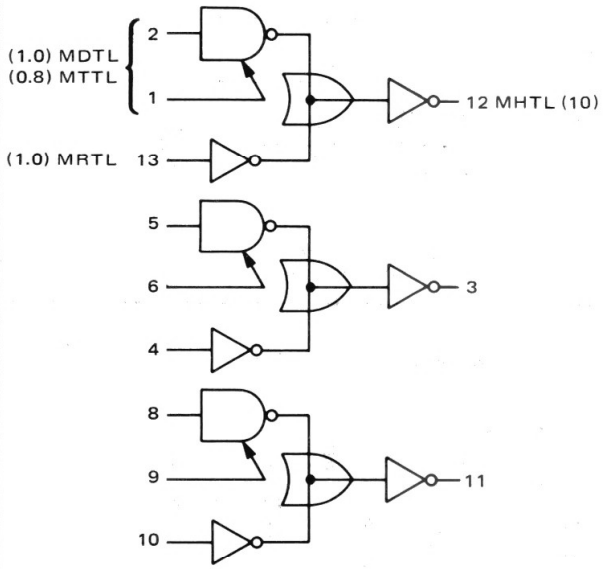
MC665
Triple Level Translator



$3 = \overline{1 \cdot [2]}$

t_{pd} = 40 ns typ
P_D = 83 mW typ/pkg (DTL)
104 mW typ/pkg (RTL)

MC666
Triple Level Translator



$12 = 2 \cdot [1] + 13$

t_{pd} = 75 ns typ
P_D = 105 mW typ/pkg