



Hi3536C H.265 CODEC Processor

Brief Data Sheet

Issue 01

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Hi3536C H.265 CODEC Processor

Key Specifications

Processor Core

- ARM Cortex A7 dual-core

Video Encoding/Decoding Protocols

- H.265/H.264/JPEG encoding and decoding

Video Encoding/Decoding

- 4x 1080p@30 fps H.265/H.264 decoding
- 8x 720p@30 fps H.265/H.264 decoding
- 16x D1@30 fps H.265/H.264 decoding
- 1x 1080p@30 fps H.265/H.264 encoding

Video and Graphics Processing

- Efficiently optimize and improve the image quality in various scenes by integrating HiSilicon's most advanced image processing engine.

Audio Encoding/Decoding

- ADPCM, G.711, and G.726 hardware audio encoding
- Software audio encoding and decoding complying with multiple protocols

Security Engine

- AES, DES, and 3DES algorithms implemented by hardware

Video Interfaces

- Support HDMI/VGA/CVBS output with high resolution up to 3840 x 2160

Audio Interfaces

- Support I²S/PCM interfaces

Ethernet Ports

- Two gigabit Ethernet ports

Peripheral Interfaces

- Support SATA 3.0 /USB 2.0 interfaces

Memory Interfaces

- DDR3 SDRAM
- Support SPI NOR/NAND flash
- Embedded 4 KB BOOTROM and 16 KB SRAM

RTC with an Independent Power Supply

- Independent battery for supplying power to the RTC

Functional Block Diagram

