



**Absolute Maximum Ratings** <sup>(1)</sup>

Supply Voltage ( $V^+ - V^-$ )	$\pm 18V$ or $36V$
Power Dissipation <sup>(2)</sup>	500 mW
Reference Input Differential Voltage (V14 to V15)	$V^-$ to $V^+$
Reference Input Common-Mode Range (V14, V15)	$V^-$ to $V^+$
Reference Input Current	5 mA
Logic Inputs	$V^-$ to $V^-$ plus $36V$
Analog Current Outputs ( $V_{S-} = -15V$ )	4.25 mA
ESD Susceptibility <sup>(3)</sup>	TBD V
Storage Temperature	$-65^\circ C$ to $+150^\circ C$
Lead Temp. (Soldering, 10 seconds)	
PDIP Package (plastic)	$260^\circ C$
CDIP Package (ceramic)	$300^\circ C$
Surface Mount Package	
Vapor Phase (60 seconds)	$215^\circ C$
Infrared (15 seconds)	$220^\circ C$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) The maximum junction temperature of the DAC0800 and DAC0802 is  $125^\circ C$ . For operating at elevated temperatures, devices in the CDIP package must be derated based on a thermal resistance of  $100^\circ C/W$ , junction-to-ambient,  $175^\circ C/W$  for the molded PDIP package and  $100^\circ C/W$  for the SOIC package.
- (3) Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

**Operating Conditions** <sup>(1)</sup>

	Min	Max	Units
Temperature ( $T_A$ )			
DAC0800L	$-55$	$+125$	$^\circ C$
DAC0800LC	0	$+70$	$^\circ C$
DAC0802LC	0	$+70$	$^\circ C$
$V^+$	$(V^-) + 10$	$(V^-) + 30$	V
$V^-$	$-15$	$-5$	V
$I_{REF}$ ( $V^- = -5V$ )	1	2	mA
$I_{REF}$ ( $V^- = -15V$ )	1	4	mA

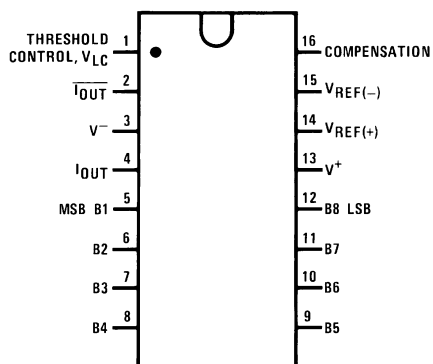
- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

## Electrical Characteristics

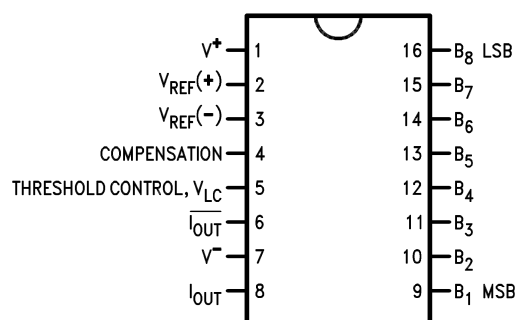
The following specifications apply for  $V_S = \pm 15V$ ,  $I_{REF} = 2\text{ mA}$  and  $T_{MIN} \leq T_A \leq T_{MAX}$  unless otherwise specified. Output characteristics refer to both  $I_{OUT}$  and  $\bar{I}_{OUT}$ .

Parameter		Test Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				$\pm 0.1$			$\pm 0.19$	%FS
$t_s$	Settling Time	To $\pm \frac{1}{2}$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ\text{C}$		100	135				ns
		DAC0800L					100	135	ns
		DAC0800LC					100	150	ns
$t_{PLH}$ , $t_{PHL}$	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ\text{C}$		35 35	60 60		35 35	60 60	ns ns
$TC_{IFS}$	Full Scale Tempco			$\pm 10$	$\pm 50$		$\pm 10$	$\pm 50$	ppm/ $^\circ\text{C}$
$V_{OC}$	Output Voltage Compliance	Full Scale Current Change $< \frac{1}{2}$ LSB, $R_{OUT} > 20\text{ M}\Omega$ , Typical	-10		18	-10		18	V
$I_{FS4}$	Full Scale Current	$V_{REF} = 10.000V$ , $R_{14} = R_{15} = 5.000\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$	1.984	1.992	2.00	1.94	1.99	2.04	mA
$I_{FSS}$	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		$\pm 0.5$	$\pm 4.0$		$\pm 1$	$\pm 8.0$	$\mu\text{A}$
$I_{ZS}$	Zero Scale Current			0.1	1.0		0.2	2.0	$\mu\text{A}$
$I_{FSR}$	Output Current Range	$V^- = -5V$ $V^- = -8V$ to $-18V$	0 0	2.0 2.0	2.1 4.2	0 0	2.0 2.0	2.1 4.2	mA
$V_{IL}$ $V_{IH}$	Logic Input Levels Logic "0" Logic "1"	$V_{LC} = 0V$			0.8			0.8	V V
$I_{IL}$ $I_{IH}$	Logic Input Current Logic "0" Logic "1"	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$ $2V \leq V_{IN} \leq +18V$		-2.0 0.002	-10 10		-2.0 0.002	-10 10	$\mu\text{A}$ $\mu\text{A}$
$V_{IS}$	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	V
$V_{THR}$	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	V
$I_{15}$	Reference Bias Current			-1.0	-3.0		-1.0	-3.0	$\mu\text{A}$
$dI/dt$	Reference Input Slew Rate	(Figure 26)	4.0	8.0		4.0	8.0		mA/ $\mu\text{s}$
$PSSI_{FS+}$	Positive Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSSI_{FS-}$	Negative Power Supply Sensitivity	$-4.5V \leq V^- \leq 18V$ , $I_{REF} = 1\text{ mA}$		0.0001	0.01		0.0001	0.01	%/%
$I^+$ $I^-$	Power Supply Current	$V_S = \pm 5V$ , $I_{REF} = 1\text{ mA}$		2.3 -4.3	3.8 -5.8		2.3 -4.3	3.8 -5.8	mA mA
$I^+$ $I^-$				2.4 -6.4	3.8 -7.8		2.4 -6.4	3.8 -7.8	mA mA
$I^+$ $I^-$	Power Supply Current	$V_S = +5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$		2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	mA mA
$I^+$ $I^-$				2.5 -6.5	3.8 -7.8		2.5 -6.5	3.8 -7.8	mA mA
$P_D$	Power Consumption	$\pm 5V$ , $I_{REF} = 1\text{ mA}$		33	48		33	48	mW
		$+5V$ , $-15V$ , $I_{REF} = 2\text{ mA}$		108	136		108	136	mW
		$\pm 15V$ , $I_{REF} = 2\text{ mA}$		135	174		135	174	mW

## Connection Diagrams

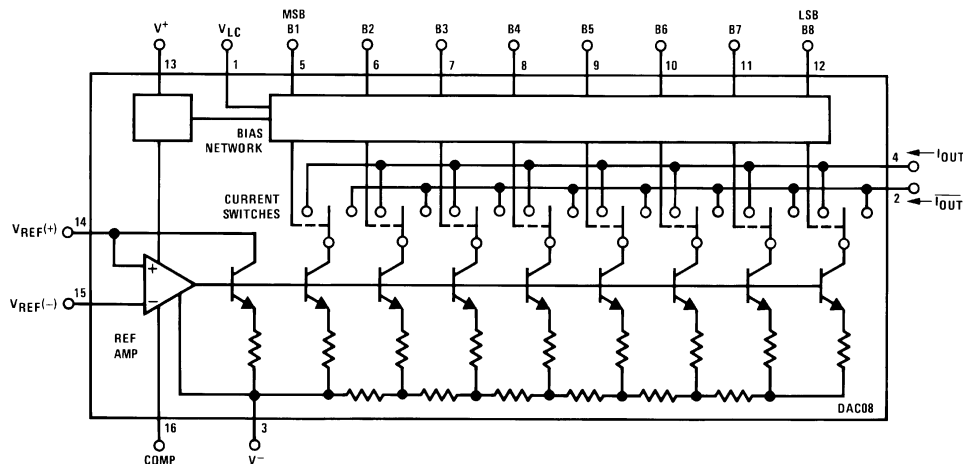


**Figure 2. PDIP, CDIP Packages - Top View**  
(See Package Number NFG0016E or NFE0016A)



**Figure 3. SOIC Package - Top View**  
(See Package Number D0016A)

## Block Diagram



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 4.**

## Typical Performance Characteristics

**Full Scale Current  
vs.  
Reference Current**

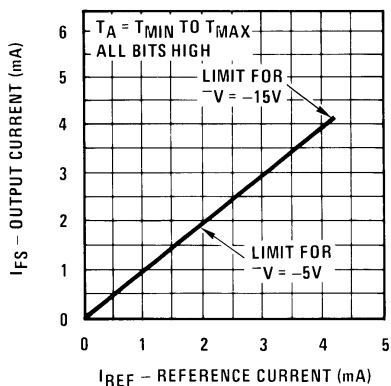


Figure 5.

**LSB Propagation Delay  
vs.  
I\_FS**

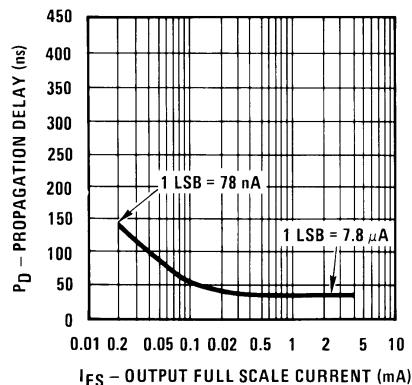
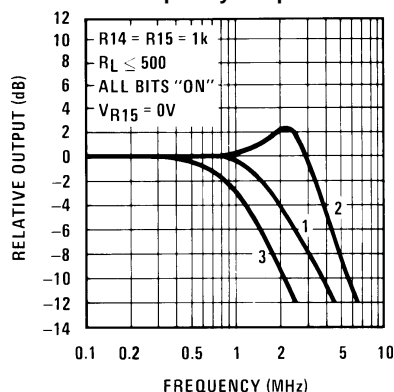


Figure 6.

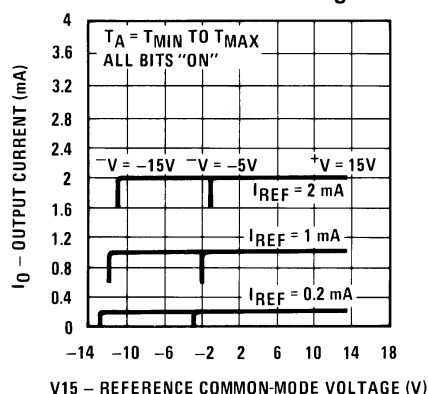
**Reference Input  
Frequency Response**



**Curve 1:**  $C_C=15$  pF,  $V_{IN}=2$  Vp-p centered at 1V.  
**Curve 2:**  $C_C=15$  pF,  $V_{IN}=50$  mVp-p centered at 200 mV.  
**Curve 3:**  $C_C=0$  pF,  $V_{IN}=100$  mVp-p centered at 0V and applied through  $50\Omega$  connected to pin 14.2V applied to R14.

Figure 7.

**Reference Amp  
Common-Mode Range**



Note. Positive common-mode range is always  $(V+) - 1.5V$ .

Figure 8.

**Logic Input Current vs.  
Input Voltage**

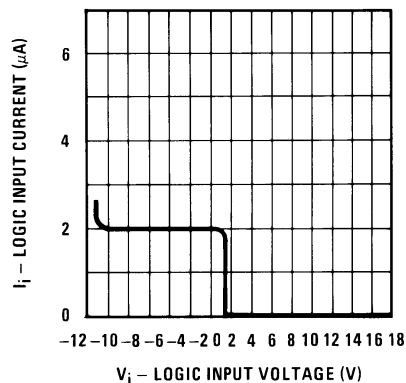


Figure 9.

**V\_TH - V\_LC  
vs.  
Temperature**

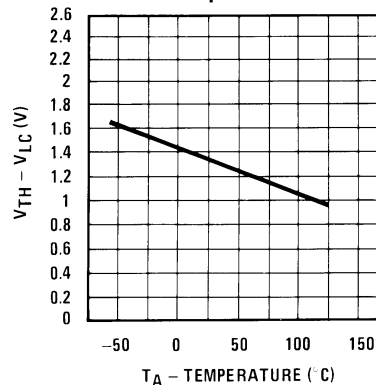


Figure 10.

## Typical Performance Characteristics (continued)

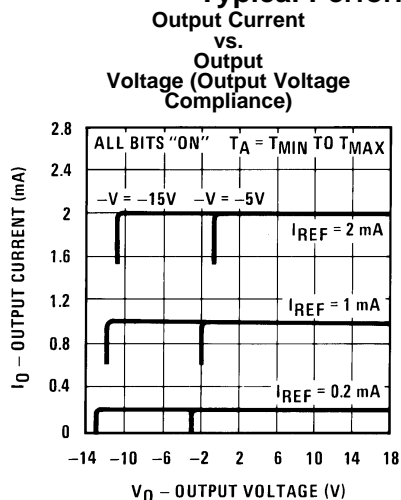


Figure 11.

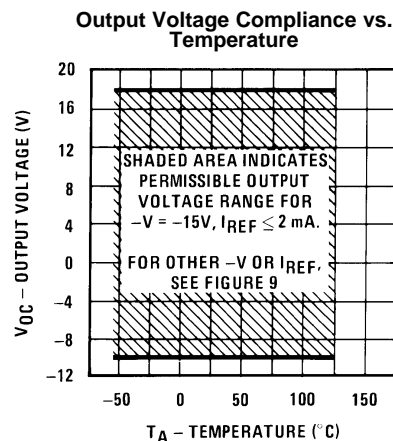
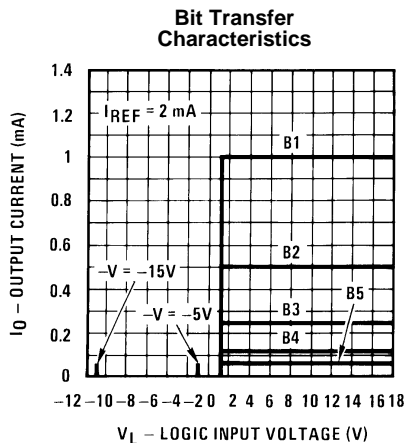


Figure 12.



Note. B1–B8 have identical transfer characteristics. Bits are fully switched with less than ½ LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2V over the operating temperature range ( $V_{LC} = 0V$ ).

Figure 13.

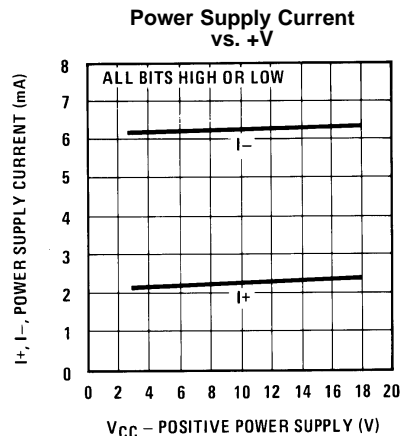


Figure 14.

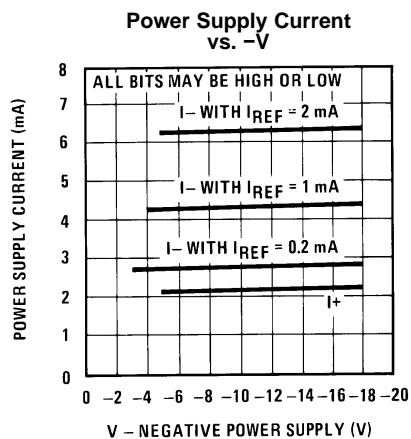


Figure 15.

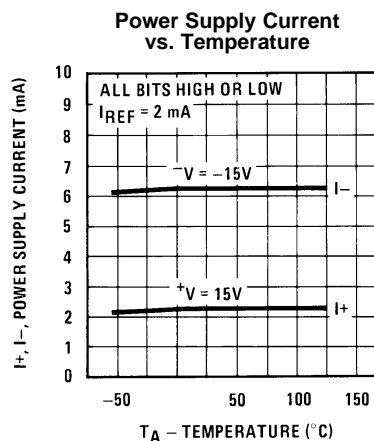
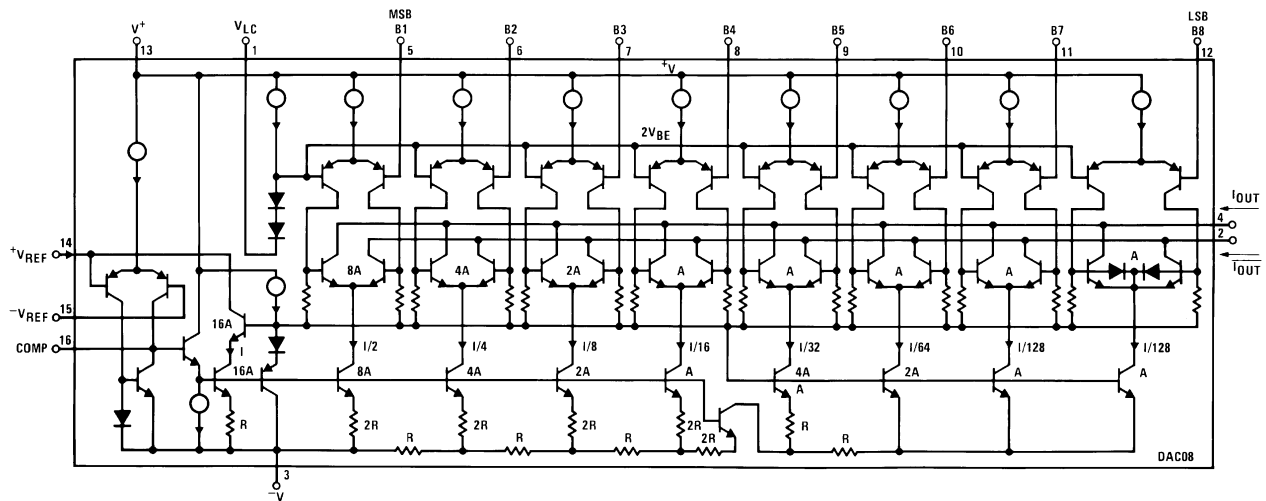


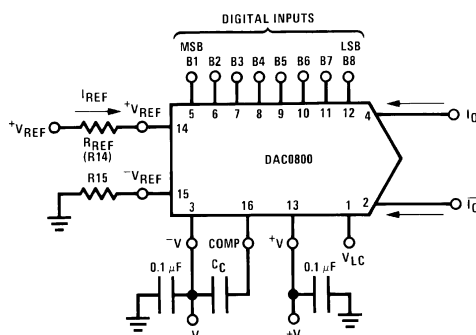
Figure 16.

## EQUIVALENT CIRCUIT



**Figure 17. Equivalent Circuit**

## TYPICAL APPLICATIONS



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

$$I_{FS} \approx \frac{+V_{REF}}{R_{REF}} \times \frac{255}{256}$$

$I_O + \bar{I}_O = I_{FS}$  for all logic states

For fixed reference, TTL operation, typical values are:

$V_{REF} = 10.000V$

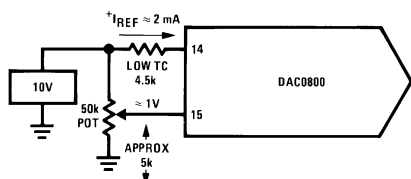
$R_{REF} = 5.000k$

$R15 \approx R_{REF}$

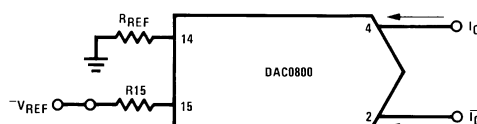
$C_C = 0.01 \mu F$

$V_{LC} = 0V$  (Ground)

**Figure 18. Basic Positive Reference Operation**



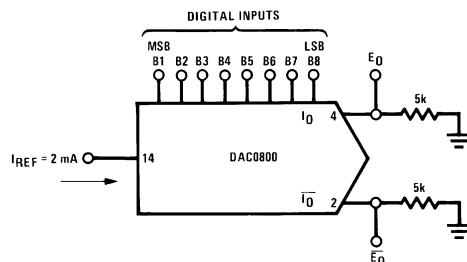
**Figure 19. Recommended Full Scale Adjustment Circuit**



**Figure 20. Basic Negative Reference Operation**

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.



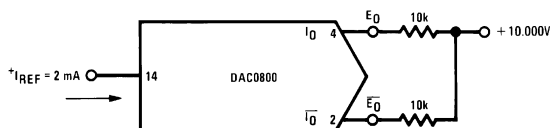


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 21. Basic Unipolar Negative Operation**

**Table 1. Basic Unipolar Negative Operation**

	B1	B2	B3	B4	B5	B6	B7	B8	$I_O$ mA	$\bar{I}_O$ mA	$E_O$	$\bar{E}_O$
Full Scale	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
Full Scale-LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
Half Scale+LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
Half Scale-LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
Zero Scale+LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

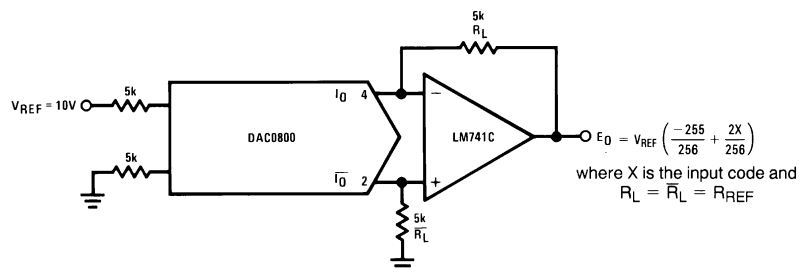


Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 22. Basic Bipolar Output Operation**

**Table 2. Basic Bipolar Output Operation**

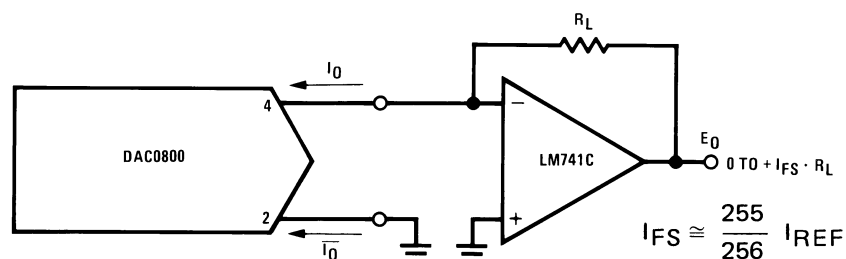
	B1	B2	B3	B4	B5	B6	B7	B8	$E_O$	$\bar{E}_O$
Pos. Full Scale	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale+LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale-LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg. Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920



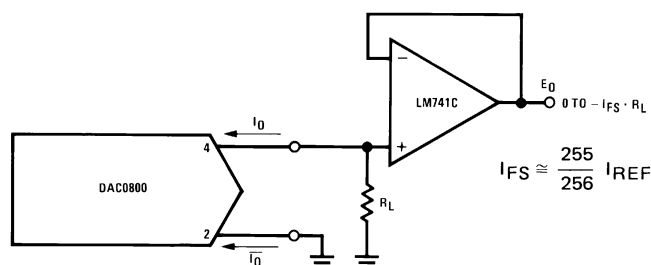
- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) If  $R_L = \bar{R}_L$  within  $\pm 0.05\%$ , output is symmetrical about ground.

**Figure 23. Symmetrical Offset Binary Operation****Table 3. Symmetrical Offset Binary Operation**

	B1	B2	B3	B4	B5	B6	B7	B8	EO
Pos. Full Scale	1	1	1	1	1	1	1	1	+9.960
Pos. Full Scale-LSB	1	1	1	1	1	1	1	0	+9.880
(+)Zero Scale	1	0	0	0	0	0	0	0	+0.040
(-)Zero Scale	0	1	1	1	1	1	1	1	-0.040
Neg. Full Scale+LSB	0	0	0	0	0	0	0	1	-9.880
Neg. Full Scale	0	0	0	0	0	0	0	0	-9.960

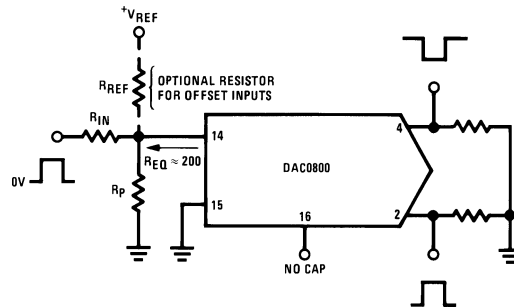


- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as negative logic DAC), connect inverting input of op amp to  $\bar{I}_O$  (pin 2), connect  $I_O$  (pin 4) to ground.

**Figure 24. Positive Low Impedance Output Operation**

- (1) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.
- (2) For complementary output (operation as a negative logic DAC) connect non-inverting input of op am to  $\bar{I}_O$  (pin 2); connect  $I_O$  (pin 4) to ground.

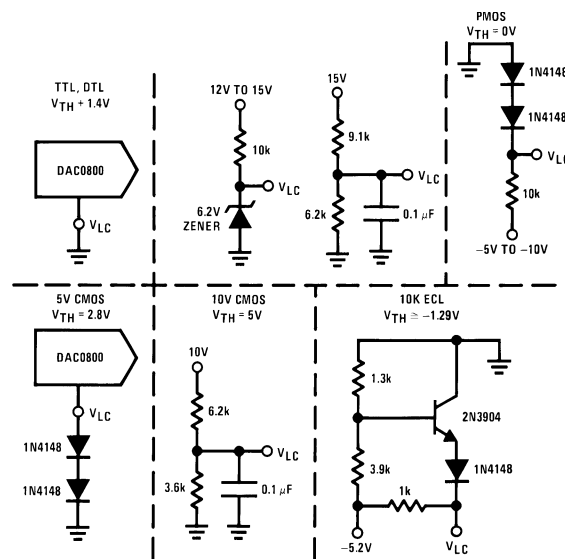
**Figure 25. Negative Low Impedance Output Operation**



Typical values:  $R_{IN}=5k, +V_{IN}=10V$

Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

### Figure 26. Pulsed Reference Operation



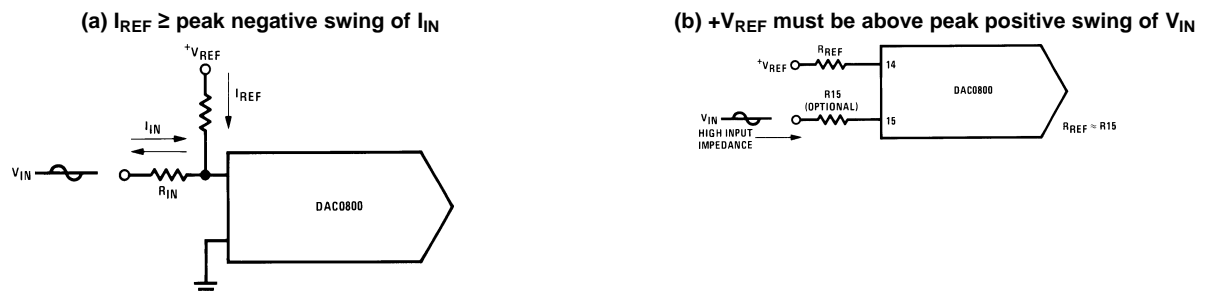
$$V_{TH} = V_{LC} + 1.4V$$

15V CMOS, HTL, HN1L

$$V_{TH} = 7.6V$$

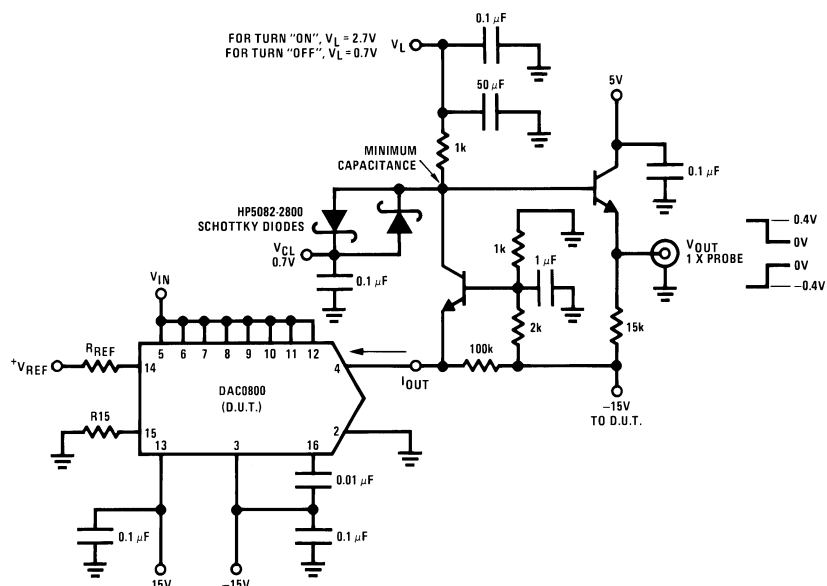
Note. Do not exceed negative logic input range of DAC.

### Figure 27. Interfacing with Various Logic Families



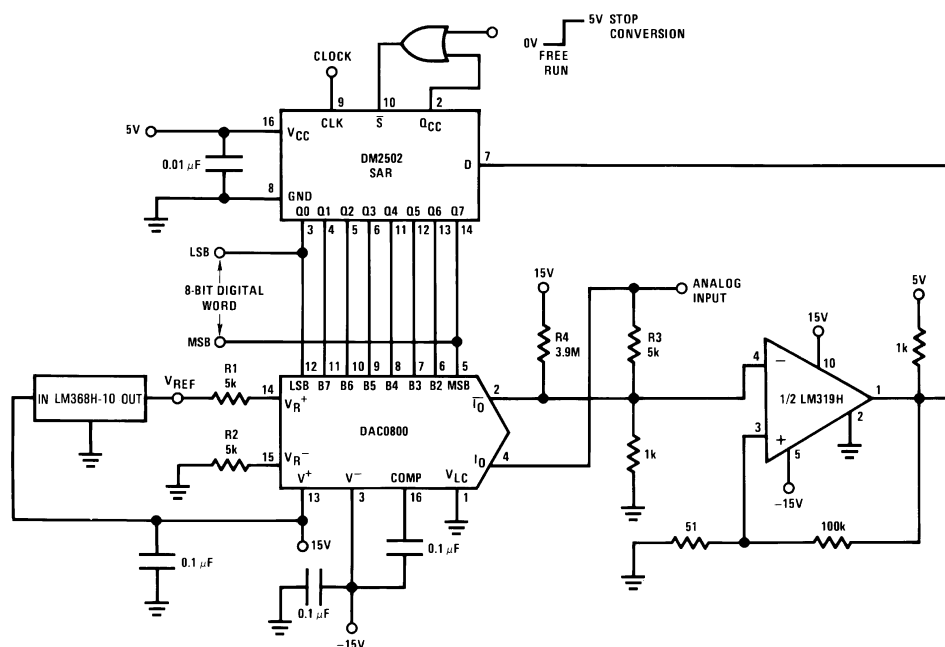
Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

### Figure 28. Accommodating Bipolar References



Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 29. Settling Time Measurement**



- (1) For 1  $\mu s$  conversion time with 8-bit resolution and 7-bit accuracy, an LM361 comparator replaces the LM319 and the reference current is doubled by reducing R1, R2 and R3 to 2.5 k $\Omega$  and R4 to 2 M $\Omega$ .
- (2) Pin numbers represent the PDIP package. The SOIC package pin numbers differ from that of the PDIP package.

**Figure 30. A Complete 2  $\mu s$  Conversion Time, 8-Bit A/D Converter**

## REVISION HISTORY

Changes from Revision B (February 2013) to Revision C	Page
<ul style="list-style-type: none"><li>Changed layout of National Data Sheet to TI format .....</li></ul>	<a href="#">12</a>

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DAC-08EP	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DAC0800LCN DAC-08EP	<a href="#">Samples</a>
DAC0800LCM	ACTIVE	SOIC	D	16	48	TBD	Call TI	Call TI	0 to 70	DAC0800LCM	<a href="#">Samples</a>
DAC0800LCM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	<a href="#">Samples</a>
DAC0800LCMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DAC0800LCM	<a href="#">Samples</a>
DAC0800LCMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0800LCM	<a href="#">Samples</a>
DAC0800LCN	ACTIVE	PDIP	NFG	16	25	TBD	Call TI	Call TI	0 to 70	DAC0800LCN DAC-08EP	<a href="#">Samples</a>
DAC0800LCN/NOPB	ACTIVE	PDIP	NFG	16	25	Pb-Free (RoHS)	SN	Level-1-NA-UNLIM	0 to 70	DAC0800LCN DAC-08EP	<a href="#">Samples</a>
DAC0802LCMX	ACTIVE	SOIC	D	16	2500	TBD	Call TI	Call TI	0 to 70	DAC0802LCM	<a href="#">Samples</a>
DAC0802LCMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DAC0802LCM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0800LCMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0800LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DAC0802LCMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC0800LCMX	SOIC	D	16	2500	367.0	367.0	35.0
DAC0800LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX	SOIC	D	16	2500	367.0	367.0	35.0
DAC0802LCMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0



N16E (Rev G)

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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