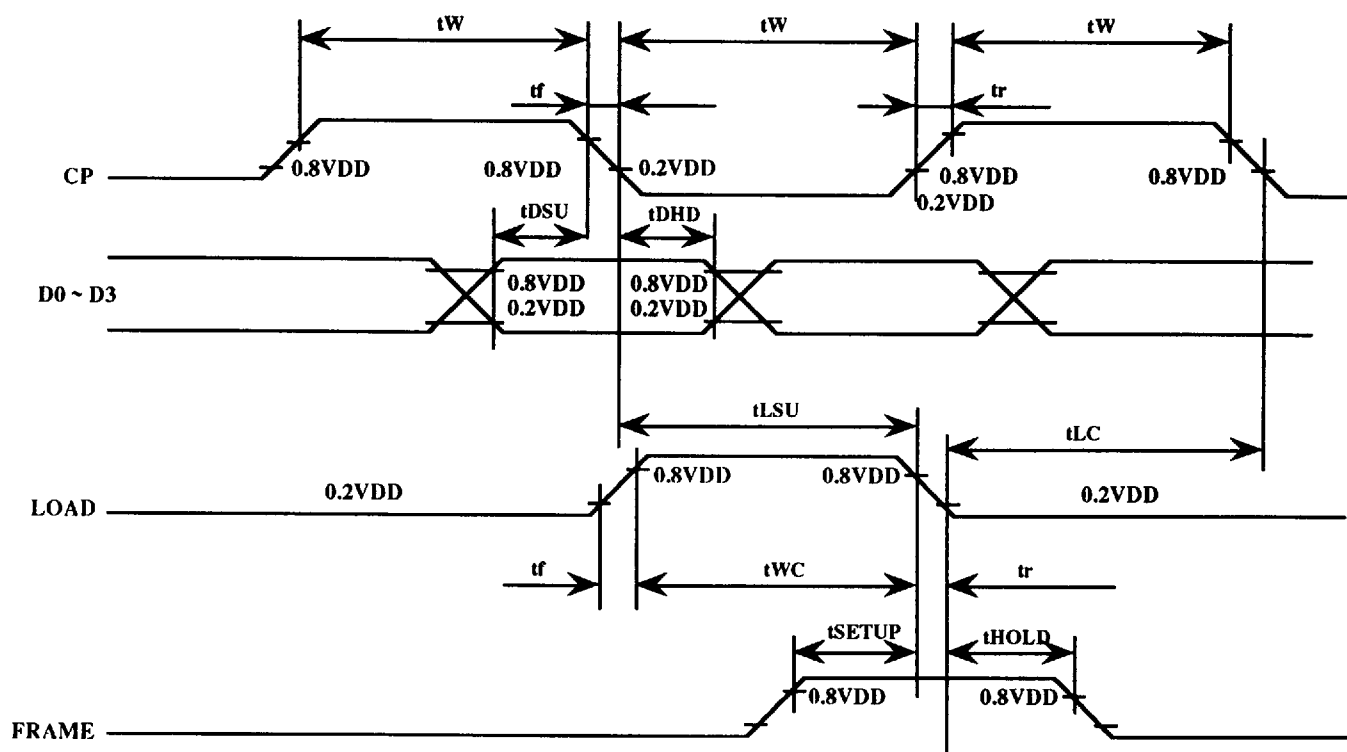


Note 1: fFRAME = 75Hz, D0 ~ D3 = 0, 1, 0, 1, ... VDD - V0 = (23.7), Ta = 25°C
 Note 2: Recommended LC Driving Voltage fluctuates about $\pm 1.0V$ by each module

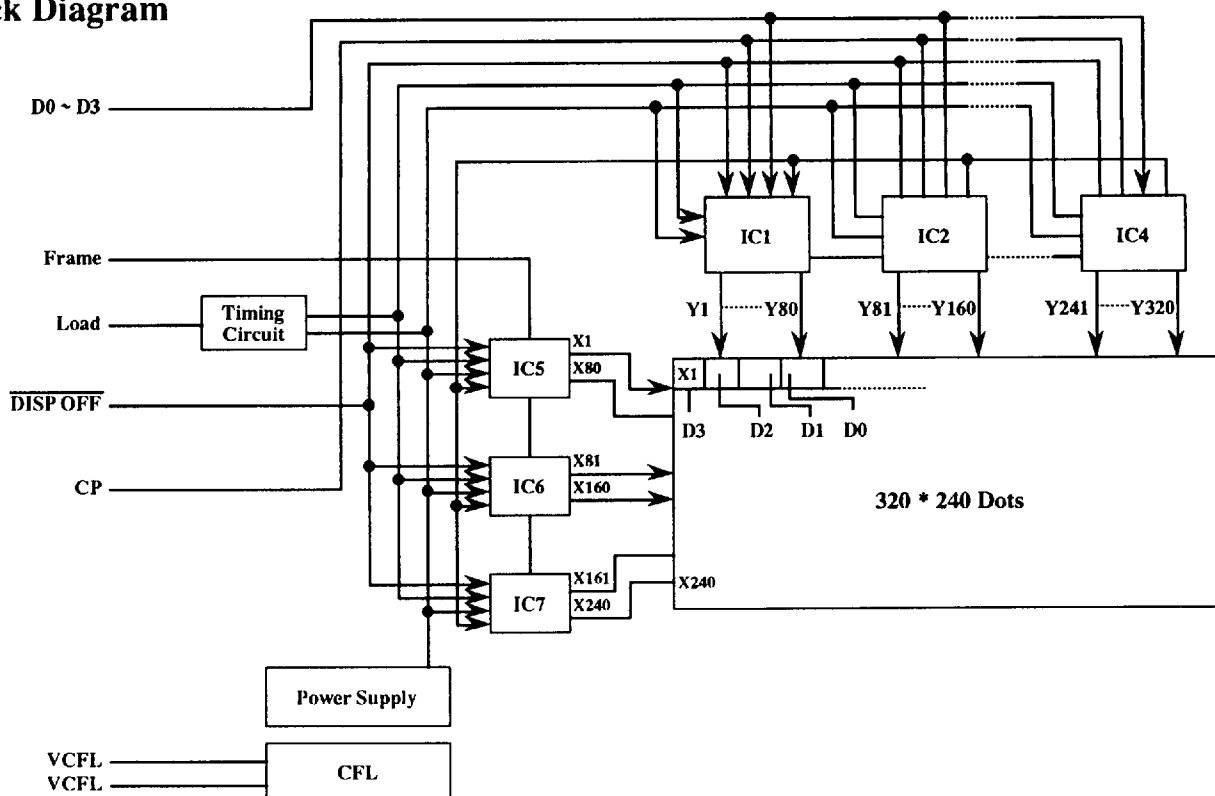
Interface Timing (MPU ↔ LMG)



Timing Characteristics

Item	Symbol	Min	Typ	Max	Unit
Clock Frequency	FCP	-	-	6.5	MHz
Clock Pulse Width	t_W	63	-	-	ns
Clock Rise, Fall Time	t_r, t_f	-	-	20	ns
Data Set-Up Time	t_{DSU}	50	-	-	ns
Data Hold Time	t_{DHD}	50	-	-	ns
Load Set-Up Time	t_{LSU}	80	-	-	ns
Load → Clock Time	t_{LC}	80	-	-	ns
"FRAME" Set-Up Time	t_{SETUP}	100	-	-	ns
"FRAME" Hold Time	t_{HOLD}	100	-	-	ns
"LOAD" Pulse Width	t_{twi}	125	-	-	ns

Block Diagram



External Dimensions

