International Rectifier

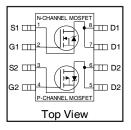
AUTOMOTIVE GRADE

AUIRF7309Q

HEXFET® Power MOSFET

Features

- Advanced Planar Technology
- Low On-Resistance
- Dual N and P Channel MOSFET
- Dynamic dV/dT Rating
- 150°C Operating Temperature
- Fast Switching
- · Lead-Free, RoHS Compliant
- Automotive Qualified*



	N-CH	P-CH
V _{(BR)DSS}	30V	-30V
R _{DS(on)} max.	0.05Ω	0.10Ω
I _D	4.7A	-3.5A

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	M	ax.	Units
		N-Channel	P-Channel	
I _D @ T _A = 25°C	10 Sec. Pulsed Drain Current, V _{GS} @ 10V	4.7	-3.5	
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	4	-3.0	
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	3.2	-2.4	A
I _{DM}	Pulsed Drain Current ①	16	-12	
P _D @T _A = 25°C	Power Dissipation 4	1	1.4	
	Linear Derating Factor 4	0.0	0.011	
V_{GS}	Gate-to-Source Voltage	±	± 20	
dv/dt	Peak Diode Recovery dv/dt ②	6.9	-6.0	V/ns
T_J	Operating Junction and	-55 to	-55 to + 150 °C	
T _{STG}	Storage Temperature Range			

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{ hetaJA}$	Junction-to-Ambient (PCB Mount, steady state) 4		90	°C/W

HEXFET® is a registered trademark of International Rectifier. *Qualification standards can be found at http://www.irf.com/

AUIRF7309Q

Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Тур.	Max.	Units	Conditions
V	Drain-to-Source Breakdown Voltage	N-Ch	30			V	$V_{GS} = 0V, I_D = 250\mu A$
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	P-Ch	-30				$V_{GS} = 0V, I_D = -250\mu A$
A)/ /AT	Brookdown Voltage Tomp Coefficient	N-Ch		0.032		V/°C	Reference to 25°C, I _D = 1mA
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	P-Ch		-0.037			Reference to 25°C, I _D = -1mA
		N-Ch			0.050		$V_{GS} = 10V, I_D = 2.4A$ ③
Ь	Static Drain-to-Source On-Resistance	IN-CII			0.080	Ω	$V_{GS} = 4.5V, I_D = 2.0A$ ③
R _{DS(on)}	Static Drain-to-Source On-Resistance	P-Ch			0.10	1	V _{GS} = -10V, I _D = 1.8A ③
		P-Cn			0.16		$V_{GS} = -4.5V, I_D = 1.5A$ ③
V	Cata Thuashald Valtage	N-Ch	1.0		3.0	V	$V_{DS} = V_{GS}, I_{D} = 250\mu A$
$V_{GS(th)}$	Gate Threshold Voltage	P-Ch	-1.0		-3.0	1	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
auf a	Famusand Transcenductions	N-Ch	5.2			S	$V_{DS} = 15V, I_D = 2.4A$
gfs	Forward Transconductance	P-Ch	2.5				$V_{DS} = -24V, I_{D} = -1.8A$
		N-Ch			1.0		$V_{DS} = 24V, V_{GS} = 0V$
	Duain to Carros Laskana Criment	P-Ch		_	-1.0	μΑ	$V_{DS} = -24V, V_{GS} = 0V$
I _{DSS}	Drain-to-Source Leakage Current	N-Ch			25		$V_{DS} = 24V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
		P-Ch			-25]	$V_{DS} = -24V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Forward Leakage	N-P			-100		$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	N-P			100	nA	V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Тур.	Max.	Units	Conditions
0	Total Cata Charge	N-Ch			25		N-Channel
Q_g	Total Gate Charge	P-Ch			25		$I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V$
0	Cata to Source Charge	N-Ch			2.9	nC	3
Q_{gs}	Gate-to-Source Charge	P-Ch			2.9		P-Channel
0	Gate-to-Drain ("Miller") Charge	N-Ch			7.9		$I_D = -2.2A$, $V_{DS} = -16V$, $V_{GS} = -4.5V$
Q_{gd}	Gate-to-Drain (Willer) Charge	N-Ch			9.0		
	Turn-On Delay Time	P-Ch		6.8			N-Channel
t _{d(on)}	Turn-On Delay Time	N-Ch		11			$V_{DD} = 10V, I_D = 2.6A R_G = 6.0\Omega$
+	Rise Time	P-Ch		21			$R_D = 3.8\Omega$
τ _r	nise fille	N-Ch		17		ns	
+	Turn-Off Delay Time	N-Ch		22			P-Channel
t _{d(off)}	Turn-On Delay Time	P-Ch		25			V_{DD} =-10V, I_{D} =-2.2A R_{G} = 6.0 Ω
+.	Fall Time	N-Ch		7.7			$R_D = 4.5\Omega$
ι _f	I all Tille	P-Ch		18			
L _D	Internal Drain Inductance	N-P		4.0			Between lead,
						nH	6mm (0.25in.)
L _S	Internal Source Inductance	N-P		6.0			from package
							and center of die contact
C _{iss}	Input Capacitance	N-Ch		520			N-Channel
Oiss	input dapacitance	P-Ch		440			$V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz$
Coss	Output Capacitance	N-Ch		180		pF	3
oss	Output Oupdonance	P-Ch		200			P-Channel
C _{rss}	Reverse Transfer Capacitance	N-Ch		72			$V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz$
orss	neverse transier Capacitance	P-Ch		93			

Diode Characteristics

	Parameter		Min.	Тур.	Max.	Units	Conditions
	Continuous Source Current	N-Ch			1.8		
I _S	(Body Diode)	P-Ch			-1.8	А	
	Pulsed Source Current	(Body N-Ch			16		
ISM	Diode) ①	P-Ch			-12		
V_{SD}	Diode Forward Voltage	N-Ch			1.0	V	$T_J = 25^{\circ}C$, $I_S = 1.8A$, $V_{GS} = 0V$ ③
V SD	blode i orward voltage	P-Ch			-1.0		$T_J = 25^{\circ}C$, $I_S = -1.8A$, $V_{GS} = 0V$ ③
+	Reverse Recovery Time	N-Ch		47	71	ns	N-Channel
L _{rr}	neverse necovery fillie	P-Ch		53	80		$T_J = 25^{\circ}C, I_F = 2.6A, di/dt = 100A/\mu s$
0	Q _{rr} Reverse Recovery Charge	N-Ch		56	84	nC	P-Channel 3
Q _{rr}		P-Ch		66	99		$T_J = 25^{\circ}C, I_F = -2.2A, di/dt = 100A/\mu s$
t _{on}	Forward Turn-On Time	N-P	Intrinsic tu	rn-on time is	negligible (turn-on is d	ominated by LS+LD)

Notes:

- $\ensuremath{\mathbb{O}}$ Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)
- $\begin{tabular}{l} \hline @ N-Channel $I_{SD} \le 2.4A$, $di/dt \le 73A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 150°C$. \\ \hline P-Channel $I_{SD} \le -1.8A$, $di/dt \le 90A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 150°C$. \\ \hline \end{tabular}$
- 3 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.
- When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Qualification Information[†]

			Automotive				
		(per AEC-Q101) ††					
Qualification Lev	rel	Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.					
Moisture Sensitiv	vity Level	SO-8 MSL1					
	Machine Model		N-CH: Class M2 (+/- 150V) ^{†††}				
		P-CH: Class M2 (+/- 150V) ^{†††}					
		AEC-Q101-002					
	Human Body Model		N-CH: Class H1A (+/- 500V) ^{†††}				
ESD			P-CH: Class H0 (+/- 250V) ^{†††}				
			AEC-Q101-001				
	Charged Device		N-CH: Class C5 (+/- 2000V) ^{†††}				
Model		P-CH: Class C5 (+/- 2000V) ^{†††}					
		AEC-Q101-005					
RoHS Compliant			Yes				

[†] Qualification standards can be found at International Rectifier's web site: http://www.irf.com/

^{††} Exceptions to AEC-Q101 requirements are noted in the qualification report.

^{†††} Highest passing voltage.

N-Channel

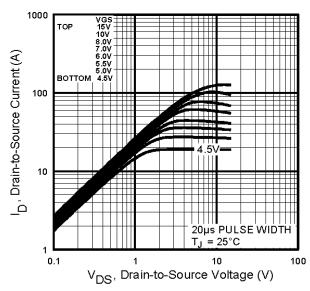


Fig 1. Typical Output Characteristics, T_J = 25°C

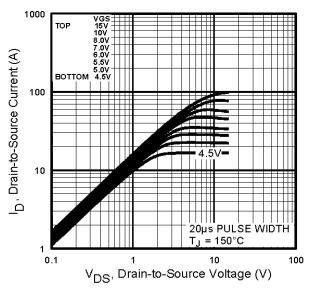


Fig 2. Typical Output Characteristics, $T_J = 150^{\circ}C$

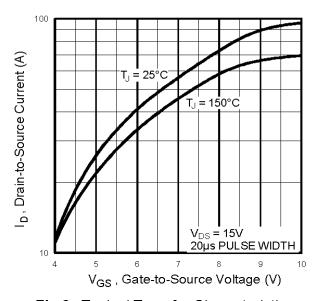


Fig 3. Typical Transfer Characteristics

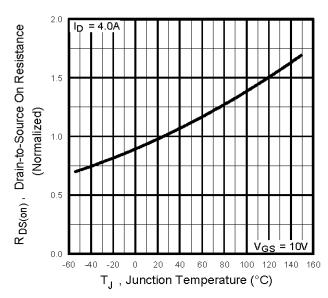


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel

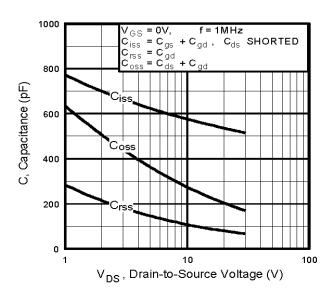


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

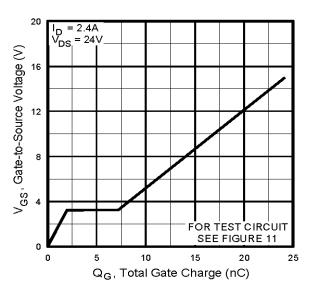


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

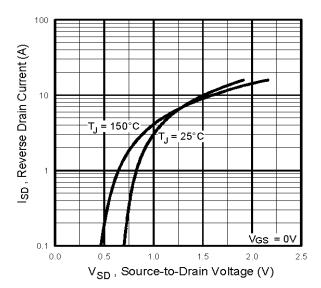


Fig 7. Typical Source-Drain Diode Forward Voltage

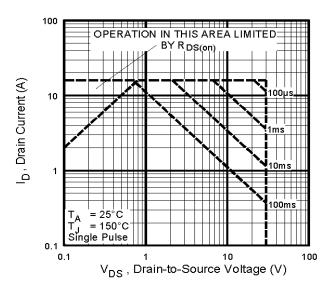


Fig 8. Maximum Safe Operating Area

0.0

1.0 Drain Current (Amps)

 $\label{eq:TA} \textbf{T}_A, \, \text{Ambient Temperature (°C)} \\ \textbf{Fig 9.} \ \, \text{Max. Drain Current } \ \, \text{Vs. Ambient Temp.} \\$

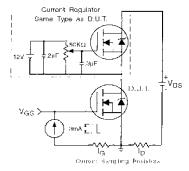
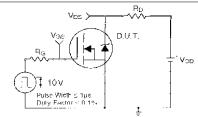


Fig 11a. Gate Charge Test Circuit



N-Channel

P-Channel

Fig 10a. Switching Time Test Circuit

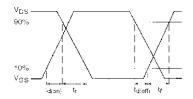


Fig 10b. Switching Time Waveforms

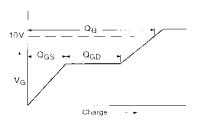


Fig 11b. Basic Gate Charge Waveform

-D-ain-to-Source Current (A) BOALCE Current (

Fig 12. Typical Output Characteristics, Ţ = 25°C

-V_{DS} , Drain-to-Source Voltage (V)

20µs PULSE WIDTH

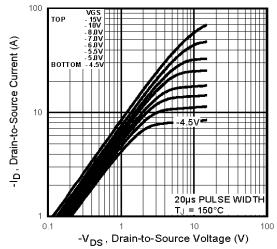
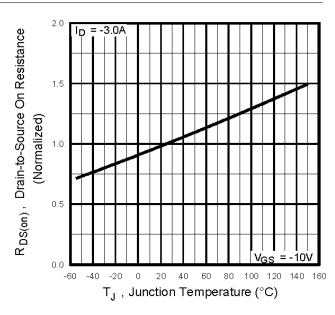


Fig 13. Typical Output Characteristics, T_J = 150°C

T_J = 25°C T_J = 150°C T_J = 150°C V_{DS} = -15V 20µs PULSE WIDTH -V_{GS}, Gate-to-Source Voltage (V)

Fig 14. Typical Transfer Characteristics



P-Channel

Fig 15. Normalized On-Resistance Vs. Temperature

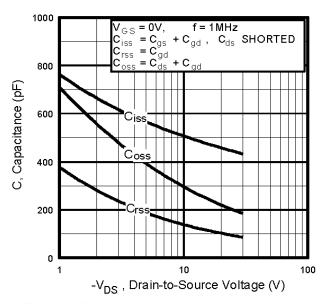


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

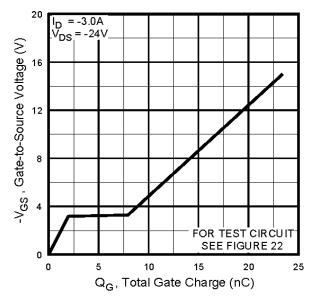


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

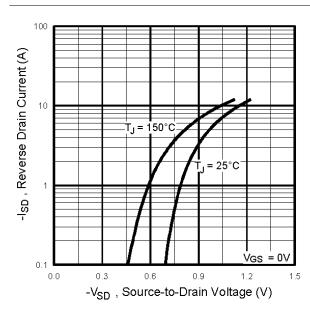


Fig 18. Typical Source-Drain Diode Forward Voltage

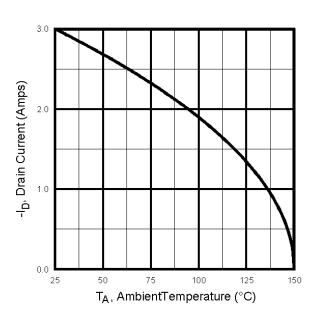


Fig 20. Max. Drain Current Vs. Ambient Temp.

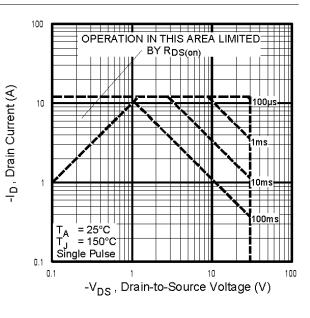


Fig 19. Maximum Safe Operating Area

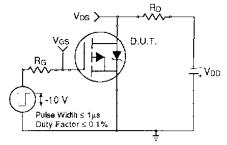


Fig 21a. Switching Time Test Circuit

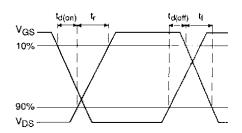
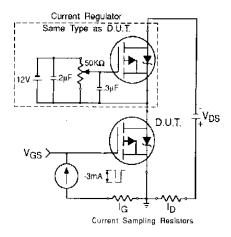


Fig 21b. Switching Time Waveforms

P-Channel





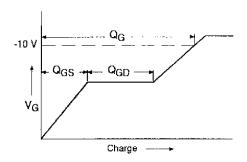


Fig 22b. Basic Gate Charge Waveform

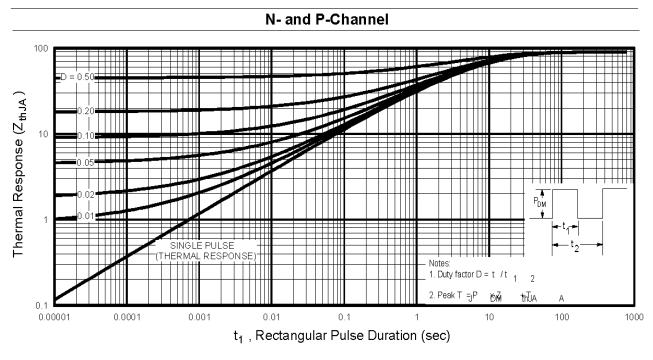
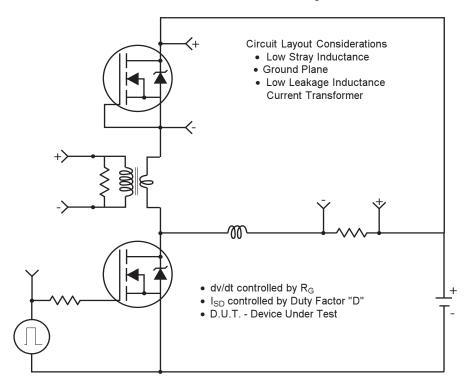
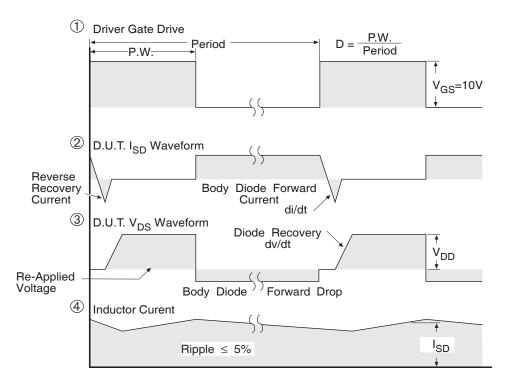


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



- * Reverse Polarity for P-Channel
- ** Use P-Channel Driver for P-Channel Measurements

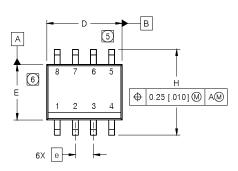


*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 24. For N and P Channel HEXFETS

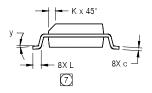
SO-8 Package Outline

Dimensions are shown in millimeters (inches)



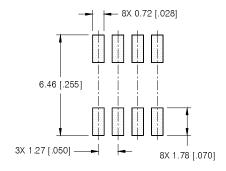
e1	A C
8X b A1	0.10 [.004]
⊕ 0.25 [.010] M C A B	

DIM	INC	HES	MILLIM	ETERS
DIM	MIN	MAX	MIN	MAX
Α	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
С	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
е	.050 B/	.050 BASIC		ASIC
e 1	.025 B/	ASIC	0.635 E	BASIC
Н	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
у	0°	8°	0°	8°



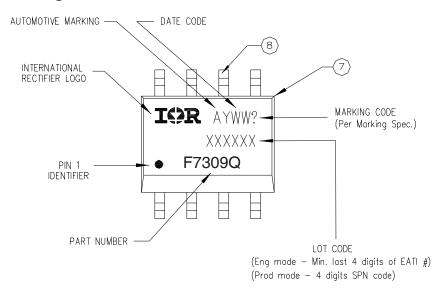
NOTES:

- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- 2. CONTROLLING DIMENSION: MILLIMETER
- 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- (5) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
- (6) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
- [7] DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



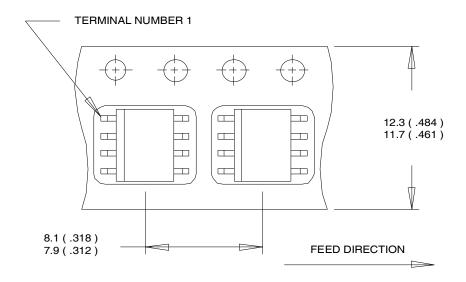
FOOTPRINT

SO-8 Part Marking



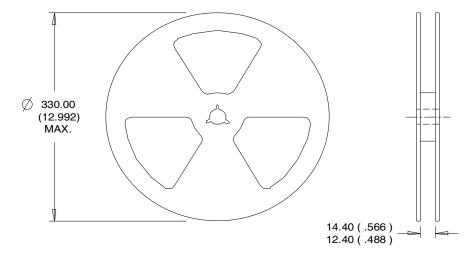
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRF7309Q	SO-8	Tube	95	AUIRF7309Q
		Tape and Reel	4000	AUIRF7309QTR

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For technical support, please contact IR's Technical Assistance Center http://www.irf.com/technical-info/

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