NEC

MOS INTEGRATED CIRCUIT

μPD6345

8 BIT SERIAL IN/PARALLEL OUT DRIVER

The μPD6345 is a monolithic Bi-CMOS integrated Circuit designed to drive LED, Solenoid and Relay.

This device consists of an 8-bit shift register, latch and buffer with high voltage N-P-N Transistors (Open Collector). Data is serially loaded into shift register on the positive-going transition of the clock. Parallel data is transferred to the output buffers through the 8-bit latch while the latch enable input is high and latched when the latch enable is low. When the output enable input is low, all outputs are off (High Impedance).

FEATURES

- High Speed Serially-shifted Data Input.
- Latches on all driver Outputs.
- 40 V Output Voltage Rating.
- 60 mA Output Sink Current.
- Built in power supply voltage detection circuit.
- Capable of connection to cascade additional device.
- Wide Operating Temperature Range: –40 to +85 °C
- Bi-CMOS STRUCTURE

ORDERING INFORMATION

Part Number	Package
μPD6345C	16 Pin Plastic DIP (300 mil)
μPD6345GS	16 Pin Plastic SOP (300 mil)

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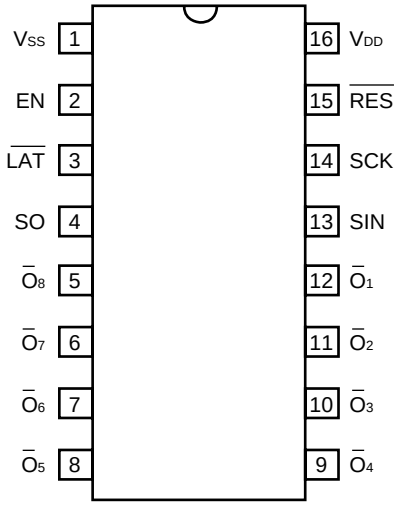
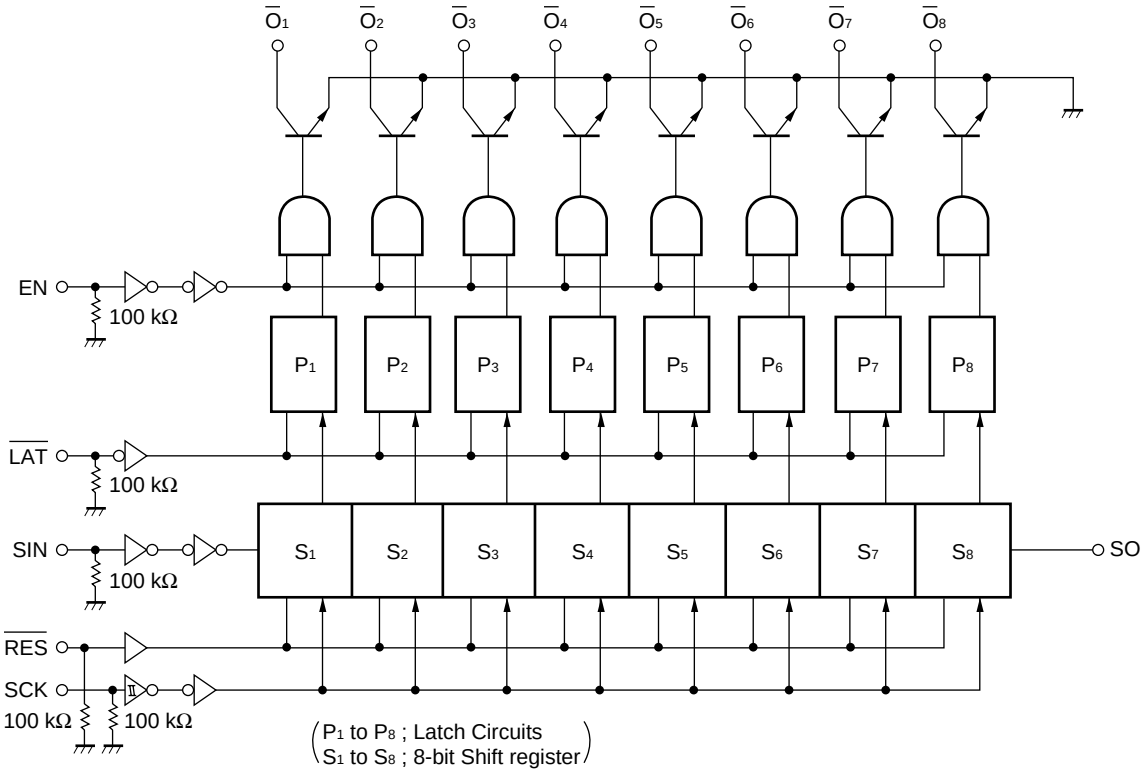
PIN CONFIGURATION (Top View)



PIN IDENTIFICATION

Pin No.	Symbol	Pin name	Input/Output	Function
1	GND	Ground	—	Connection to Ground (GND) of system.
2	EN	Output Enable	Input	When this pin is low or open, all outputs are OFF, and data is output during high.
3	$\overline{LAT}$	Latch Enable	Input	When this pin is low or open, data is latched and data is through to output during high.
4	SO	Serial data Output	Output	Serial data is output on positive-going transition of the clock. In case of connection to cascade additional device (μPD6345), this pin will be connected to SIN terminal of additional device.
5 to 12	$\overline{O_8}$ to $\overline{O_1}$	Driver Output	Output	High Voltage and Current Driver Outputs.
13	SIN	Serial data Input	Input	Data is loaded to shift register on positive-going transition.
14	SCK	Clock	Input	Data of SIN is loaded to shift register on positive-going transition of SCK. Also, serial data is output from SO on positive-going transition of SCK.
15	$\overline{RES}$	Reset	Input	When this pin is low or open, data of shift register is all cleared, and this device operate normally during high.
16	V_{DD}	Power Supply	—	Normally supply 5 V.

BLOCK DIAGRAM



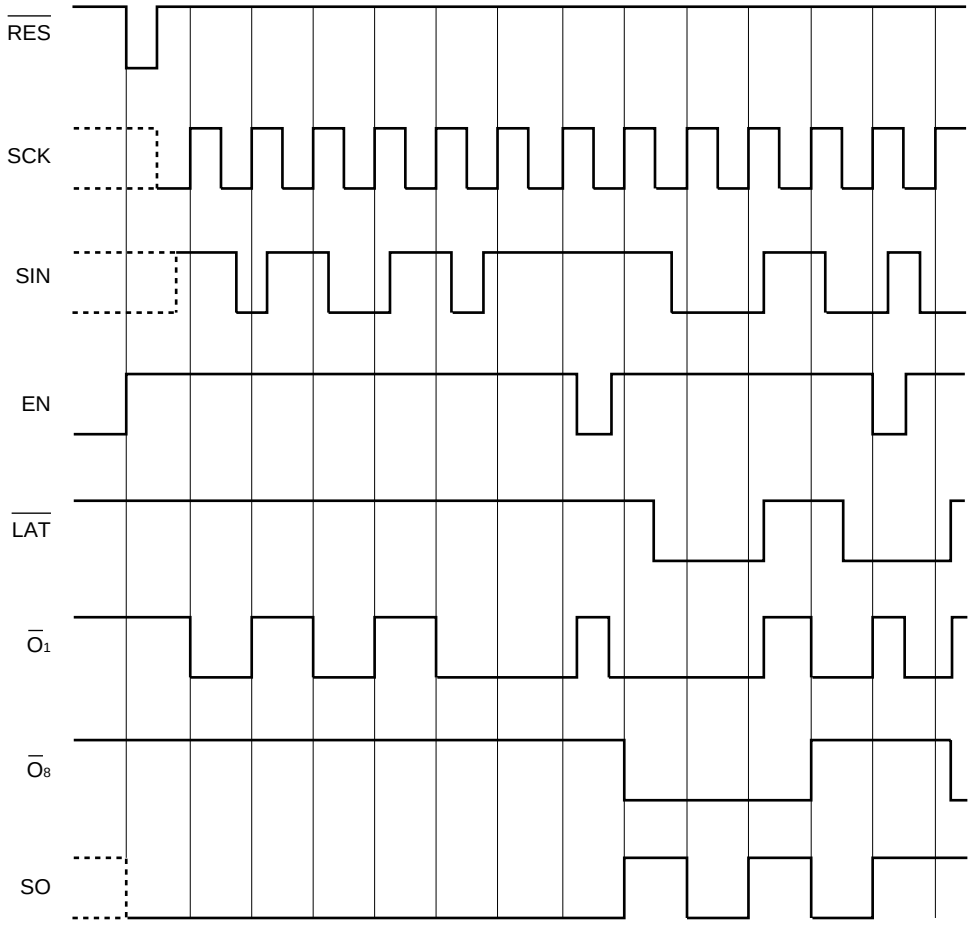
TRUTH TABLE

SCK	EN	$\overline{RES}$	$\overline{LAT}$	SIN	OUT		SO*1	Note
					$\overline{O_1}$	$\overline{O_n}$		
↑	H	H	H	L	High Impedance	$\overline{O_{n-1}}$	S_7	SCK = CLOCK EN = Output Enable $\overline{RES}$= Reset $\overline{LAT}$= Latch Enable SIN = Serial data Input OUT = Driver Output SO = Serial data Output * = H or L H = High level L = Low level
↑	H	H	H	H	L	$\overline{O_{n-1}}$	S_7	
↑	H	H	L*2	*	NO CHANGE	NO CHANGE	S_7	
↑	L	H	*	*	High Impedance	High Impedance	S_7	
↓	*	*	*	*	NO CHANGE	NO CHANGE	S_8	
*	*	L	H	*	High Impedance	High Impedance	L	
*	H	⊓	L	*	NO CHANGE	NO CHANGE	L	

*1) Seventh data S_7 of shift register is loaded to eighth data S_8 on positive-going transition of clock, and is output to Serial data Output pin.

*2) Shift register operates normally.

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C ± 2 °C)

Supply Voltage	V_{DD}	–0.3 to 7.0	V
Input Voltage	V_{IN}	–0.3 to V_{DD} + 0.3	V
Input Current	V_{IN}	±10	mA
Logic Output Voltage	V_{SO1}	–0.3 to V_{DD} + 0.3	V
Driver Output Voltage	V_{OUT2}	–0.3 to 40	V
Driver Output Current	I_{OUT}	100	mA
Logic Output Current	I_{SO}	+10 –5	mA
Power Dissipation	P_D	850 (DIP), 800 (SOP)	mW
Operating Temperature	T_{opt}	–40 to + 85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Temperature	T_{opt}	–40		+85	°C
Supply Voltage	V_{DD}	4.0	5.0	6.0	V
Input Voltage	V_{IN}	0		V_{DD}	V
High Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V
Low Level Input Voltage	V_{IL}	0		0.2 V_{DD}	V
Clock Frequency	f_{SCK}			8	MHz
Driver Output Voltage	V_{OUT}	0		38	V

ELECTRICAL CHARACTERISTICS (RH ≤ 70 %, V_{SS} = 0 V)

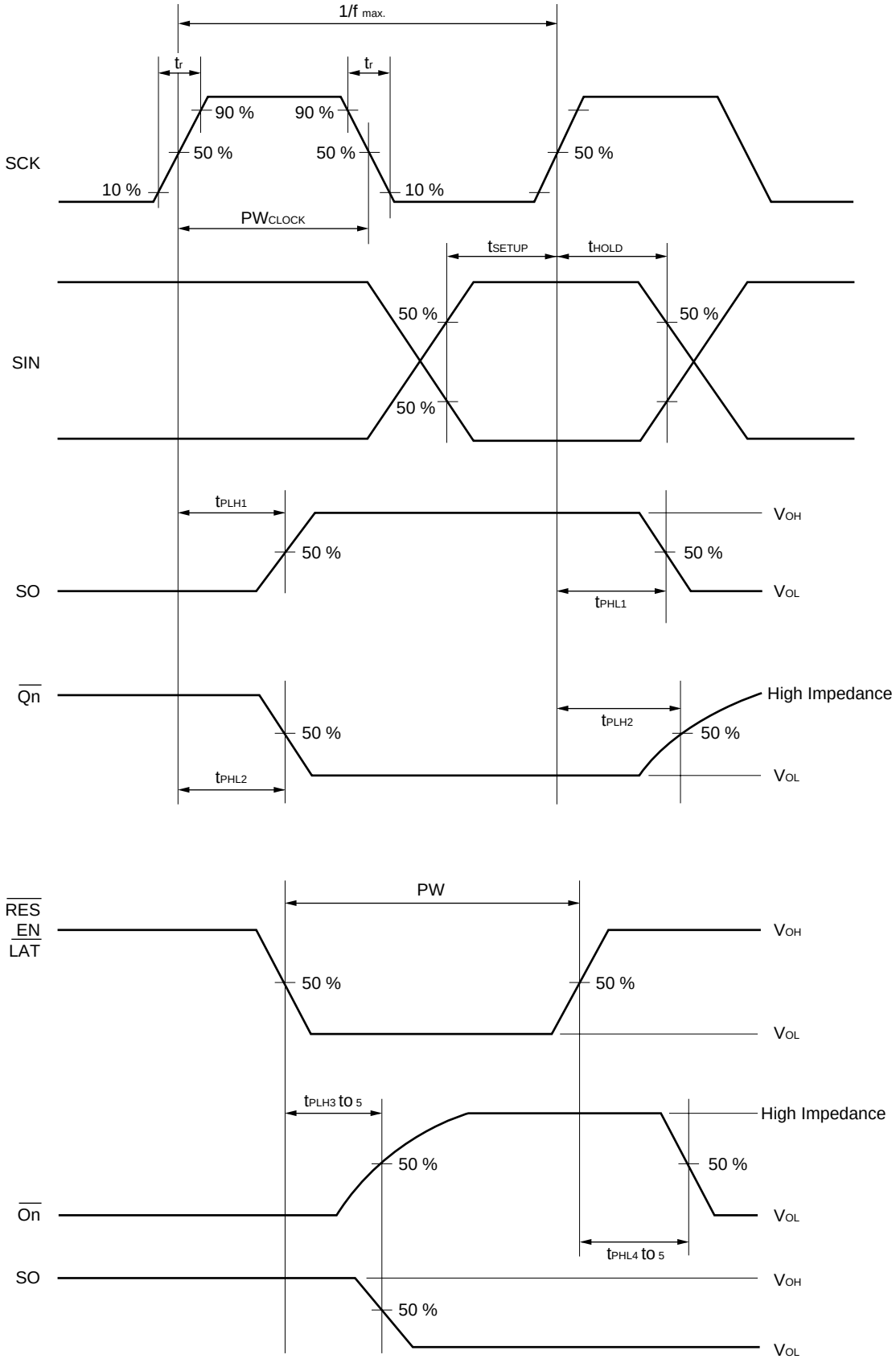
ITEM	SYMBOL	CONDITION		T_a = 25 °C			T_a = –40 to +85 °C			UNIT
		V_{DD} (V)		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
High Level Input Voltage	V_{IH}	5.0		3.5	2.4		3.5			V
		6.0		4.2			4.2			
Low Level Input Voltage	V_{IL}	5.0			1.7	1.0			1.0	V
		6.0				1.2			1.2	
High Level Input Current	I_{IH}	6.0	$V_{IN} = V_{DD}$		100	300			300	μA
Low Level Input Current	I_{IL}	6.0	$V_{IN} = V_{SS}$		0.03	0.3			1	μA
High Level Output Voltage 1	V_{SOH1}	5.0	I_{SOH} = –250 μA	3.6			3.6			V
		6.0	I_{SOH} = –300 μA	4.3			4.3			
High Level Output Voltage 2	V_{SOH2}	5.0	I_{SOH} = –10 μA	4.0			4.0			V
		6.0		5.0			5.0			
High Level Output Voltage 3	V_{SOH3}	5.0	I_{SOH} = –1 μA	3.3			3.3			V
		6.0		4.0			4.0			
Low Level Output Voltage	V_{SOL}	5.0	I_{SOL} = 8 μA						0.6	V
		6.0							0.5	
Low Level Output Voltage (Driver)	$V_{OUT(L)}$	5.0	I_{OUT} = 60 μA		0.45	0.8			1.0	V
High Level Output Leakage Current	I_{OHL}	5.0				10			10	μA
Supply Current	I_{DD1}	5.0	$\overline{O_1} – \overline{O_8}$		0.25	0.5			1.0	mA
	I_{DD2}	5.0			23	35			40	
Input Capacitance	C_{IN}	—			6	15			15	pF

SWITCHING CHARACTERISTICS

(T_a = 25 °C, V_{DD} = 5 V, C_L = 15 pF, R ($\overline{O_n}$) = 300 Ω, V_{OUT} = 12 V, t_r = t_f = 6 ns)

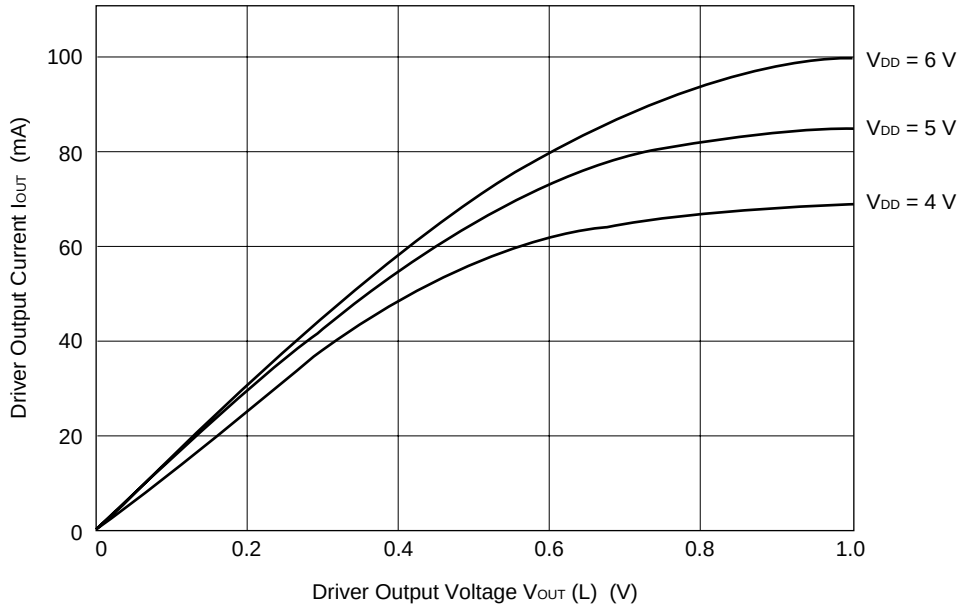
ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time	t_{PLH1}	SCK → SO (High Level)	20		100	ns
	t_{PLH2}	SCK → Driver Output (High Level)	20		1	μs
	t_{PHL1}	SCK → SO (Low Level)			100	ns
	t_{PHL2}	SCK →Driver Output (Low Level)			1	μs
	t_{PHL3}	RESET → SO			100	ns
	$t_{PHL/PLH4}$	Output Enable → Driver Output			1	μs
	$t_{PHL/PLH5}$	Latch Enable → Driver Output			1	μs
Clock Transition Time	t_r t_f	SCK		70		μs
Maximum Clock Frequency	f_{max}			13	8	MHz
Minimum Data Setup Time	t_{SETUP}		20	10		ns
Minimum Data Hold Time	t_{HOLD}		20	10		ns
Minimum Reset Pulse Width	PW_{RESET}		62.5	10		ns
Minimum Output Enable Pulse Width	PW_{ENABLE}		1	0.55		μs
Minimum Latch Enable Pulse Width	PW_{LATCH}		62.5	38		ns
Clock Pulse Width	PW_{SCK}			38	62.5	ns

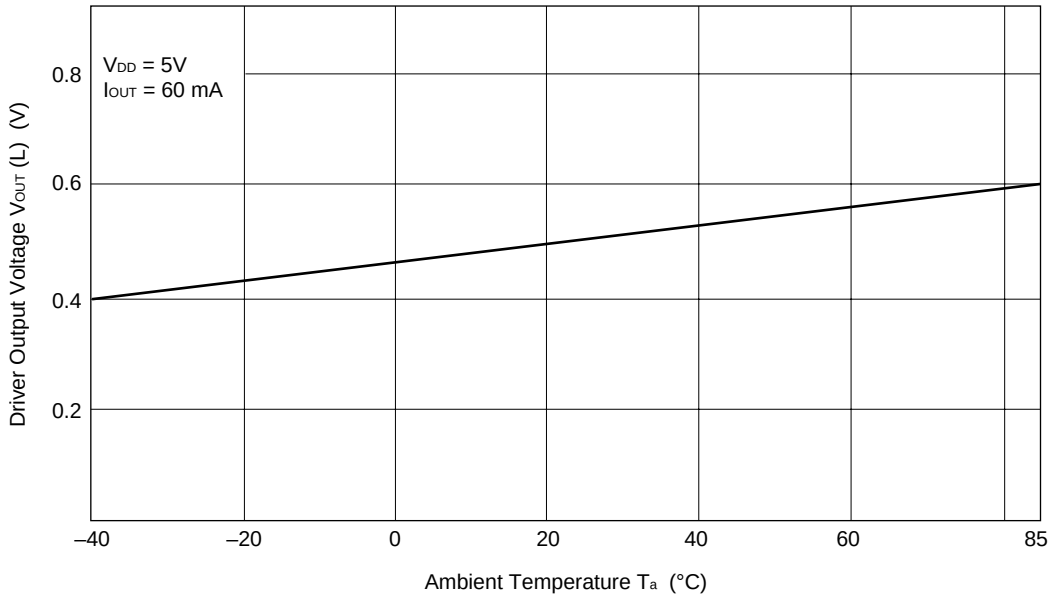
TIMING WAVEFORMS



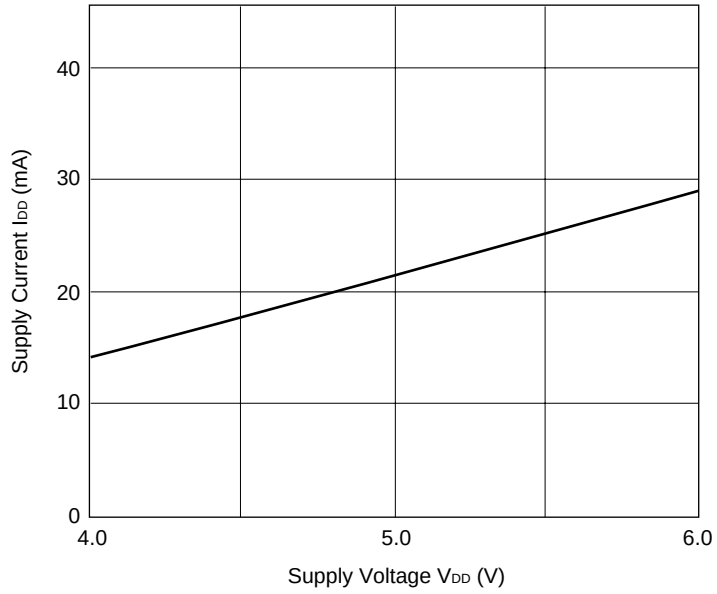
TYPICAL CHARACTERISTICS (T_a = 25 °C)

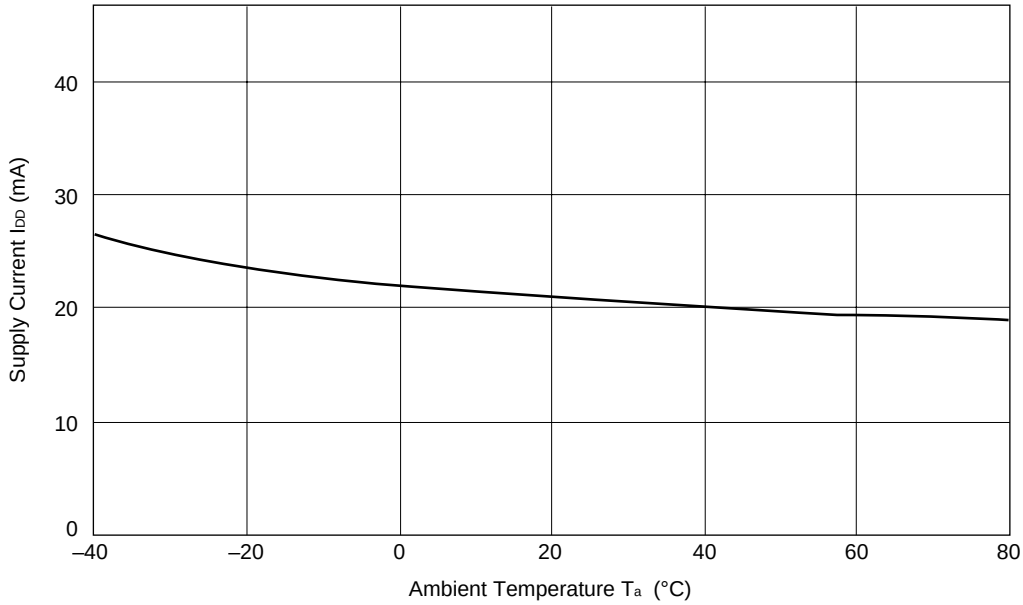
DRIVER OUTPUT CHARACTERISTICS





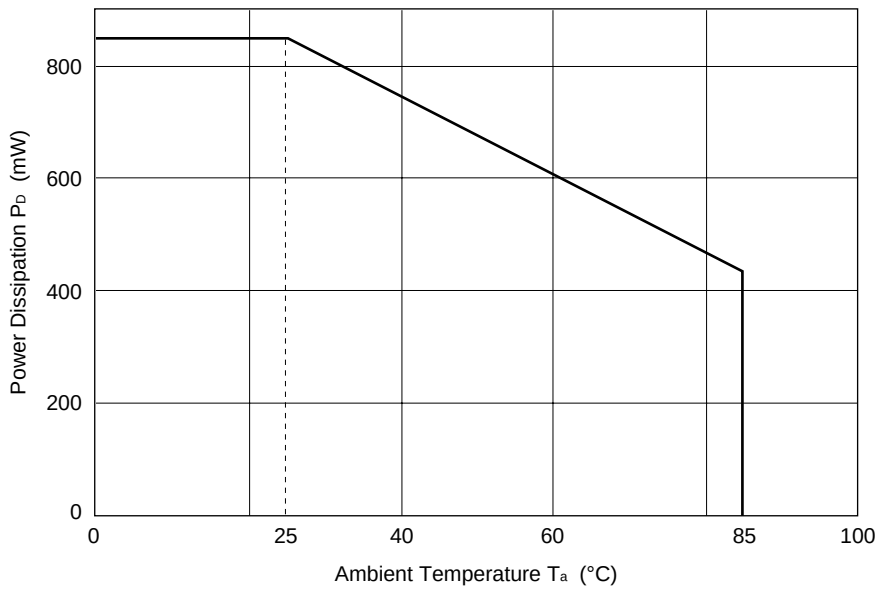
SUPPLY CURRENT CHARACTERISTICS (8 Outputs is all ON, No load)



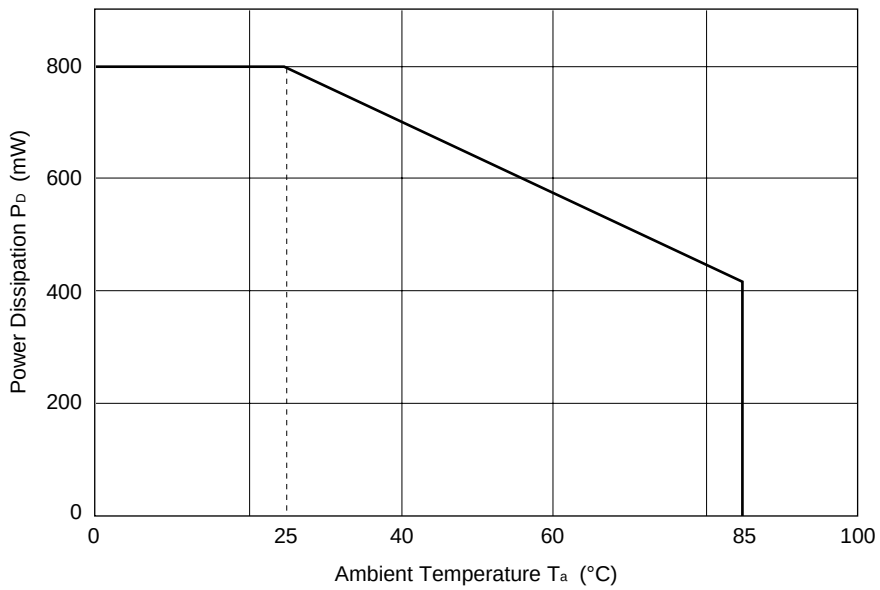


PACKAGE POWER DISSIPATION CHARACTERISTICS

μPD6345 (DIP)

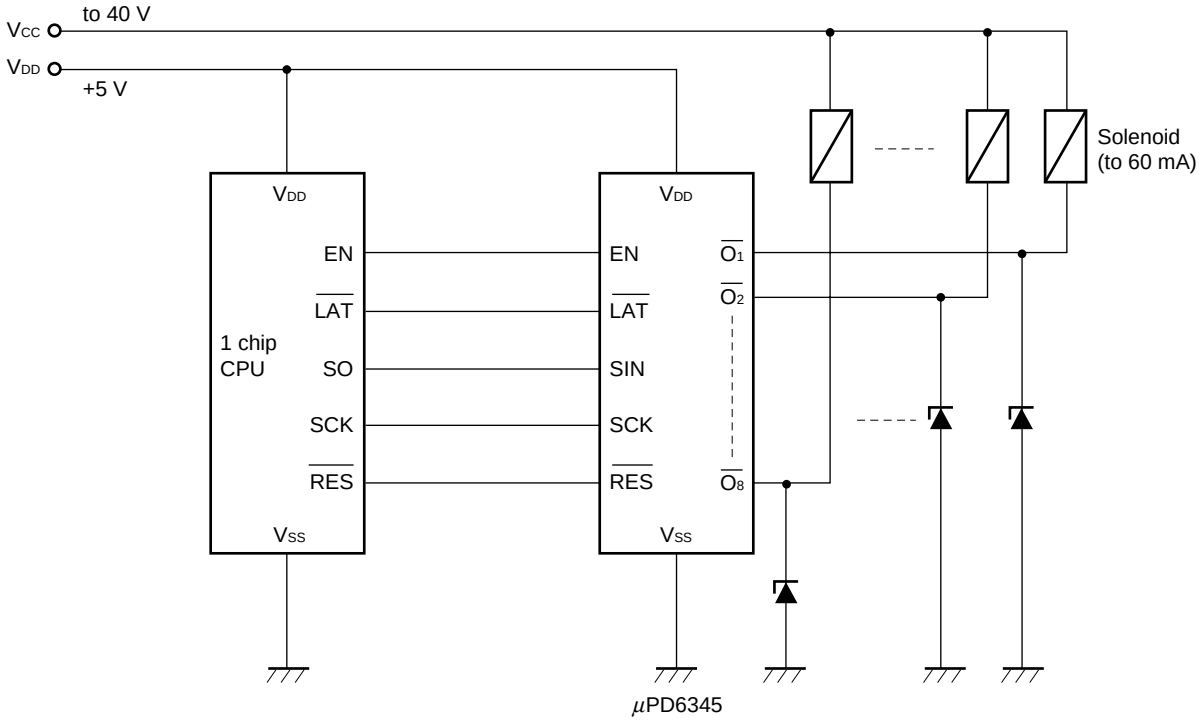


μPD6345 (SOP)

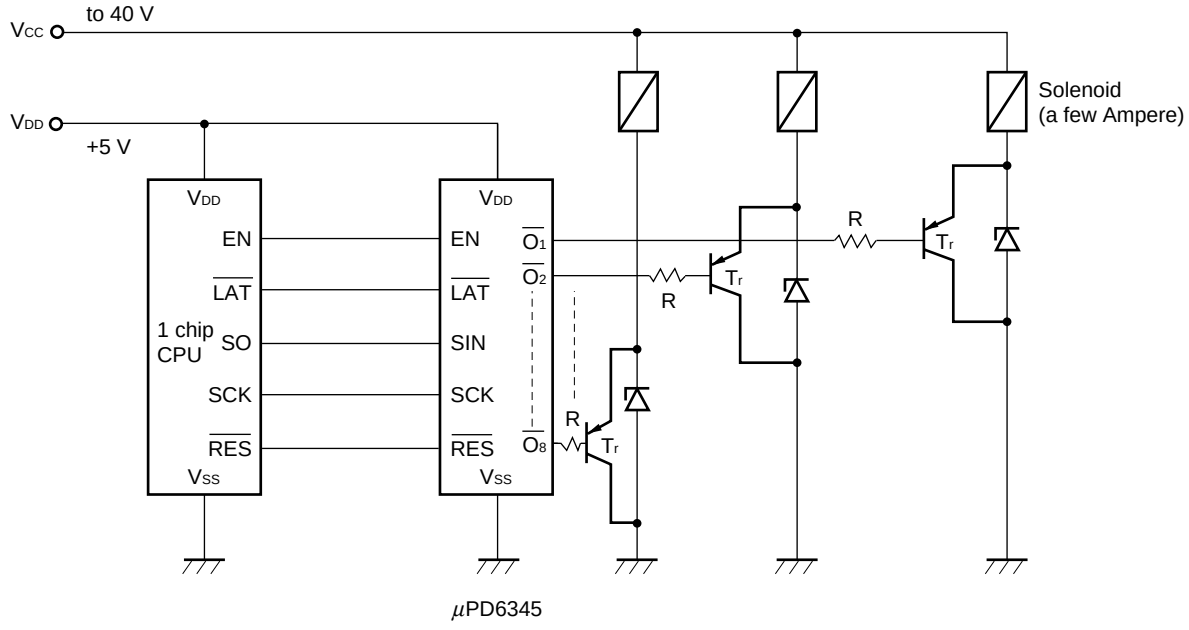


APPLICATION CIRCUIT

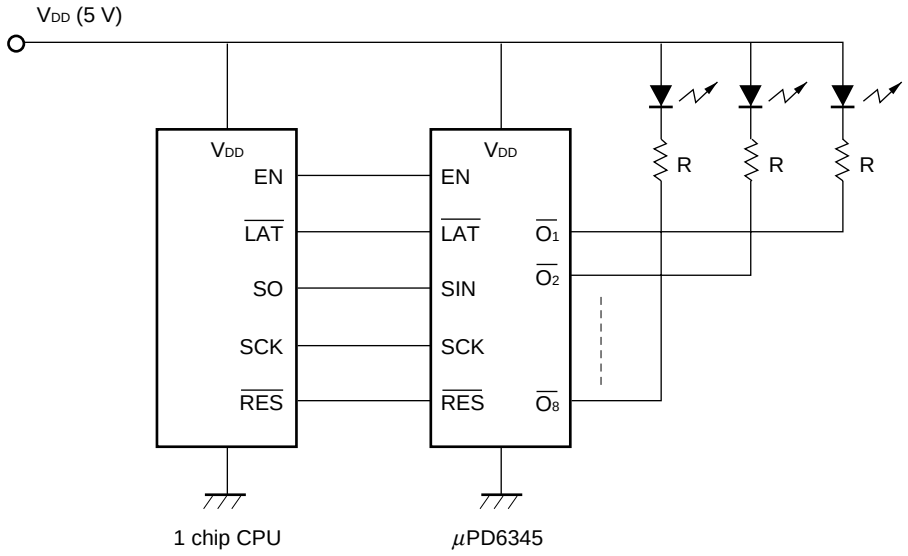
(1) Driving of Solenoid



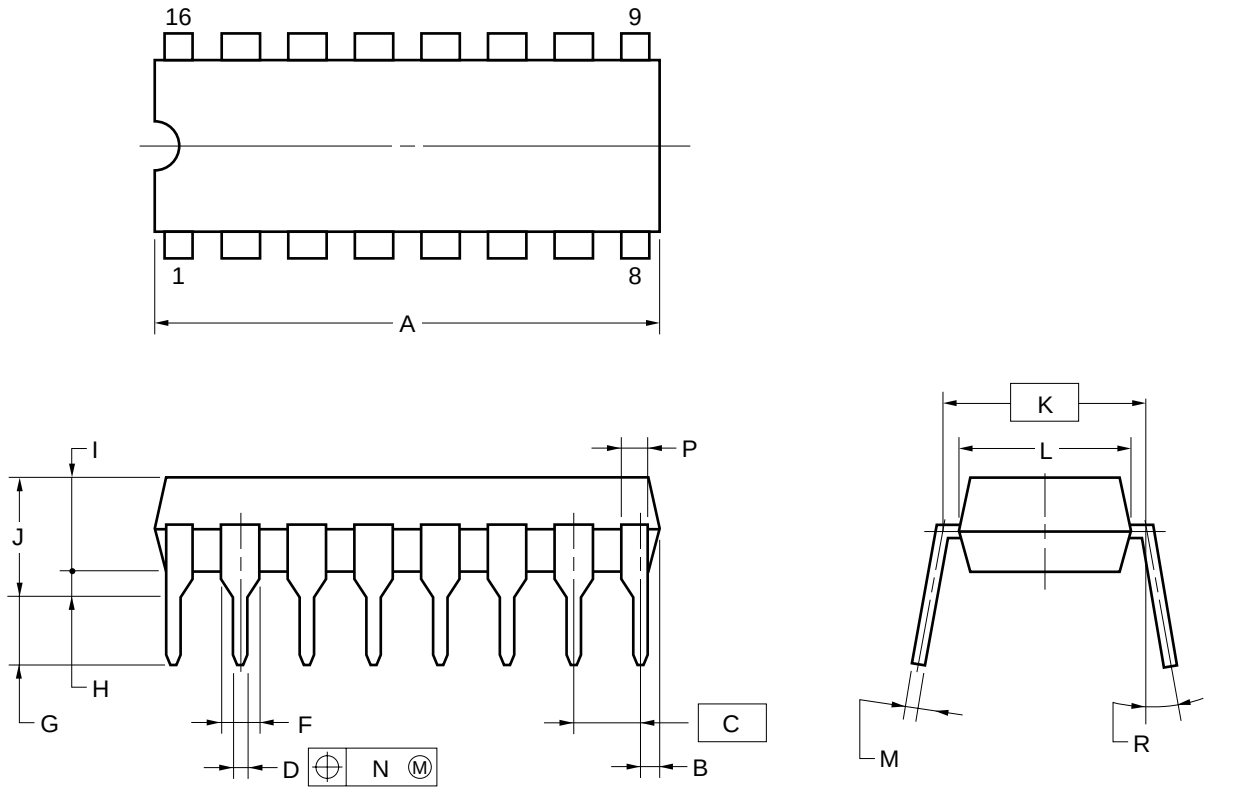
(2) Driving of Solenoid for High Current



(2) Driving of LED



16PIN PLASTIC DIP (300 mil)



NOTES

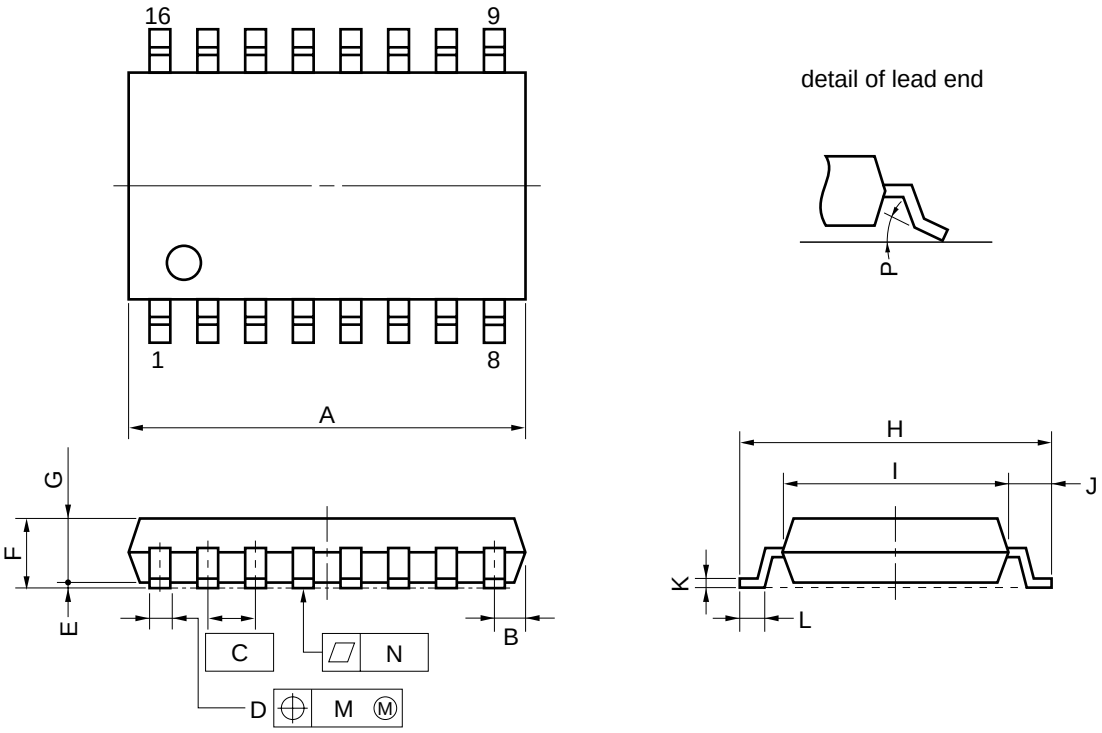
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.
R	0~15°	0~15°

P16C-100-300A,C-1

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P16GM-50-300B-4

[MEMO]

M4 96.5