TEXAS INSTRUMENTS

TUSS4470 Direct Drive Ultrasonic Sensor IC With Logarithmic Amplifier

1 Features

- Integrated driver for directly driving transducers and receiver stage with analog output for ultrasound applications
- 86-dB input dynamic range analog front-end
    - First stage low noise amplifier adjustable to 10, 12.5, 15 and 20 V/V
    - Configurable bandpass filter from 40 KHz to 500 KHz
    - Wide-band logarithmic amplifier
- Supported transducer frequencies (controlled by external clock)
    - 40 KHz to 1 MHz
    - Pre-driver mode: 40 KHz to 440 KHz
- For low-power applications
    - Standby mode: 1.7 mA (typical)
    - Sleep mode: 220 µA (typical)
- Configurable drive stage:
    - Direct drive using internal H-Bridge for transducer excitation
    - Pre-driver configuration to use internal H-bridge to drive external Field Effect Transistors (FETs) for higher current drive
    - Configurable burst patterns using IO1 and IO2 pins
- Outputs:
    - Voltage output of the demodulated echo envelope on VOUT
    - Input signal zero crossing comparator output on OUT3 pin
    - Programmable VOUT threshold crossing on OUT4 pin
- Serial Peripheral Interface (SPI) for configuration by microcontroller (MCU)

2 Applications

- Position sensor
- Level transmitter
- Proximity sensor

3 Description

The TUSS4470 is a highly integrated direct drive analog front end for industrial ultrasonic applications. The transducer drive stage is an internal H-bridge that can be configured to drive the transducer in direct-drive mode to achieve maximum voltage across the transducer. The internal H-bridge can also be configured as a pre-driver for external FETs, enabling higher current and voltage drive for larger transducers.

The receive signal path includes a low-noise linear amplifier, a bandpass filter, followed by a logarithmic gain amplifier for input dependent amplification. The logarithmic amplifier allows for high sensitivity for weak echo signals and offers excellent input dynamic range over full range of reflected echoes.

The drivers can be controlled directly through the microcontroller for complete customization of the burst signal, or can be programmed through SPI with a customizable burst length. The TUSS4470 can support a single transducer to send and receive burst signals, or can set up two transducers to split the send and receive functions.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSS4470	WQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
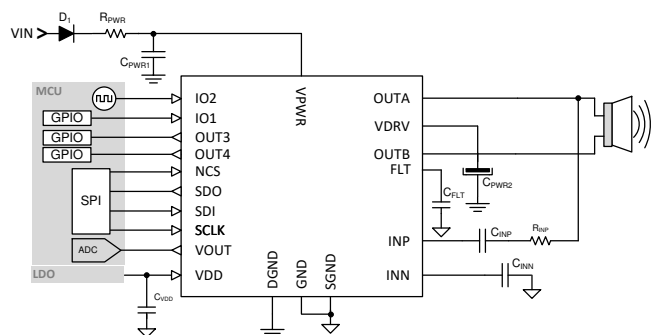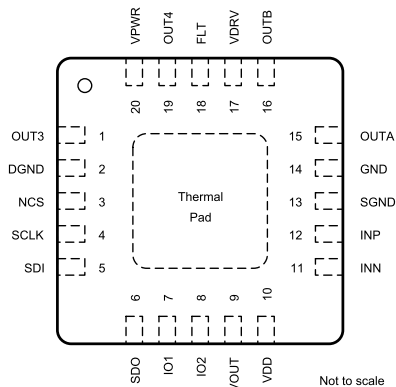
TUSS4470 Application Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2019	*	Initial release.

Product Folder Links: *TUSS4470*

5 Pin Configuration and Functions

RTJ Package
Pin WQFN With Exposed Thermal Pad
Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	OUT3	O	General-purpose digital output
2	DGND	G	Digital ground
3	NCS	I	SPI negative chip select
4	SCLK	I	SPI CLK
5	SDI	I	SPI data input
6	SDO	O	SPI data output
7	IO1	I	General-purpose digital input
8	IO2	I	General-purpose digital input
9	VOUT	O	Demodulated echo analog output
10	VDD	P	Voltage regulator input
11	INN	I	Negative transducer receive
12	INP	I	Positive transducer receive
13	SGND	G	Sensor ground (quiet)
14	GND	G	Ground
15	OUTA	O	Transducer driver output A
16	OUTB	O	Transducer driver output B
17	VDRV	P	H-bridge driver supply voltage
18	FLT	I/O	Filter components
19	OUT4	O	General-purpose digital output
20	VPWR	P	Input supply voltage

(1)   I = input, O = output, I/O = input and output, G = ground, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{VPWR}	Supply voltage range	−0.3	40	V
V_{VDD}	Voltage regulator input voltage	−0.3	5.5	V
V_{VDRV}	H-bridge drive voltage	−0.3	V_{VPWR} + 0.3	V
V_{FLT}	Filter component pin	−0.3	V_{VDD} + 0.3	V
V_{INX}	INP, INN pins input voltage	0.5	1.3	V
V_{DIG_IN}	SCLK, SDI, NCS, IOx pin input voltage	−0.3	V_{VDD} + 0.3	V
V_{VOUT}	Analog output voltage	−0.3	V_{VDD} + 0.3	V
V_{DIG_OUT}	SDO, OUTx, IOx pin output voltage	−0.3	V_{VDD} + 0.3	V
V_{OUTA_B}	OUTA, OUTB pins output voltage	−0.3	V_{VDRV} + 0.3	V
T_A	Ambient temperature	−40	105	
T_J	Junction temperature	−40	125	°C
T_{stg}	Storage temperature	−40	125	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VPWR}	Supply voltage on VPWR pin	5		36	V
V_{VDRV}	Voltage on VDRV pin, internal regulation on VDRV disabled (VDRV_HI_Z=1)[1]	5		36	V
	VDRV voltage Pre driver mode (PRE_DRIVER_MODE=1), internal regulation on VDRV disabled (VDRV_HI_Z=1)[1]	5		15	V
V_{VDIG_IO}	Digital I/O pins	−0.1		V_{VDD}	V
V_{VDD}	Regulated voltage Input	3.1		5.5	V
I_{VPWR_INDIR}	Current consumption at VPWR pin during ranging	150	240	340	µA
I_{VPWR_STDBY}	Current consumption at VPWR in standby mode	150	220	340	µA
I_{VDD_INDIR}	Current consumption at VDD pin during ranging	7	11.5	13	mA
I_{VDD_STDBY}	Current consumption at VDD in standby mode	1.2	1.5	2.5	mA
I_{VDD_SLEEP}	Current consumption in sleep mode			350	µA
T_A	Operating free-air temperature	−25		105	°C
T_J	Operating junction temperature	−40		125	°C

(1) Always V_{VPWR} > V_{VDRV} + 0.3 V to prevent reverse current from VDRV pin to VPWR pin

6.4 Thermal Information

THERMAL METRIC[1]	TUSS4470 RTJ (WQFN) 20 PINS	UNIT
$R_{\theta JA}$ Junction-to-ambient thermal resistance	36.3	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	29.4	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	14.7	°C/W
Ψ_{JT} Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB} Junction-to-board characterization parameter	14.7	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Power-Up Characterstics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PWR_ON}	Time to power up when SPI communication is possible				10	ms
V_{VDRV}	Regulated voltage on VDRV pin[1]	VDRV_VOLTAGE_LEVEL = 0x0; $V_{VPWR} > V_{VDRV}$ + 100 mV	4.5	5	5.3	V
		VDRV_VOLTAGE_LEVEL = 0x4; $V_{VPWR} > V_{VDRV}$ + 100 mV	8.1	9	9.9	
		VDRV_VOLTAGE_LEVEL = 0x7; $V_{VPWR} > V_{VDRV}$ + 100 mV	11.5	12	12.6	
		VDRV_VOLTAGE_LEVEL = 0x8; $V_{VPWR} > V_{VDRV}$ + 100 mV	12.09	13	13.91	
		VDRV_VOLTAGE_LEVEL = 0xC; $V_{VPWR} > V_{VDRV}$ + 100 mV	15.81	17	18.9	
		VDRV_VOLTAGE_LEVEL = 0xD; $V_{VPWR} > V_{VDRV}$ + 100 mV	16.74	18	19.26	
		VDRV_VOLTAGE_LEVEL = 0xE; $V_{VPWR} > V_{VDRV}$ + 100 mV	17.67	19	20.33	
		VDRV_VOLTAGE_LEVEL = 0xF; $V_{VPWR} > V_{VDRV}$ + 100 mV	19.0	20	21.4	
I_{VDRV}	VDRV capacitor charging current	VDRV_CURRENT_LEVEL = 0x0; $V_{VPWR} > V_{VDRV}$ + 1 V	8.5	10	11.5	mA
		VDRV_CURRENT_LEVEL = 0x1; $V_{VPWR} > V_{VDRV}$ + 1 V	17	20	23	

(1) Other VDRV voltage levels possible.

6.6 Transducer Drive

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{HS_FET}	High-side MOSFET on-resistance	T_A = +105°C			30	Ω
R_{LS_FET}	Low-side MOSFET on-resistance	T_A = +105°C			20	Ω

6.7 Receiver Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
G_{LNA}	Low-noise amplifier fixed gain	LNA_GAIN = 0x00; f_{DRV_CLK} = 58 KHz	13.7	15	16.8	V/V
G_{LNA}		LNA_GAIN = 0x01; f_{DRV_CLK} = 58 KHz	9.4	10	12	
G_{LNA}		LNA_GAIN = 0x10; f_{DRV_CLK} = 58 KHz	17.6	20	21.8	
G_{LNA}		LNA_GAIN = 0x11; f_{DRV_CLK} = 58 KHz	11.6	12.5	14.2	
DR_{VIN_MIN}	Minimum receive input[1]	LOGAMP_DIS_FIRST=0x0;LOGAMP_DIS_LAST=0x0 LNA_GAIN=0x00; ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500KHz		2.4		µVrms
DR_{VIN_MAX}	Maximum receive input[1]			48		mVrms
SL_{AFE}	Slope of analog front end[2]	VOUT_SCALE_SEL = 0x0; f_{DRV_CLK} = 58 KHz	25	29.7	33	mV/dB
		VOUT_SCALE_SEL = 0x1; f_{DRV_CLK} = 58 KHz	38	45.1	46	
DR_{AFE}	Receiver path dynamic range (minimum to maximum input)[1]	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	82		92	dB
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1 ERR_{LOG} < ± 3dB; f_{DRV_CLK} < 500 KHz	59		70	
	Receiver path dynamic Range (noise floor to maximum input)[3]	LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0 ERR_{LOG} < ± 3 dB; f_{DRV_CLK} < 500 KHz	74		84	
BW_{LOG}	Logamp bandwidth	Information only	40		1000	KHz
INT_{LOG}	Intercept point in dBV	LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0; f_{DRV_CLK} = 40 KHz	-108		-97	dBV
		LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-94		-86	
		LOGAMP_DIS_FIRST = 0x1; LOGAMP_DIS_LAST=0x1; f_{DRV_CLK} = 40 KHz	-80		-70	
ERR_{LOG}	Log conformance error	Information only	-3		3	dB
f_{BPF}	Configurable range of center frequency of BPF	BPF_BYPASS = 0x0; BPF_FC_TRIM = 0x0; set by different values of BPF_HPF_FREQ	40		500	KHz
Q_{BPF}	Q of bandpass filter	BPF_BYPASS = 0x0; BPF_Q_SEL = 0x0[4]	3	4	5.2	
R_{LPF}	Internal resistor on FLT pin to ground			6.25		KΩ
V_{O_PDSTL}	Output pedestal level[1]	V_{VDD} = 3.3 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	0.3		0.45	V
		V_{VDD} = 5.0 V; f_{DRV_CLK} = 40 KHz; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0;LOGAMP_DIS_LAST = 0x0	0.45		0.675	

(1) Measured with effectively very large C_{FLT}. Actual minimum signal detectable will depend on $V_{N\_pk\_pk}$. Minimum and maximum input levels are defined by ERR_{LOG}.
(2) Slope measured with factory trim at f_{DRV_CLK} = 58 KHz. Slope can be adjusted with with LOGAMP_SLOPE_ADJ bits for different f_{DRV_CLK} settings.
(3) Measured with different C_{FLT} values according to Equation 3. Noise floor is set by $V_{N\_PK\_PK}$ in addition to V_{O_PDSTL}.
(4) Other choices of Q possible.

Product Folder Links: *TUSS4470*

Receiver Characteristics (continued)

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{N\_pk\_pk}$	Output peak-to-peak noise	V_{VDD}=3.3 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x0 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST=0x0	50		200	mVpp
		V_{VDD}=5.0 V; f_{DRV_CLK} = 40 KHz; C_{FLT} = 15 nF; VOUT_SCALE_SEL = 0x1 LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0	75		300	

6.8 Echo Interrupt Comparator Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT_SCALE_SEL = 0x0						
$V_{ECMP\_THR\_0}$	Echo interrupt comparator threshold[1]	ECHO_INT_THR_SEL = 0x0	0.37	0.4	0.43	V
		ECHO_INT_THR_SEL = 0x5	0.56	0.6	0.64	
		ECHO_INT_THR_SEL = 0xA	0.75	0.8	0.85	
		ECHO_INT_THR_SEL = 0xF	0.94	1	1.06	
$V_{ECMP\_HYS\_0}$	Echo interrupt comparator hysteresis			7	68	mV
VOUT_SCALE_SEL = 0x1						
$V_{E\_CMP\_THR\_1}$	Echo interrupt comparator threshold[1]	ECHO_INT_THR_SEL = 0x0	0.56	0.6	0.64	V
		ECHO_INT_THR_SEL = 0x5	0.84	0.9	0.96	
		ECHO_INT_THR_SEL = 0xA	1.13	1.2	1.27	
		ECHO_INT_THR_SEL = 0xF	1.41	1.5	1.59	
$V_{ECMP\_HYS\_1}$	Echo interrupt output threshold level hysteresis			7	68	mV

(1)   Other thresholds possibe.

6.9 Digital I/O Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH_DIGIO}	Digital input high-level	NCS, SDI, SCLK and IOx pins	0.7			V_{VDD}
V_{IL_DIGIO}	Digital input low-level				0.3	V_{VDD}
V_{HYS_DIGIO}	Digital input hysteresis		100			mV
V_{OH_DIGIO}	Digital output high-level[1]	SDO, OUTx pins; I_{DIGIO_OUT} = − 1 mA	$V_{VDD} - 0.1$			V
V_{OL_DIGIO}	Digital output low-level[1]	SDO, OUTx pins; I_{DIGIO_OUT} = 1 mA			0.1	V
V_{O_CAP}	Maximum output load capacitance	SDO pin. Information Only			10	pF
R_{PU_DIGIO}	Digital input pullup resistance to VDD	NCS, IO1, IO2 pins	80	100	130	kΩ
R_{PD_DIGIO}	Digital Input pulldown resistance to GND	SCLK, SDI pins	80	100	130	kΩ

(1)   No short-circuit protection on output pins. Damage may occur for currents higher than specified.

6.10 Switching Characteristics

over operating free-air temperature range, V_{VPWR}, V_{VDRV} and V_{VDD} recommended voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{DRV_CLK}	Frequency of drive clock at IO1 and IO2 pin ; depends on the VDRV voltage	Used as burst frequency; PRE_DRIVER_MODE = 0x0	40		1000	KHz
	Frequency of drive clock at IO1 and IO2 pin	Used as burst frequency; PRE_DRIVER_MODE = 0x1; Load cap on OUTA/OUTB = 2nF	40		440	KHz
SPI_{RATE}	SPI bit rate				500	KHz

6.11 Typical Characteristics

VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
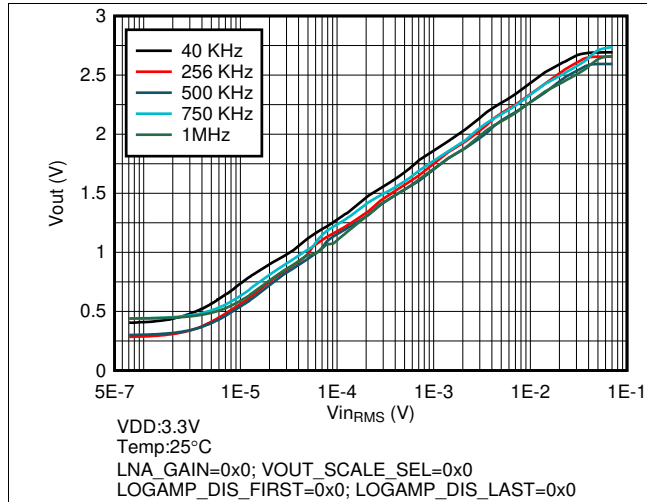
Figure 1. Receive Signal Path Transfer Function for VDD = 3.3 V

VDD:5.0V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x1
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
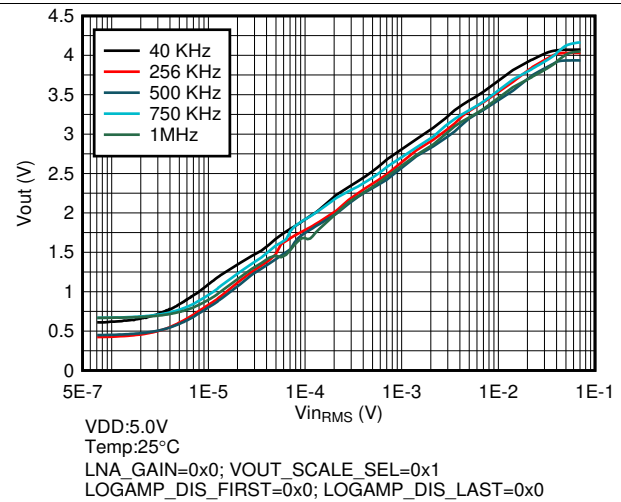
Figure 2. Receive Signal Path Transfer Function for VDD = 5 V

VDD:3.3V
F_C:256KHz
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
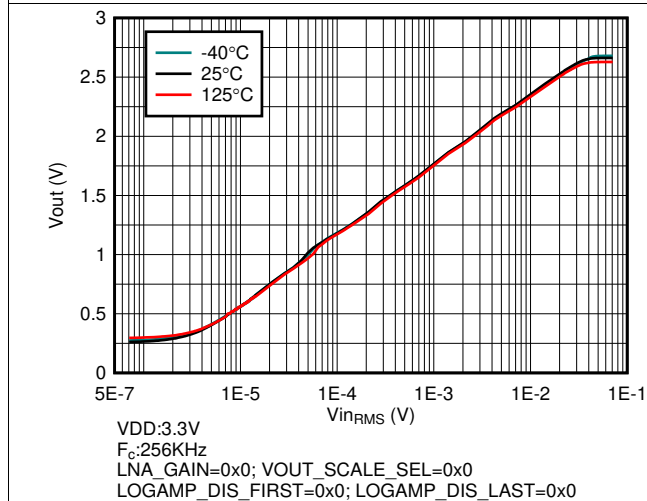
Figure 3. Receive Signal Path Transfer Function Across Temperature

VDD:3.3V; Temp:25°C
F_C:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
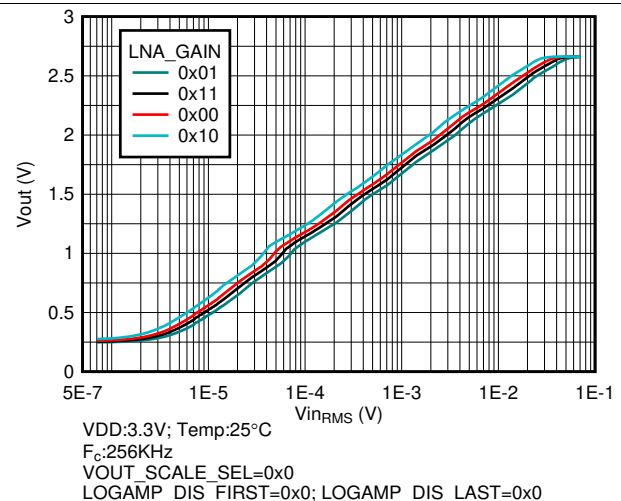
Figure 4. Receive Signal Path Transfer Function Across LNA Gain

VDD:3.3V
F_C:256KHz
Temp:25°C
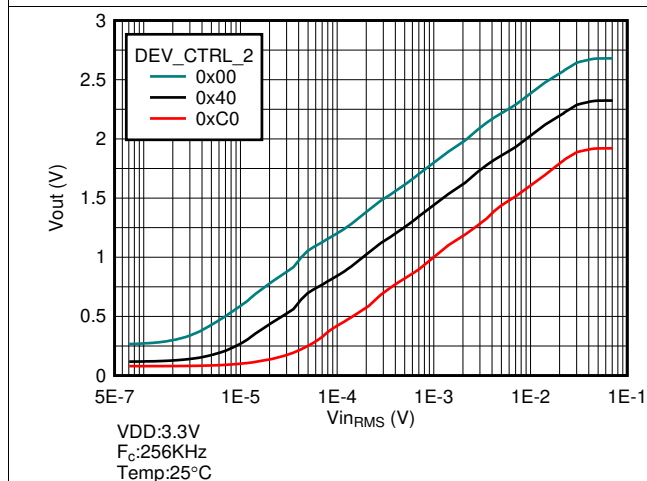
Figure 5. Receive Signal Path Transfer Function for Various Logamp Stages Disabled

LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
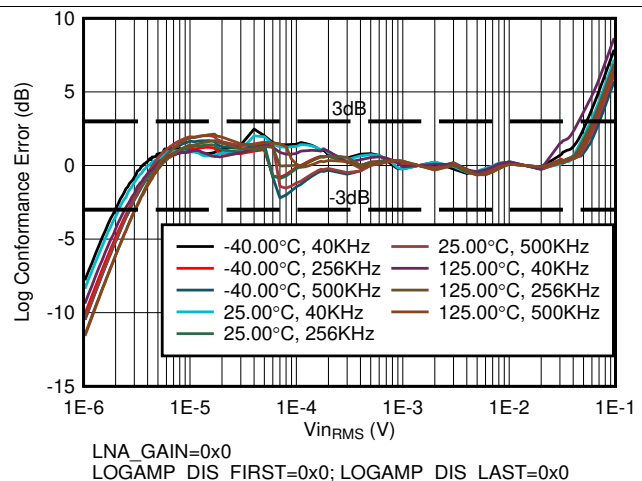
Figure 6. Receive Signal Path Log Conformance Error With All Stages Enabled

Product Folder Links: *TUSS4470*

Typical Characteristics (continued)

LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x1
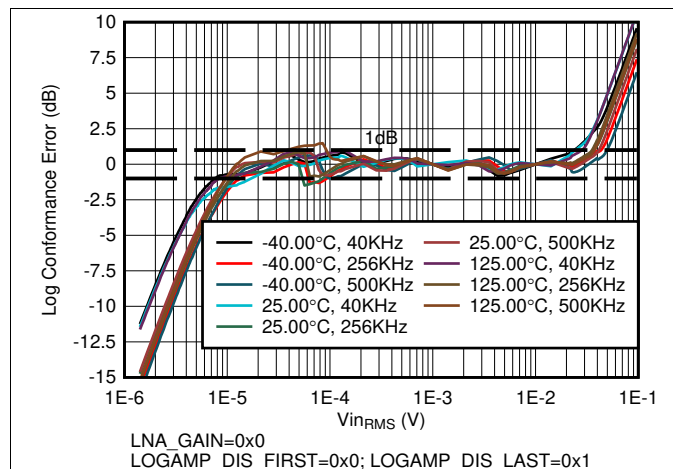
Figure 7. Receive Signal Path Log Conformance Error With Last Stage Disabled

LNA_GAIN=0x0
LOGAMP_DIS_FIRST=0x1; LOGAMP_DIS_LAST=0x1
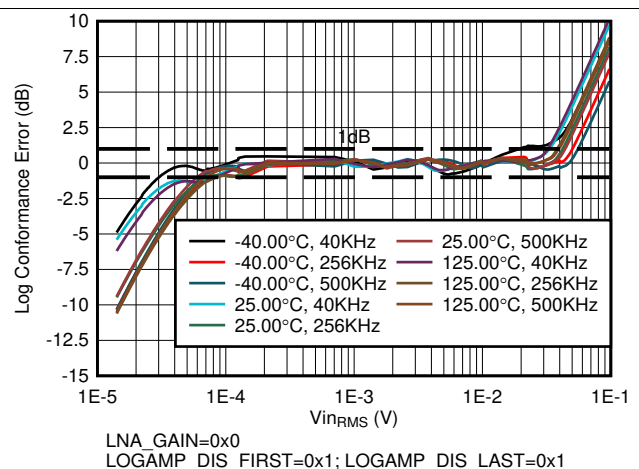
Figure 8. Receive Signal Path Log Conformance Error With First and Last Stage Disabled

VDD:3.3V
Temp:25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
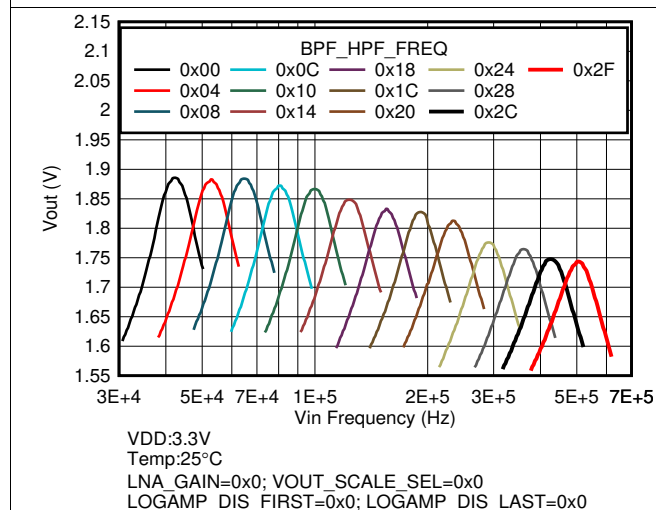
Figure 9. Receive Signal Path Bandpass Filter Transfer Function

LNA_GAIN=0x0;
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
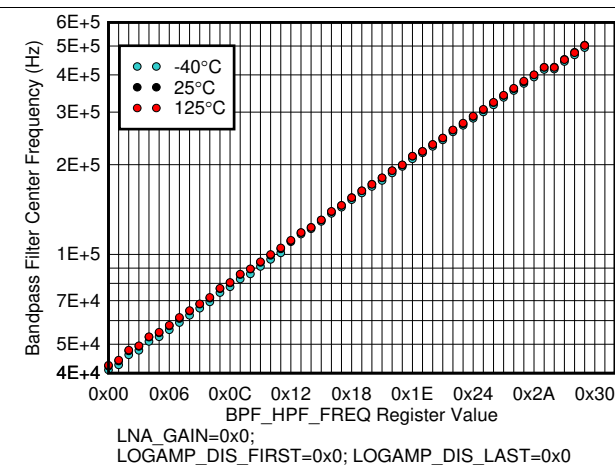
Figure 10. Receive Signal Path Bandpass Filter frequency for Various Register Settings

VDD=3.3V
Temp=25°C
LNA_GAIN=0x0; VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0
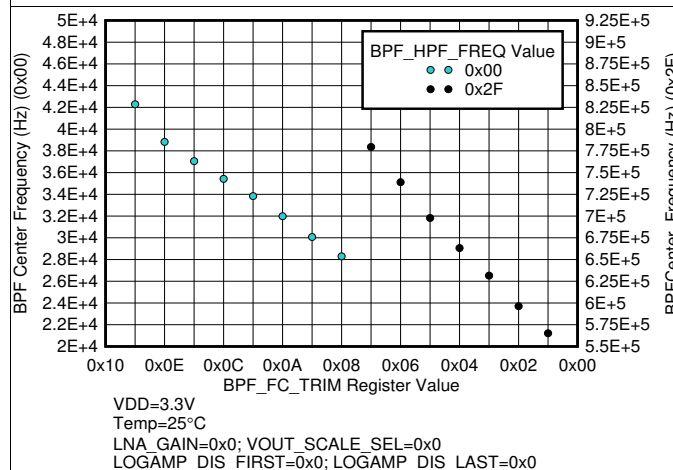
Figure 11. Receive Signal Path Bandpass Filter Center Frequency Trim
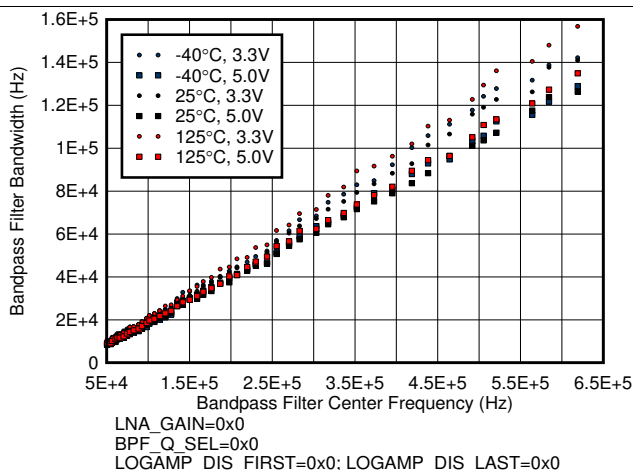

LNA_GAIN=0x0
BPF_Q_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 12. Receive Signal Path Bandpass Filter Bandwidth for Various Center Frequency Settings

Product Folder Links: *TUSS4470*

Typical Characteristics (continued)

VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 13. Receive Signal Path Transfer Function for Various Slope Adjustments

VDD:3.3V; Temp:25°C
F_c:256KHz
VOUT_SCALE_SEL=0x0
LOGAMP_DIS_FIRST=0x0; LOGAMP_DIS_LAST=0x0

Figure 14. Receive Signal Path Transfer Function for Various Intercept Adjustments

Product Folder Links: *TUSS4470*
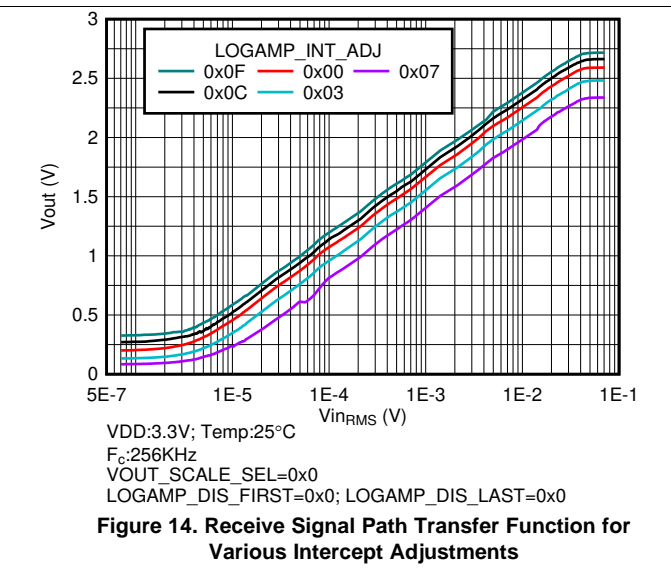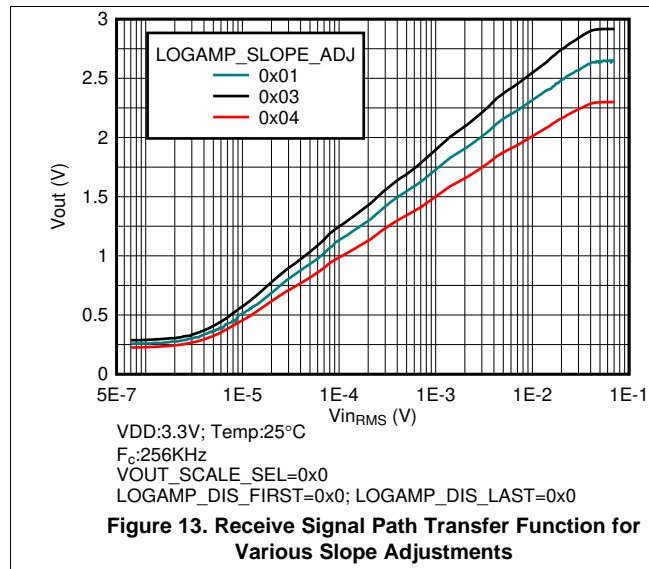
7 Detailed Description

7.1 Overview

The TUSS4470 is a highly integrated driver and receiver IC designed especially for ultrasonic transducers operating between the range of 40 KHz to 1 MHz. The TUSS4470 integrates an H-bridge to drive the transducer directly. This is useful in applications where the receive transducer sensitivity is high and large driving voltage is not required to create sufficient sound pressure level and where short distance measruements are needed. The driver stage has flexible and configurable controls set through the SPI interface or through digital input pins that can be driven by an external MCU. The receive stage consists of a logarithmic amplifier receive chain. The logamp enables the TUSS4470 to have a wide dynamic input range. This enables applications where objects with different physical properties must be detected with the same sensor. A key advantage of the TUSS4470 is that it integrates a bandpass filter that can be tuned to the center frequency of the transducer. A demodulated analog output representing the receive echo, the zero crossing of the input signal, and a simple threshold crossing indicator enable a variety of end applications from complex object detection to simple presence detection.

7.2 Functional Block Diagram
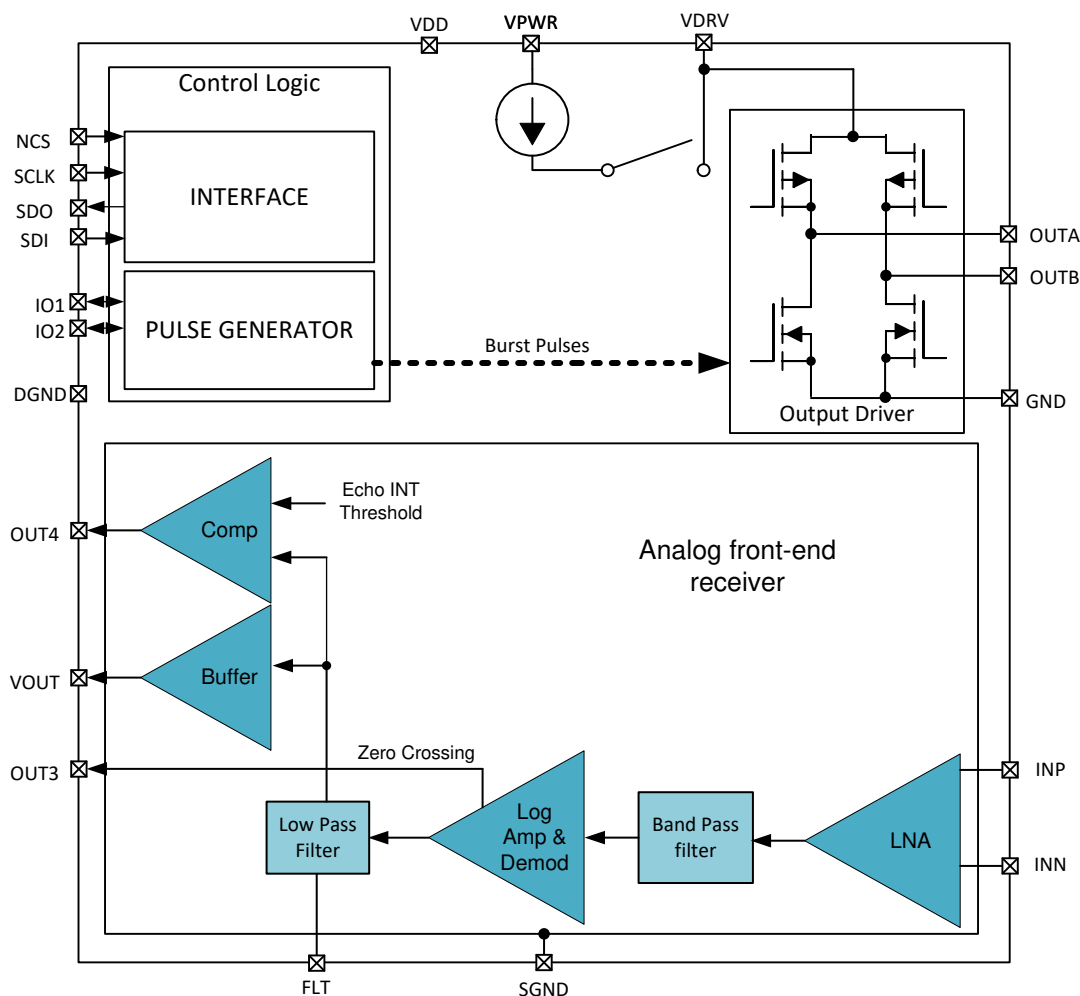
7.3 Feature Description

7.3.1 Excitation Power Supply (VDRV)

The TUSS4470 device includes a current source which charges a capacitor connected to the VDRV pin. The VDRV pin serves as the power supply for the integrated H-Bridge driver circuit The voltage on the VDRV pin (V_{VDRV}) is controlled by an internal voltage monitor which can be configured by the VDRV_VOLTAGE_LEVEL bits. The current source is switched off after VDRV pin voltage crosses the configured V_{VDRV} value. The charging current (I_{VDRV}) can be configured using VDRV_CURRENT_LEVEL bits.

In applications where VPWR can vary over a wide range, this allows the transducer drive voltage to be fixed for every burst for a deterministic sound pressure level created by the transducer. This is possible only when the minium supply voltage on the VPWR pin is greater than the configured value of V_{VDRV}.

The VDRV regulation is disabled at device power up indicated by VDRV_HI_Z bit being set. To enable VDRV this bit must be cleared. This feature enables applications where the the H-Bridge driver supply is connected to an external power supply source through the VDRV pin.

NOTE
- When VDRV pin is supplied from an external power supply, it must be ensured that all times including during power up, $V_{VPWR} > V_{VDRV} + 0.3$ V to prevent any reverse current from VDRV pin to VPWR pin. Alternatively a reverse current prevention diode can be used on VPWR pin as shown in Figure 25 (D1).
- Very fast ramp-up rate on VPWR pin should be avoided to prevent damage to the device. If fast ramp rates are possible, a series resistor between power supply and VPWR pin as shown in Figure 25 (R_{PWR}) is recommended.

After a burst is completed and during the long receive time (listen mode), the capacitor on VDRV pin will discharge causing the charging current to turn on intermittently. This can inject switching noise which can be picked by the analog front end as a spurious echo. To eliminate this noise, the DIS_VDRV_REG_LSTN bit can be set. This disables charging of VDRV automatically after the burst is done. The VDRV charging current can be turned on again by setting the VDRV_TRIGGER bit. Setting this bit may create a spurious echo which can be ignored by the echo processing in the MCU. The VDRV_READY bit in DEV_STAT register can be monitored to know when the required voltage level has been reached and the device is ready to generate a new burst. The VDRV_TRIGGER bit must be un-set through SPI just before the start of burst and will have to be set again for next charging cycle. If the VDRV_TRIGGER bit is not un-set before next burst cycle, the VDRV charging current will not be automatically disabled after the burst even when DIS_VDRV_REG_LSTN is set. This functionality is ignored when the VDRV_HI_Z bit is set.

7.3.2 Burst Generation

TUSS4470 has multiple modes to excite the transducer through OUTA and OUTB pins. For each of the modes, the desired frequency of burst is supplied through an external clock on the IOx pins. This enables the user to supply a highly precise clock calibrated to the center frequency of transducer to enable the highest sound pressure level generation. These modes can be selected by the IO_MODE bits in the DEV_CTRL_3 register.

The burst mode is enabled first, then the start of burst (OUTA/OUTB changing states) happens at the next falling edge of IO1 or IO2, depending on the mode selected. These modes are described below.
- **IO_MODE = 0:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled by setting the CMD_TRIGGER in the TOF_CONFIG register through SPI, as shown in Figure 15. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. The end of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent, or when the CMD_TRIGGER = 0 is set through SPI, whichever occurs earlier. TI recommends that IO2 is held high before burst enable to count the number of pulses correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins as shown in Table 22. A transition of CMD_TRIGGER from high to low to high again is required to initiate a new burst sequence.
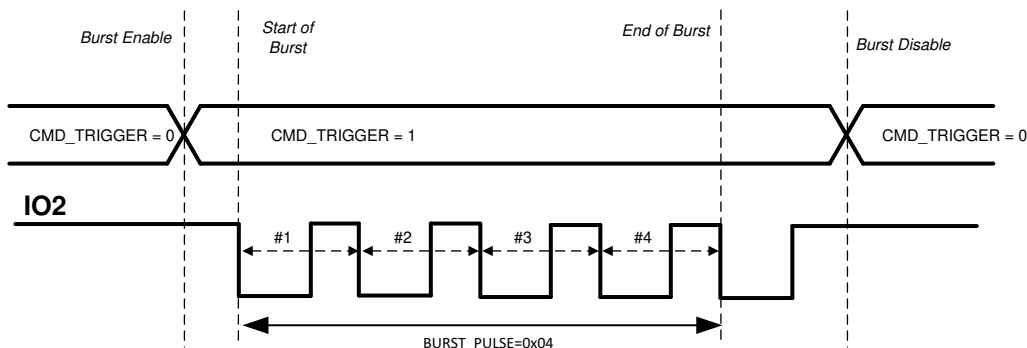
Feature Description (continued)

Figure 15. IO_MODE 0 Description

- **IO_MODE = 1:** In this mode, the external clock for the transducer is applied at the IO2 pin and the burst mode is enabled when IO1 pin transitions low as shown in Figure 16. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins. The start of burst happens from the first falling edge of IO2. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent or or IO1 transitions high, whichever occurs earlier. TI recommends that IO2 is held high before start of burst to count the number of pulse correctly. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins as shown in Table 22. A transition of IO1 from low to high to low again is required to initiate a new burst sequence.
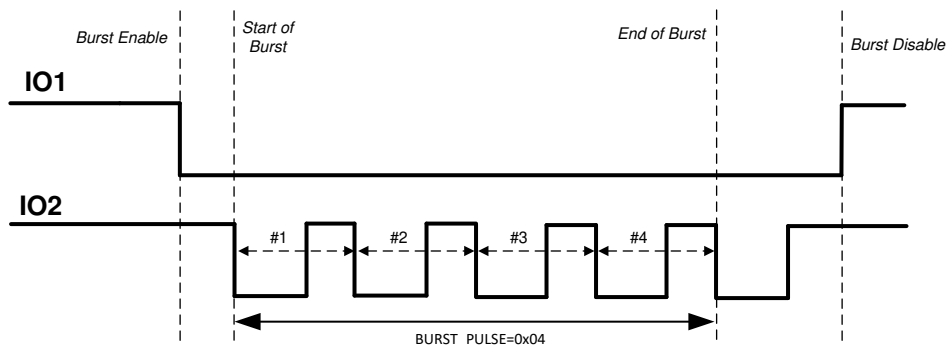

Figure 16. IO_MODE 1 Description

- **IO_MODE = 2:** In this mode both IO1 and IO2 are used to control OUTA and OUTB. The burst enable is triggered when either IO1 or IO2 transitions from high to low. Start of burst (OUTA and OUTB changing state) happens only at the next falling edge of IO1. Figure 17 shows the case where a high-to-low transition on IO2 is used to enable the burst. A burst is emulated when IO1 and IO2 are toggled in a non-overlapping sequence. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins as shown in Table 21. During a burst, if there is a condition where both IO1 and IO2 are high for more than half period of the internal clock f_{INT_CLK} (caused by differential delays due to PCB parasitics or MCU code), an end of burst and burst mode disable will be triggered. Any falling edge just after this condition will be ignored to toggle OUTA and OUTB as it would be considered as a new burst enable signal. A systematic condition of overlap can cause a continuos end of burst trigger such that OUTA and OUTB do not toggle even though IO1 and IO2 are toggling. TI recommends no overlap or minimum non-overlap between the IO1 and IO2 signals when measured at the pins. BURST_PULSE has no effect in this mode.
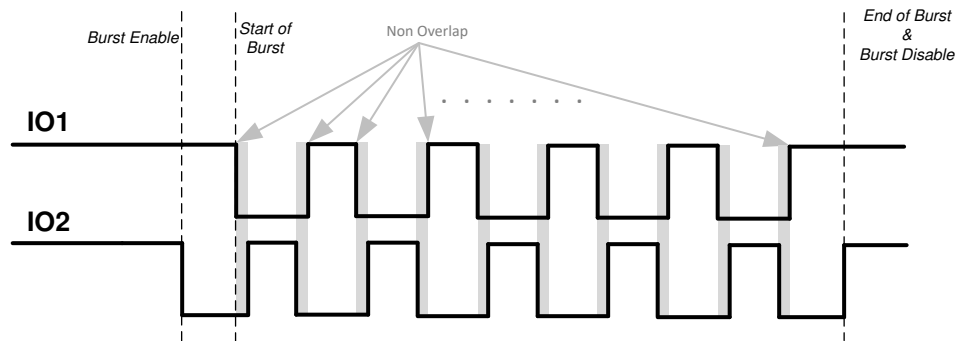
Feature Description (continued)

Figure 17. IO_MODE 2 Description

- **IO_MODE = 3:** In this mode, burst enable and start of burst are both triggered by the falling edge of IO2. TI recommends that IO2 pin is kept pulled up to VDD for this mode. The device then expects a clock at IO2 pin to generate pulses on the OUTA/OUTB pins as shown in Figure 18. The number of pulses are counted by counting falling edge to next falling edge transitions on IO2 once the start of burst is triggered. End of burst sequence is signaled when the number of pulses defined in BURST_PULSE are sent. After end of burst, a blank-out timer interval defined by the DRV_PLS_FLT_DT register is started to prevent triggering of a new start of burst in the event if the IO2 pin is still toggling. After the start of burst, the state of OUTA and OUTB pins are determined by IO1 and IO2 pins as shown in Table 22.
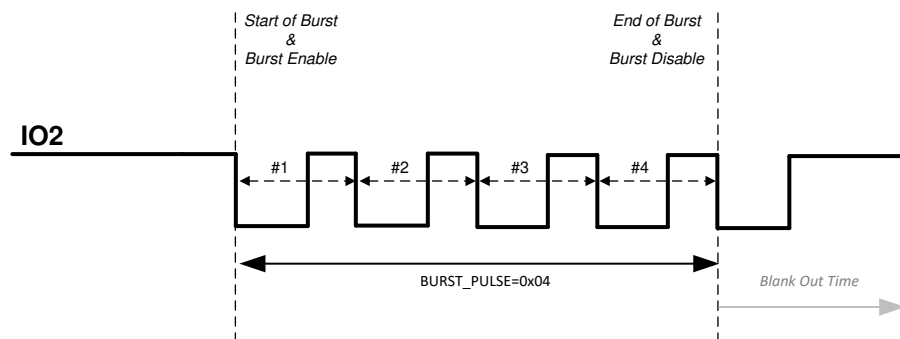
Figure 18. IO_MODE 3 Description

NOTE

- For IO_MODE 0 and 1, by setting BURST_PULSE = 0, the device will generate continuos burst pulses on OUTA and OUTB until the end of burst is signaled through SPI or the IO1 pin, respectively. Continuos bursting is not available for IO_MODE=3.
- A higher noise floor at the VOUT pin is expected in continuous mode where one transducer is used to transmit burst signals and another transducer is used to receive, as the switching noise of the digital IO pins can couple into the highly sensitive analog front end for the receive channel. This also applies to the single transducer use case where a continuous clock is applied on IO2 pin when the device is in indirect or listening mode.
- The range for frequency of switching for the output drivers is given by f_{DRV_CLK} parameter in the *Switching Charactestics* table.
- When the device is not in direct sensing or bursting mode, the device is always in indirect sensing or listening mode.

Feature Description (continued)

7.3.2.1 Burst Generation Diagnostics

In IO_MODE 0, 1 and 3, a pulse number diagnostic is active after start of burst (not when the burst is enabled) to monitor if the correct number of pulses (as set in BURST_PULSE) were generated before the end of burst was signaled through SPI or the IO1 pin. A fault, if detected, is then reported through the PULSE_NUM_FLT bit.

The pulse duration after start of burst (not when the burst is enabled) is monitored to detect a stuck condition, which will keep the FETs on OUTA or OUTB turned on. This can happen because of loss of external clock or the driving signal on IO1 and IO2 pins being stuck in one state. The device expects to see a toggle on IOx pins (based on IO_MODE) within the time period as defined in the DRV_PLS_FLT_DT register. If this diagnostic triggers, it will force an end of burst. The fault is reported by setting the DRV_PULSE_FLT bit. If a DRV_PULSE_FLT is set in IO_MODE 0, 1 and 3—and the programmed number of pulses were not sent before end of burst—the PULSE_NUM_FLT will also be set.

NOTE
- The DRV_PULSE_FLT bit is cleared when a new start of burst is triggered, when DRV_PLS_FLT_DT = 0x7 is set, or if the device is put into Standby or Sleep mode.
- The PULSE_NUM_FLT bit is cleared when a new start of burst is triggered, or if the device is put into Standby or Sleep mode.

7.3.3 Direct Transducer Drive

Figure 19 shows the internal structure for driving an ultrasonic transducer connected directly to the device output using an H-bridge output stage. This configuration drives $2 \times V_{VDRV}$ as the peak-to-peak voltage across the transducer. The voltage on VDRV pin can be set as described in the *Excitation Power Supply (VDRV)* section.
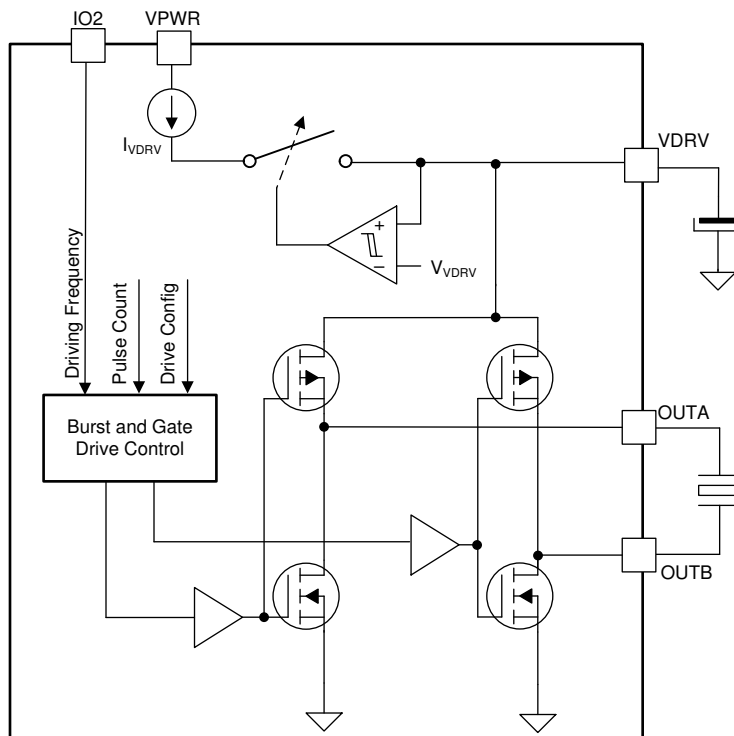
Figure 19. Direct Drive Configuration Using Internal FETs

Figure 19 shows the most common application case for the TUSS4470 device, in which the output driver pulses the two half-bridges out-of-phase. It is also possible to use the driver in half-bridge mode by setting the HALF_BRG_MODE bit. In this mode, only V_{VDRV} is applied across the transducer. This mode is useful for transducers where one side of the membrane must be always grounded.

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Feature Description (continued)

The device can also be configured as a pre-driver to drive external FETs or BJTs to drive higher current and voltage into the primary side of the transformer, as shown in Figure 20, by setting the PRE_DRIVER_MODE bit. The high-side and low-side devices are used to drive the external low-side drivers. The VDRV voltage level can be configured to ensure that the OUTA and OUTB voltages do not violate the V_{GS} or V_{BE} specification for external the FET or BJT, respectively. In the configuration shown in Figure 20, it is possible to use a voltage (VBOOST) which is higher than the supply of the system for generating higher voltage across the transducer.

Refer to the *Application and Implementation* section for an application diagram and information on how the polarity and state of OUTA and OUTB pins are defined with respect to IO1 and IO2 pin states and other register settings.

Figure 20. Center-Tap Transformer Drive Using External FETs

Feature Description (continued)

7.3.4 Analog Front End
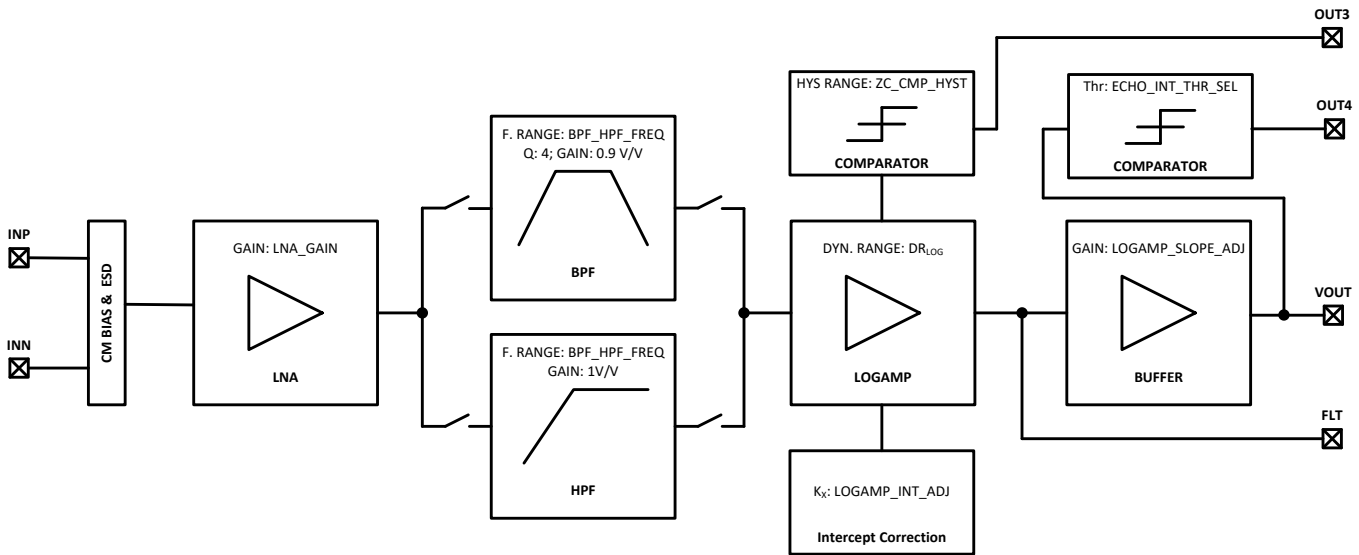

Figure 21. TUSS4470 Analog Front-End Block Diagram

Figure 21 shows the analog front-end block diagram that can receive and condition the signals from the transducer during listen mode. The received echo is first amplified with a fixed linear low-noise amplifier, followed by either a bandpass filter or a high-pass filter to remove noise out of the expected signal band. After filtering the signal, the signal is fed into a logarithmic amplifier. The output of the logarithmic amplifier is then buffered to the VOUT pin. In Figure 21, every block has the register name associated with it that can be used to configure the signal path. The final equation for the signal path is given by Equation 2:

$$V_{OUT} = G_{VOUT} \cdot SL_{LOG} \cdot 20 \log_{10}\left(\frac{G_{LNA} \cdot G_{BPF} \cdot V_{IN}}{INT_{LOG} \cdot K_X}\right)$$

where

- G_{VOUT} is set by the LOGAMP_SLOPE_ADJ bits.
- SL_{LOG} is slope of logarithmic amplifier as specified in the *Receiver Characterstics* table.
- G_{LNA} is set by the LNA_GAIN bits.
- G_{BPF} is typically 0.9V/V.
- V_{IN} is the input V_{INP}
- INT_{LOG} is logarithmic amplifier intercept specified in the *Receiver Characterstics* table.
- K_X is the log intercept adjustment set by the LOGAMP_INT_ADJ bits. (1)

The bandpass filter is critical for reducing noise to allow utilization of the complete dynamic range of the logarithmic amplifier. The center frequency of the bandpass filter can be configured to be close the transducer frequency which is set by the BPF_HPF_FREQ bits. Table 1 shows the nominal values for the BPF center frequency corresponding to the BPF_HPF_FREQ register value. The TUSS4470 supports a wide range of frequencies, therefore a factory trim is used to remove process variation for a particular pre-determined frequency. It is possible that all other frequencies listed in Table 1 do not correspond exactly to value of BPF_HPF_FREQ in a factory trim. The user can vary the value of the BPF_HPF_FREQ register around the desired center frequency while actively bursting and observing the VOUT signal. The value with maximum voltage at VOUT pin will the desired setting for the BPF_HPF_FREQ register.

Table 1. Bandpass Filter Center Frequency Configuration

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F$_c$ (KHz)
0x00	40.64

Feature Description (continued)

Table 1. Bandpass Filter Center Frequency Configuration (continued)

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F$_c$ (KHz)
0x01	44.05
0x02	45.6
0x03	18.86
0x04	50.58
0x05	52.96
0x06	56.75
0x07	60.11
0x08	62.95
0x09	66.68
0x0A	71.44
0x0B	74.81
0x0C	79.24
0x0D	82.03
0x0E	86.89
0x0F	92.04
0x10	97.49
0x11	103.27
0x12	109.4
0x13	114.54
0x14	121.33
0x15	128.52
0x16	134.58
0x17	142.55
0x18	151.01
0x19	159.94
0x1A	167.48
0x1B	177.41
0x1C	185.77
0x1D	196.78
0x1E	206.05
0x1F	218.26
0x20	228.54
0x21	244.89
0x22	256.43
0x23	271.63
0x24	284.43
0x25	301.28
0x26	319.13
0x27	338.14
0x28	353.97
0x29	374.95
0x2A	397.16
0x2B	408.17
0x2C	420.7
0x2D	455.63

Product Folder Links: *TUSS4470*

Feature Description (continued)

Table 1. Bandpass Filter Center Frequency Configuration (continued)

BPF_HPF_FREQ (HEX) (BPF_FC_TRIM_FRC = 0)	BPF_F$_c$ (KHz)
0x2E	472.03
0x2F	500

The factory trim can be overridden by setting the BPF_FC_TRIM_FRC bit first and varying the BPF_FC_TRIM bit after. This is useful in two ways:
- If the factory trimmed bandpass filter center frequency is higher than the desired value for BPF_HPF_FREQ = 0x00, or lower than desired value for BPF_HPF_FREQ = 0x2F, then BPF_FC_TRIM can be used to recover the range.
- This setting can also be used to extend the frequency range of the bandpass filter center frequency.

The BPF_FC_TRIM acts like an offset on top of the BPF_HPF_FREQ setting. Table 2 shows the nominal value of center frequency when this offset is added to the minimum and maximum BPF_HPF_FREQ code. Measured data is shown in Figure 11. For BPF_HPF_FREQ values greater than 0x08 and less than 0x27, varying BPF_FC_TRIM keeping BPF_HPF_FREQ fixed is the same as setting BPF_FC_TRIM = 0x00 and varying BPF_HPF_FREQ to find the optimum setting.

Table 2. Bandpass Filter Center Frequency Range Extension

BPF_HPF_FREQ (hex) + BPF_FC_TRIM (hex) (BPF_FC_TRIM_FRC = 1)	BPF_F$_c$ (KHz)
0x00 + 0x8	27.48
0x00 + 0x9	29.44
0x00 + 0xA	30.83
0x00 + 0xB	31.19
0x00 + 0xC	32.65
0x00 + 0xD	34.19
0x00 + 0xE	35.8
0x00 + 0xF	38.81
0x2F + 0x1	523.56
0x2F + 0x2	554.59
0x2F + 0x3	587.45
0x2F + 0x4	622.23
0x2F + 0x5	651.58
0x2F + 0x6	690.19
0x2F + 0x7	731.09

NOTE
- The Q factor of the filter is specified in the Receiver Characterstics table, and can be selected by the BPF_Q_SEL bits.
- The bandpass filter can also be converted into a high-pass filter by setting the BPF_BYPASS bit for transducer frequencies in the range above what is shown in Table 1. The corner frequency for high-pass filter is also controlled by the BPF_HPF_FREQ bits.
- BPF_Q_SEL and BPF_FC_TRIM have no effect when BPF_BYPASS = 1.

The logamp provides compression for large signal inputs and amplifies linearly small signal inputs. Logamp simplifies system design to detect varying strengths of echoes that happens because of difference in reflectivity of different types of objects and objects at different distances. It automatically adjusts its gain based on the input signal level. The logamp also demodulates the incoming signal.

The logamp consists of multiple gain stages and range extension stages that are combined to give a logarithmic response. The current consumption of the device can be reduced by turning off the either the first stage, the last stage of the logamp, or both, by setting the LOGAMP_DIS_FIRST and LOGAMP_DIS_LAST bits. Disabling the stages will reduce the input dynamic range on the lower side of the range as shown in Figure 4. The pedestal noise floor will be lower because the gain stages are disabled, but the minimum detectable signal value becomes higher due to the reduced dynamic range. Depending on the received input signal strength, stages can be disabled to get optimum object detection. For very small inputs, all stages should be enabled to get maximum input dynamic range even though the noise floor is higher. Figure 6, Figure 7, and Figure 8 show the effect on the log conformance error when all stages are enabled, when the last stage is disabled, and when both first and last stages are disabled. When stages are disabled, a lower error is obtained with a lower noise floor, but the input dynamic range is reduced.

At the output of the logamp, the user can apply an adjustment to the intercept of the logamp curve. This is denoted by the K_X factor in Equation 1. The intercept adjustment is controlled by the LOGAMP_INT_ADJ bits. The nominal values of K_X factor corresponding to register values is shown in Table 3, and its effect on the transfer function is shown in Figure 14.

Table 3. Logamp Intercept Adjustment

LOGAMP_INT_ADJ	K_X
0x00	1
0x01	1.155
0x02	1.334
0x03	1.54
0x04	1.778
0x05	2.054
0x06	2.371
0x07	2.738
0x08	1
0x09	0.931
0x0A	0.866
0x0B	0.806
0x0C	0.75
0x0D	0.698
0x0E	0.649
0x0F	0.604

The output of the logamp is filtered using a low-pass filter to remove the high-frequency components and provide a sufficient peak hold time for the demodulated envelope signal. The cut-off frequency of the low-pass filter is set by the internal impedance of the FLT pin and the value of an external capacitor connected to the pin. As this filter capacitance (C_{FLT}) suppresses the high frequency fluctuations, it also slows down the response time of the logamp. Higher C_{FLT} capacitance will result in lower peak-to-peak voltage variations at VOUT, and slower rise and fall times for the VOUT voltage to reach its maximum value for a given input signal. A nominal value can be calculated using Equation 3, and must be optimized depending on the application.

The output of the low-pass filter is buffered to the VOUT pin using an internal buffer. The buffer is designed to support an ADC input of a MCU. It is possible to change output dynamic range of the VOUT buffer using the VOUT_SCALE_SEL bit. Once the range is set, the gain of the VOUT buffer can be set by the LOGAMP_SLOPE_ADJ bits. The slope variation of the receiver analog front end is show in Figure 13.

Echo interrupt signal is available on the OUT4 pin that goes high when the signal on the VOUT pin crosses a threshold as defined by the ECHO_INT_THR_SEL bits. As long as the VOUT signal is higher than this threshold, the echo interrupt signal is held high. The signal goes low asynchronously when the VOUT signal drops below the programmed threshold. This signal can be used to interrupt a MCU when an object has been detected. The threshold value is also dependent on the setting of the VOUT_SCALE_SEL bit.

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A zero-crossing signal is output at the OUT3 pin which can be used to validate the frequency of the received echo signal to provide robustness against interference from other signals. This zero-crossing signal is derived from the raw amplified input signal from a particular stage as it is being demodulated in the logamp block. This function is disabled at device power up. but can be enabled by setting the ZC_CMP_EN bit. When enabled, the ZC_CMP_STG_SEL bits are used to select which logamp gain stage is used to generate the zero crossing signal while the ZC_CMP_HYST bits control the hysteresis of the zero-crossing comparator. The stage selection to see the OUT3 pin toggling depends on the strength of signal received by the logamp and has to be configured depending on the application. For large amplitude of input signal, a lower stage of the logamp should be selected, whereas for lower amplitude signal, a higher stage should be selected. To avoid switching noise generated by the toggling of the zero-crossing comparator when the ZC_EN_ECHO_INT bit is set, the zero-crossing output will be only enabled while the echo interrupt signal is high.

7.4 Device Functional Modes

The device has four functional modes:

Sleep Mode Ultra-low current consumption sleep mode

>In this mode, all major blocks of the device are disabled, including VDRV regulation. The SPI interface is still active. This transition into and out of this mode is done using the SLEEP_MODE_EN register bit. Upon issuing a command to exit this mode, the device transitions to other modes only when the VDRV pin reaches the programmed regulation voltage.

Standby Mode Low current standby mode

>In this state, the VDRV regulation is active, but other analog blocks are shut down to reduce quiescent current consumption. The STDBY_MODE_EN bit is used to enter and exit this mode through SPI. The device can transition very quickly from this state to one of the active states for bursting and listening.

Listen Mode   Default mode of the device

>This is the default mode of the device when it is not in Sleep mode or Standby mode. In this mode, there is no activity on the transmitter block and the device is actively listening for any ultrasonic signals.

Burst Mode Mode in which the device is enabled to start a burst to drive the transducer

>In this mode, the transmitter blocks are active and enabled to drive the transducer depending on when the start of burst occurs. The receiving path is also active at the same time listening for signals at the input. This mode is entered when a burst enable event occurs and exited when an end of burst occurs as described in *Burst Generation* section.

Figure 22 shows an example of the transitions between the different modes of the device for IO_MODE = 0, where the burst is activated through a SPI command and end of burst occurs as the number of programmed pulses are sent.
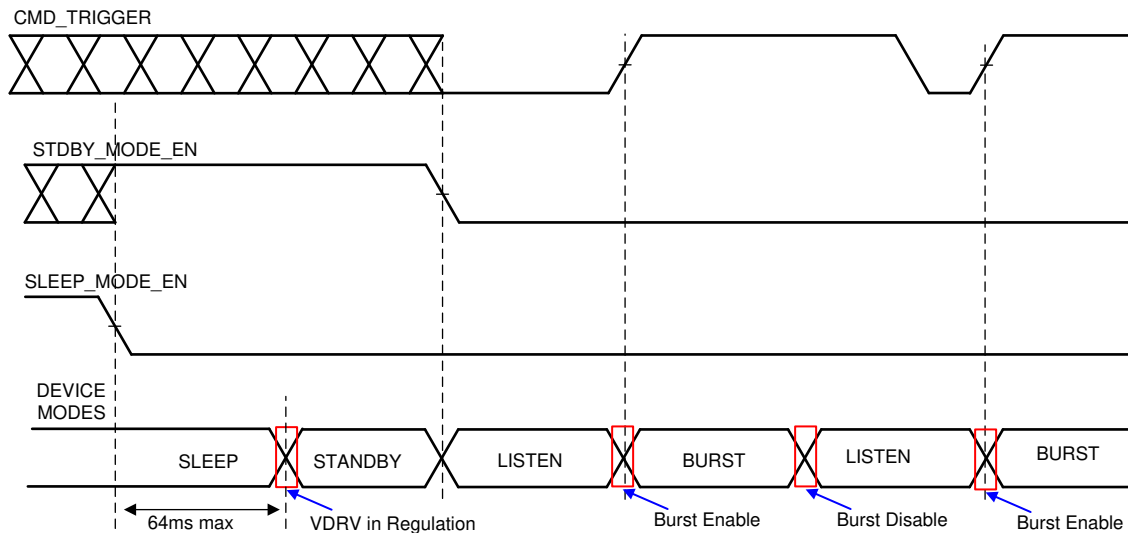
Device Functional Modes (continued)

Figure 22. Device Modes Timing Diagram

NOTE

- The transition to standby or active mode (listen or burst) from power-up or sleep mode is done only once the VDRV voltage crosses the programmed VDRV_VOLTAGE_LEVEL bit, or is higher 64 ms, whichever occurs earlier.
- In the case when VDRV is disabled, the device immediately transitions from power or sleep mode to standby and active modes.

7.5 Programming

The primary communication between the IC and the external MCU is through an SPI bus that provides full-duplex communications in a master-slave configuration. The external MCU is **always** a SPI master that sends command requests on the SDI pin and receives device responses on the SDO pin. The device is **always** a SPI slave device that receives command requests and sends responses to the external MCU over the SDO line. The following lists the characteristics of the SPI:

- The SPI is a 4-pin interface.
- The frame size is 16 bits and is assigned as follows:

Master-to-slave (MCU to TUSS4470 over the SDI line) 1 RW bit, 6 bits for the register address, 1 ODD parity bit for entire SPI frame, 8 bits for data

Slave-to-master (TUSS4470 to MCU over the SDO line) 1 bit for Master Parity error reporting during previous frame reception, 6 bits for the status, 1 bit for ODD parity for entire SPI frame, 8 bits for data

- SPI commands and data are shifted with the MSB first and the LSB last.
- The SDO line is sampled on the falling edge of the SCLK pin.
- The SDI line is shifted out on the rising edge of the SCLK pin.

The SPI communication begins with the NCS falling edge and ends with the NCS rising edge. The NCS high-level maintains the SPI slave-interface in the RESET state. The SDO output is in the tri-state condition.

The SPI does not support *back-to-back* SPI frame operation. After each SPI transfer the NCS pin must go from low to high before the next SPI transfer can begin.

Figure 23 shows an overview of a complete 16-bit SPI frame.

Product Folder Links: *TUSS4470*
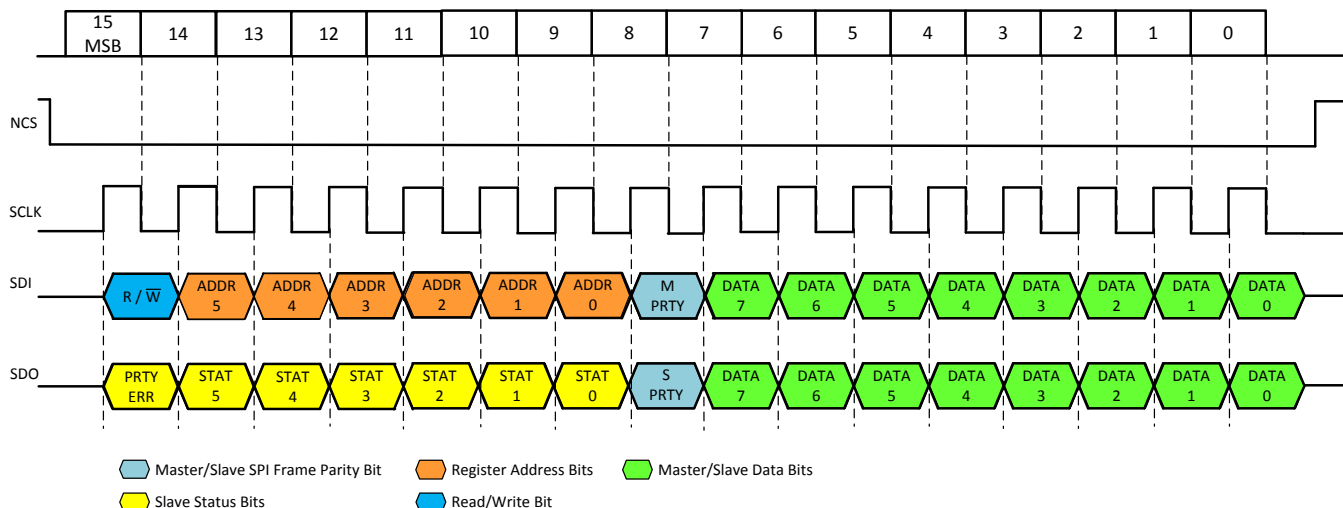
Programming (continued)

Figure 23. 16-Bit SPI Frame

Figure 24 shows a SPI transfer sequence between the master and the slave TUSS4470 device. When the master is writing a SPI frame, the parity error bit indicates if there was a parity error for the previous frame. When the master is transmitting the data for the SPI write, the slave echoes back register address that was sent just before in the command.
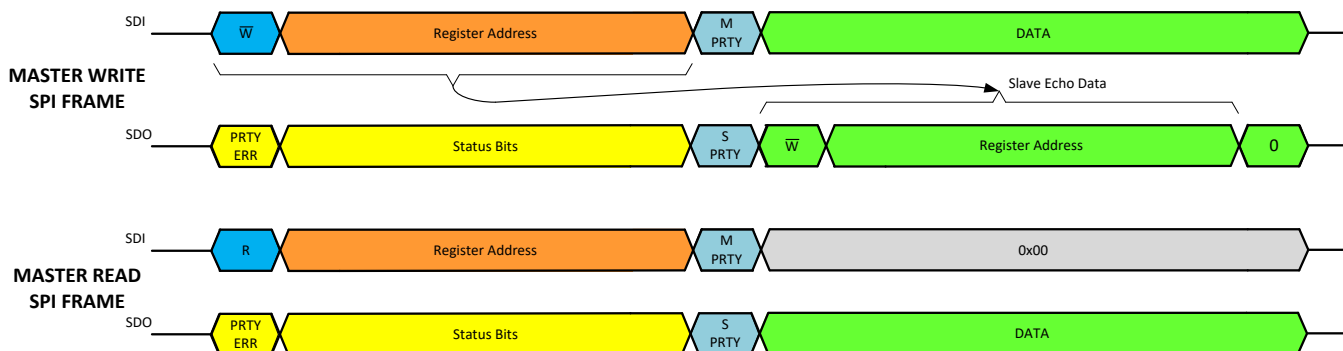
Figure 24. SPI Transfer Sequence

The status bits are defined in Table 4:

Table 4. SPI Interface Status Bits Description

STATUS BIT	DESCRIPTION
STAT 5 - VDRV_READY	Set when VDRV power regulator has reached the programmed voltage level. This is also indicated by VDRV_READY bit.
STAT 4- PULSE_NUM_FLT	Set if the burst sequence was terminated before completing the pulse number selected. This is also indicated by PULSE_NUM_FLT bit.
STAT 3 - DRV_PULSE_FLT	Set if there is a "stuck" fault detected during pulsing in a burst sequence. This is also indicated by DRV_PULSE_FLT
STAT 2 - EE_CRC_FLT	Set if there is a CRC Error when loading internal EEPROM memory. This is also indicated by EE_CRC_FLT bit.
STAT <1:0> - DEV_STATE	Device State: 00 - LISTEN 01 - BURST 10 - STANDBY 11 - SLEEP

Product Folder Links: TUSS4470

7.6 Register Maps

This section lists the REG_USER registers that are part of the volatile memory that can be configured by the MCU at power up or any time during the operation of the device. For register bits that are marked reserved, their reset value should not be changed.

7.6.1 REG_USER Registers

Table 5 lists the REG_USER registers. All register offset addresses not listed in Table 5 should be considered as reserved locations and the register contents should not be modified.

Table 5. REG_USER Registers

Address	Acronym	Register Name	Section
0x10	BPF_CONFIG_1	Bandpass filter settings	Go
0x11	BPF_CONFIG_2	Bandpass filter settings	Go
0x12	DEV_CTRL_1	Log-amp configuration	Go
0x13	DEV_CTRL_2	Log-amp configuration	Go
0x14	DEV_CTRL_3	Device Configuration	Go
0x16	VDRV_CTRL	VDRV Regulator Control	Go
0x17	ECHO_INT_CONFIG	Echo Interrupt Control	Go
0x18	ZC_CONFIG	Zero Crossing configuation	Go
0x1A	BURST_PULSE	Burst pulse configuration	Go
0x1B	TOF_CONFIG	Time of Flight Config	Go
0x1C	DEV_STAT	Fault status bits	Go
0x1D	DEVICE_ID	Device ID	Go
0x1E	REV_ID	Revision ID	Go

Complex bit access types are encoded to fit into small table cells. Table 6 shows the codes that are used for access types in this section.

Table 6. REG_USER Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.6.1.1 BPF_CONFIG_1 Register (Address = 0x10) [reset = 0x0]

BPF_CONFIG_1 is shown in Table 7.

Return to the Summary Table.

Table 7. BPF_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BPF_FC_TRIM_FRC	R/W	0x0	Override factor settings for Bandpass filter trim and control via BPF_FC_TRIM register. Valid only when BPF_BYPASS = 0 0x0 = Factory trim 0x1 = Override Factory trim
6	BPF_BYPASS	R/W	0x0	Select between Bandpass filter or high pass filter 0x0 = BPF Enabled 0x1 = HPF Enabled (BPF Bypass)

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Table 7. BPF_CONFIG_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	BPF_HPF_FREQ	R/W	0x0	If BPF_BYPASS = 0: Band pass filter center frequency. See "Bandpass filter center frequency configuration" table If BPF_BYPASS = 1: High pass filter corner frequency 0x00 - 0x0F - 200kHz 0x10 - 0x1F - 400kHz 0x20 - 0x2F - 50kHz 0x30 - 0x3F - 100kHz

7.6.1.2 BPF_CONFIG_2 Register (Address = 0x11) [reset = 0x0]

BPF_CONFIG_2 is shown in Table 8.

Return to the Summary Table.

Table 8. BPF_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:4	BPF_Q_SEL	R/W	0x0	Bandpass filter Q factor. Valid only when BPF_BYPASS = 0 0x0 = 4 0x1 = 5 0x2 = 2 0x3 = 3
3:0	BPF_FC_TRIM	R/W	0x0	Offset BPF_HPF_FREQ when BPF_FC_TRIM_FRC = 1: BPF_HPF_FREQ = BPF_HPF_FREQ + BPF_FC_TRIM See "Bandpass filter center frequency range extension" table.

7.6.1.3 DEV_CTRL_1 Register (Address = 0x12) [reset = 0x0]

DEV_CTRL_1 is shown in Table 9.

Return to the Summary Table.

Table 9. DEV_CTRL_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_FRC	R/W	0x0	Override for factory settings for LOGAMP_SLOPE_ADJ and LOGAMP_INT_ADJ
6:4	LOGAMP_SLOPE_ADJ	R/W	0x0	Slope or gain adjustment at the final output on VOUT pin. Slope adjustment depends on the setting of VOUT_SCALE_SEL. $0x0 = 3.0 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.56 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x1 = 3.1 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.71 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x2 = 3.2 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.86 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x3 = 3.3 \times \overline{\text{VOUT\_SCALE\_SEL}} + 5.01 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x4 = 2.6 \times \overline{\text{VOUT\_SCALE\_SEL}} + 3.94 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x5 = 2.7 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.10 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x6 = 2.8 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.25 \times \text{VOUT\_SCALE\_SEL}$ V/V $0x7 = 2.9 \times \overline{\text{VOUT\_SCALE\_SEL}} + 4.4 \times \text{VOUT\_SCALE\_SEL}$ V/V
3:0	LOGAMP_INT_ADJ	R/W	0x0	Logamp Intercept adjustment. See "Logamp intercept adjustment" table in specification for values.

7.6.1.4 DEV_CTRL_2 Register (Address = 0x13) [reset = 0x0]

DEV_CTRL_2 is shown in Table 10.

Return to the Summary Table.

Table 10. DEV_CTRL_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOGAMP_DIS_FIRST	R/W	0x0	Disable first logamp stage to reduce quiescent current
6	LOGAMP_DIS_LAST	R/W	0x0	Disable last logamp stage quiescent current
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	VOUT_SCALE_SEL	R/W	0x0	Select VOUT scaling 0x0 = Select Vout gain to map ouput to 3.3 V 0x1 = Select Vout gain to map output to 5.0 V
1:0	LNA_GAIN	R/W	0x0	Adjust LNA Gain in V/V 0x0 = 15 V/V 0x1 = 10 V/V 0x2 = 20 V/V 0x3 = 12.5 V/V

7.6.1.5 DEV_CTRL_3 Register (Address = 0x14) [reset = 0x0]

DEV_CTRL_3 is shown in Table 11.

Return to the Summary Table.

Table 11. DEV_CTRL_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6:5	RESERVED	R/W	0x0	Reserved
4:2	DRV_PLS_FLT_DT	R/W	0x0	Driver Pulse Fault Deglitch Time. In IO_MODE = 0 or IO_MODE = 1, DRV_PULSE_FLT will be set if start of burst is triggerd and IO2 pin has not toggled for greater than deglitch Time. In IO_MODE = 2, DRV_PULSE_FLT will be set if start of burst is triggerd and if IO1 or IO2 do not toggle a period longer than the deglitch time except when both pins are high. 0x0 = 64 µs 0x1 = 48 µs 0x2 = 32 µs 0x3 = 24 µs 0x4 = 16 µs 0x5 = 8 µs 0x6 = 4 µs 0x7 = Check Disabled
1:0	IO_MODE	R/W	0x0	Configuration for low voltage IO pins. 0x0 = IOMODE 0 0x1 = IOMODE 1 0x2 = IOMODE 2 0x3 = IOMODE 3

7.6.1.6 VDRV_CTRL Register (Address = 0x16) [reset = 0x20]

VDRV_CTRL is shown in Table 12.

Return to the Summary Table.

Table 12. VDRV_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	DIS_VDRV_REG_LSTN	R/W	0x0	Automatically disable VDRV charging in listen mode every time after burst mode is exited given VDRV_TRIGGER =0x0. 0x0 = Do not automatically disable VDRV charging 0x1 = Automatically disable VDRV charging
5	VDRV_HI_Z	R/W	0x1	Turn off current source between VPWR and VRDV and disable VDRV regulation. 0x0 = VDRV not HiZ 0x1 = VDRV in HiZ mode
4	VDRV_CURRENT_LEVEL	R/W	0x0	Pull up current at VDRV pin 0x0 = 10 mA 0x1 = 20 mA
3:0	VDRV_VOLTAGE_LEVEL	R/W	0x0	Regulated Voltage at VDRV pin Value is calculated as : VDRV = VDRV_VOLTAGE_LEVEL + 5 [V]

7.6.1.7 ECHO_INT_CONFIG Register (Address = 0x17) [reset = 0x7]

ECHO_INT_CONFIG is shown in Table 13.

Return to the Summary Table.

Table 13. ECHO_INT_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	ECHO_INT_CMP_EN	R/W	0x0	Enable echo interrupt comparator output
3:0	ECHO_INT_THR_SEL	R/W	0x7	Threshold level to issue interrupt on OUT4 pin. Applied to Low pass filter output. If VOUT_SCALE_SEL=0x0 : Threshold = 0.04 x ECHO_INT_THR_SEL + 0.4 [V] If VOUT_SCALE_SEL=0x1: Threshold = 0.06 x ECHO_INT_THR_SEL + 0.6 [V]

7.6.1.8 ZC_CONFIG Register (Address = 0x18) [reset = 0x14]

ZC_CONFIG is shown in Table 14.

Return to the Summary Table.

Table 14. ZC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ZC_CMP_EN	R/W	0x0	Enable Zero Cross Comparator for Frequency detection
6	ZC_EN_ECHO_INT	R/W	0x0	When set, provides ZC information only when object is detected
5	ZC_CMP_IN_SEL	R/W	0x0	Zero Comparator Input Select 0x0 = INP - VCM 0x1 = INP - INN
4:3	ZC_CMP_STG_SEL	R/W	0x2	Zero Cross Comparator Stage Select

Table 14. ZC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	ZC_CMP_HYST	R/W	0x4	Zero Cross Comparator Hysteresis Selection 0x0 = 30 mV 0x1 = 80 mV 0x2 = 130 mV 0x3 = 180 mV 0x4 = 230 mV 0x5 = 280 mV 0x6 = 330 mV 0x7 = 380 mV

7.6.1.9 BURST_PULSE Register (Address = 0x1A) [reset = 0x0]

BURST_PULSE is shown in Table 15.

Return to the Summary Table.

Table 15. BURST_PULSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HALF_BRG_MODE	R/W	0x0	Use output driver in half-bridge mode. When enabled, drive both high-side FET together and low-side FETs together. 0x0 = Disable half-bridge mode 0x1 = Enable half bridge mode
6	PRE_DRIVER_MODE	R/W	0x0	Pre-driver mode to drive external FETs 0x0 = Disable pre-driver mode 0x1 = Enable pre-driver mode
6	RESERVED	R/W	0x0	Reserved
5:0	BURST_PULSE	R/W	0x0	Number of burst pulses. REG_VALUE=0x00 enables continuous burst mode

7.6.1.10 TOF_CONFIG Register (Address = 0x1B) [reset = 0x0]

TOF_CONFIG is shown in Table 16.

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Table 16. TOF_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SLEEP_MODE_EN	R/W	0x0	For entering or exiting sleep mode 0x0 = Wake up or exit Sleep Mode 0x1 = Enter sleep mode
6	STDBY_MODE_EN	R/W	0x0	For entering or exiting standby mode 0x0 = Exit Standby Mode 0x1 = Enter Standby mode
5:2	RESERVED	R	0x0	Reserved
1	VDRV_TRIGGER	R/W	0x0	Control charging of VDRV pin when DIS_VDRV_REG_LSTN = 1. This has no effect when VDRV_HI_Z=0x1. 0x0 = Disable I_{VDRV} 0x1 = Enable I_{VDRV}
0	CMD_TRIGGER	R/W	0x0	For IO_MODE=0x0, control enabling of burst mode. Ignored for other IO_MODE values. 0x0 = Disable burst mode 0x1 = Enable burst mode

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7.6.1.11 DEV_STAT Register (Address = 0x1C) [reset = 0x0]

DEV_STAT is shown in Table 17.

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Table 17. DEV_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	VDRV_READY	R	0x0	VDRV pin voltage status 0x0 = VDRV is below configured voltage 0x1 = VDRV is equal or above configured voltage
2	PULSE_NUM_FLT	R	0x0	The Driver has not received the number of pulses defined by BURST_PULSE
1	DRV_PULSE_FLT	R	0x0	The Driver has been stuck in a single state in burst mode for a period longer than delgitch time set by DRV_PLS_FLT_DT
0	EE_CRC_FLT	R	0x0	CRC error for internal memory

7.6.1.12 DEVICE_ID Register (Address = 0x1D) [reset = X]

DEVICE_ID is shown in Table 18.

Return to the Summary Table.

Table 18. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	X	Device ID: 0xB9

7.6.1.13 REV_ID Register (Address = 0x1E) [reset = 0x2]

REV_ID is shown in Table 19.

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Table 19. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	0x2	Revsion ID

8 Application and Implementation

8.1 Application Information

The TUSS4470 device must be paired with an external ultrasonic transducer. The TUSS4470 device drives the transducer to generate an ultrasonic echo and applies logarithmic gain scaling to the received echo signal in the analog front end. The transducer should be chosen based on the resonant frequency, input voltage requirements, sensitivity, beam pattern, and decay time. The TUSS4470 device is flexible enough to meet most transducer requirements by adjusting the driving frequency, driving current limit, and center frequency of the band-pass filter. The only available interface to configure the device registers is SPI. During the burst-and-listen cycles, an external ADC or analog receiver should be used to capture the echo envelope from the VOUT pin to compute time of flight (ToF), distance, amplitude, and/or width of the return echo.
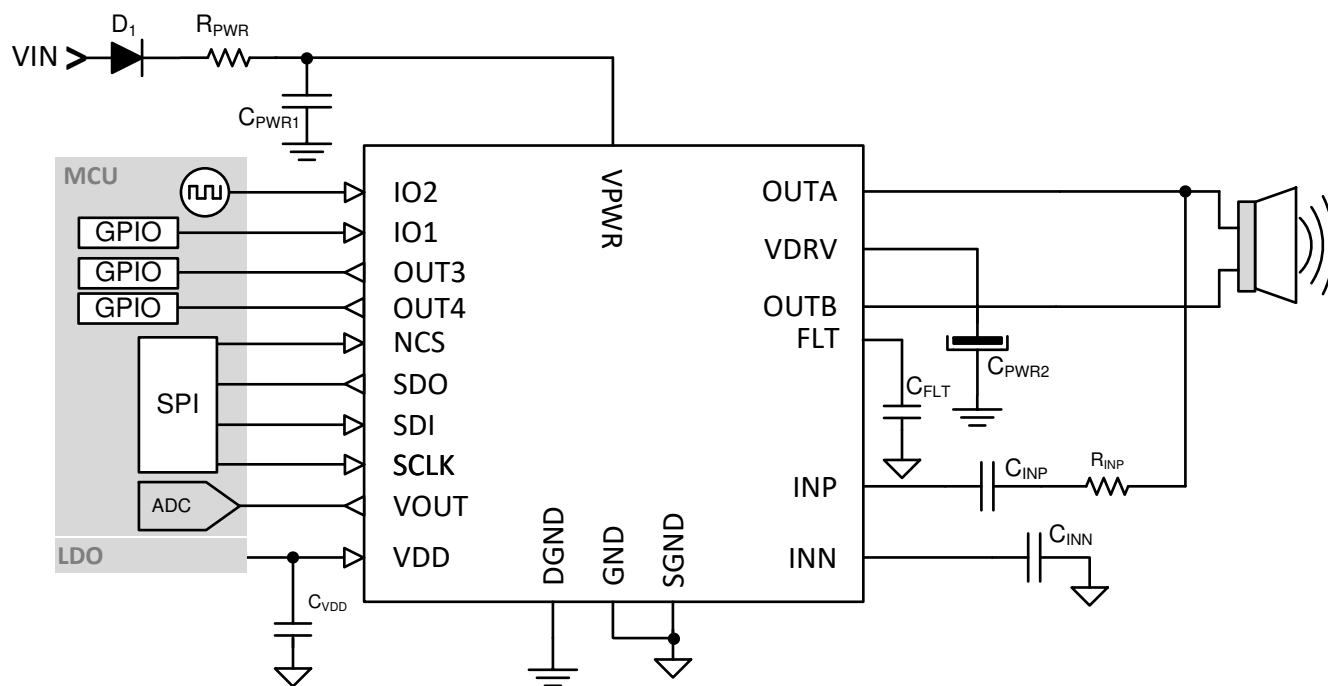
8.2 Typical Application

**Figure 25. TUSS4470 Application Diagram**

Typical Application (continued)

Table 20. Recommended Component Values for Typical Applications

DESIGNATOR	VALUE	COMMENT
R$_{PWR}$	10 Ω	Optional (to limit fast voltage transient on VPWR pin during power up)
R$_{(INP)}$	200Ω (1/4 Watt)	Optional higher value for EMI/ESD robustness
C$_{PWR1}$	50V, 100nF	
C$_{PWR2}$	40V, 2μF	
C$_{VDD}$	>5V, 10nF	
C$_{INP}$	40V, 330pF	
C$_{INN}$	>5V, C$_{INN}$	Use equation below to estimate value of C$_{INN}$ depending on the burst frequency $$C_{INN} = \frac{1}{2 \cdot \pi \cdot 150 \cdot \left(\dfrac{f_{DRV\_CLK}}{4}\right)}$$ (2)
C$_{FLT}$	5V, C$_{FLT}$	Use equation below to estimate value of C$_{FLT}$ depending on the burst frequency . Value has to be optimized for application depending on noise and response time requirements. $$C_{FLT} = \frac{25}{2 \cdot \pi \cdot \left(6250 \cdot f_{DRV\_CLK}\right)}$$ (3)
D1	1N4001 or equivalent	Optional for reverse supply and reverse current protection.
XDCR (transducer)		Example devices for low-frequency range: Closed top: 40 kHz: PUI Audio UTR-1440K-TT-R Open top: muRata MA40H1S-R, SensComp 40LPT16, Kobitone 255-400PT160-ROX Example devices for high-frequency range: Closed top: 300 kHz: Murata MA300D1-1

8.2.1 Transducer Drive Configuration Options

For different transducer drive configurations, the TUSS4470 supports multiple configurations to accommodate specific system needs as shown in Figure 26. The typical application diagram in Figure 25 is considered as "Case 1".
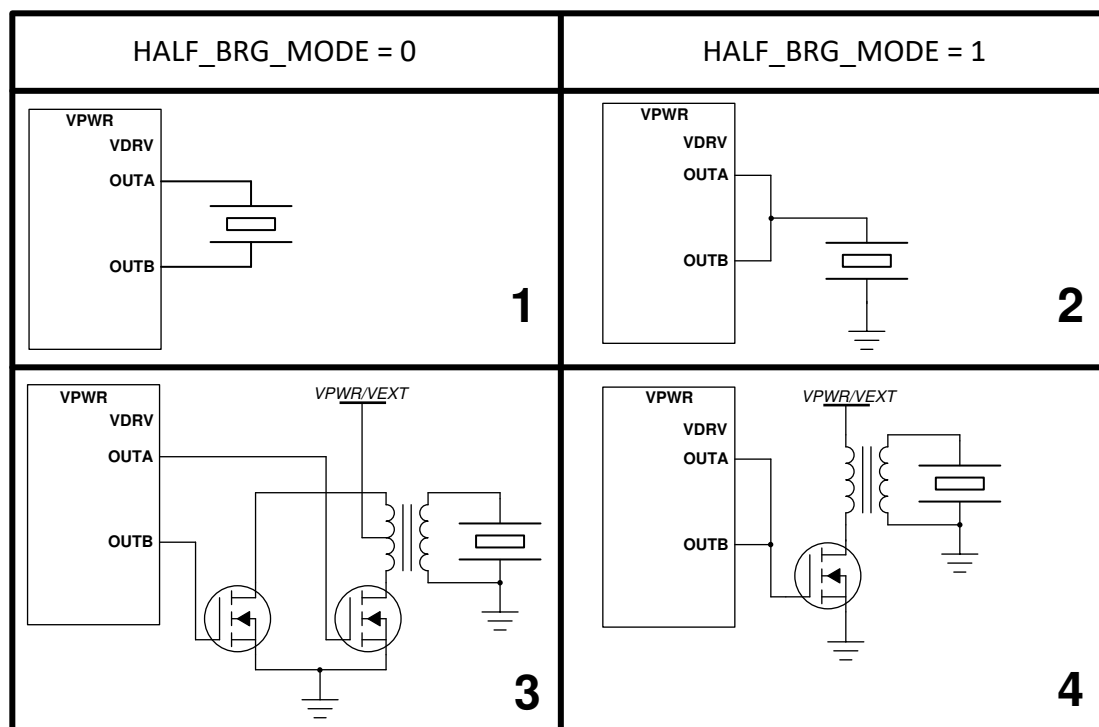
Figure 26. TUSS4470 Transducer Drive Options

The behavior of the internal FETs in the TUSS4470 device is different for each configuration in Figure 26. The relationship between the IOx pins and the state of the OUTA and OUTB pins for different register settings is shown in Table 21 and Table 22.

Table 21. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 2

IO MODE 2							
START OF BURST	PRE_DRIVER_MODE	HALF_BRG_MODE	IO1	IO2	OUTA	OUTB	APPLICATION CASE
YES	0	0	0	0	GND	GND	CASE 1
	0	0	0	1	GND	V_{VDRV}	
	0	0	1	0	V_{VDRV}	GND	
NO	0	0	1	1	Hi-Z	GND	
YES	0	1	0	0	Hi-Z	Hi-Z	CASE 2
	0	1	0	1	V_{VDRV}	V_{VDRV}	
	0	1	1	0	GND	GND	
NO	0	1	1	1	Hi-Z	Hi-Z	
YES	1	0	0	0	GND	GND	CASE 3
	1	0	0	1	GND	V_{VDRV}	
	1	0	1	0	V_{VDRV}	GND	
NO	1	0	1	1	GND	GND	
YES	1	1	0	0	GND	GND	CASE 4
	1	1	0	1	V_{VDRV}	V_{VDRV}	
	1	1	1	0	GND	GND	
NO	1	1	1	1	GND	GND	

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Table 22. OUTA / OUTB Pin Behavior for Different Drive Configurations in IO MODE 0, IO MODE 1 and IO MODE 3

						IO MODE 0, IO MODE 1, IO MODE 3		
START OF BURST	PRE_DRIVER_MODE	HALF_BRG_MODE	CMD_TRIGGER (IO MODE 0)	IO1 (IO MODE 1)	IO2	OUTA	OUTB	APPLICATION CASE
NO	0	0	0	1	0	Hi-Z	GND	CASE 1
	0	0	0	1	1	Hi-Z	GND	
YES	0	0	1	0	0	GND	V_{VDRV}	
	0	0	1	0	1	V_{VDRV}	GND	
NO	0	1	0	1	0	Hi-Z	Hi-Z	CASE 2
	0	1	0	1	1	Hi-Z	Hi-Z	
YES	0	1	1	0	0	GND	GND	
	0	1	1	0	1	V_{VDRV}	V_{VDRV}	
NO	1	0	0	1	0	GND	GND	CASE 3
	1	0	0	1	1	GND	GND	
YES	1	0	1	0	0	GND	V_{VDRV}	
	1	0	1	0	1	V_{VDRV}	GND	
NO	1	1	0	1	0	GND	GND	CASE 4
	1	1	0	1	1	GND	GND	
YES	1	1	1	0	0	GND	GND	
	1	1	1	0	1	V_{VDRV}	V_{VDRV}	

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 23 as the input and operating parameters. All other device settings can be assumed to be factory default.

Table 23. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5 to 36 V
Input voltage recommended	5 V or 20 V
Transducer driving voltage	5 V_{AC} or 20 V_{AC}
Transducer frequency	40 kHz or 400 kHz
Transducer pulse count	16

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:
- Transducer
    - Transducer driving voltage
    - Transducer resonant frequency
    - Transducer pulse count maximum

8.2.1.2.1 Transducer Driving Voltage

When a voltage is applied to piezoelectric ceramics, mechanical distortion is generated according to the voltage and frequency. The mechanical distortion is measured in units of sound pressure level (SPL) to indicate the volume of sound, and can be derived from a free-field microphone voltage measurement using Equation 4.

$$SPL\ (db) = 20 \times \log \frac{\left(\dfrac{V_{(MIC)}}{3.4\ mV} \right)}{P_O}$$

where
- $V_{(MIC)}$ is the measured sensor sound pressure (mV_{RMS}).

- P_O is a referenced sound pressure of 20 μPa. (4)

The SPL does not increase indefinitely with the driving voltage. After a particular driving voltage, the amount of SPL that a transducer can generate becomes saturated. A transducer is given a maximum driving voltage specification to indicate when the maximum SPL is generated. Driving the transducer beyond the maximum driving voltage makes the ultrasonic module less power-efficient and can damage or decrease the life expectancy of the transducer.

8.2.1.2.2 Transducer Driving Frequency

The strength of ultrasonic waves propagated into the air attenuate proportionally with distance. This attenuation is caused by diffusion, diffraction, and absorption loss as the ultrasonic energy transmits through the medium of air. As shown in Figure 27, the higher the frequency of the ultrasonic wave, the larger the attenuation rate and the shorter the distance the wave reaches.
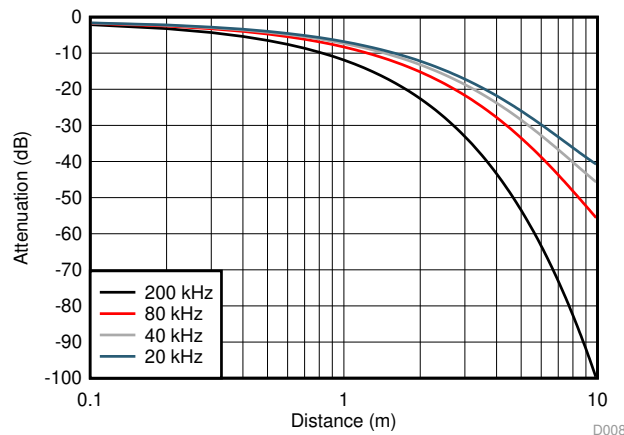

Figure 27. Attenuation Characteristics of Sound Pressure by Distance

An ultrasonic transducer has a fixed resonant center frequency with a typical tolerance of ±2%. The lower frequency range of 30 kHz to 100 kHz is the default operating range for common long range applications for a step resolution of 1 cm and typical range of 30 cm to 5 m. The upper frequency range of 100 kHz to 1000 kHz is reserved for high-precision applications with a step resolution of 1 mm and a typical range of 5 cm to 1 m.

8.2.1.2.3 Transducer Pulse Count

The pulse count determines how many alternating periods are applied to the transducer by the complementary low-side drivers and determines the total width of the ultrasonic ping that was transmitted. The larger the width of the transmitted ping, the larger the width of the returned echo signature of the reflected surface and the more resolution available to set a stable threshold. A disadvantage of a large pulse count is a large ringing-decay period, which limits how detectable objects are at short distances.

Select a pulse count based on the minimum object distance requirement. If short-distance object detection is not a priority, a high pulse count is not a concern. Certain transducers can be driven continuously while others have a limit to the maximum driving-pulse count. Refer to the specification for the selected transducer to determine if the pulse count must be limited.

8.2.1.3 Application Curves

Figure 28 and Figure 29 show the typical ranging performance of a 40-kHz, closed-top transducer under nominal operating conditions as indicated in Table 23. The targeted object is a PVC pole measuring 1000 mm in height and 75 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x1.
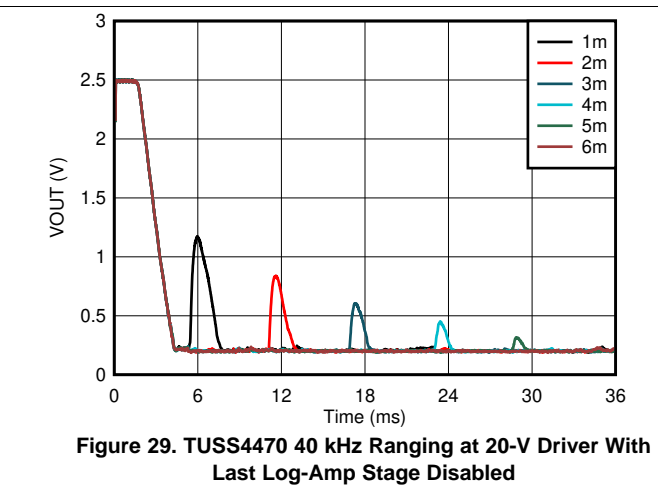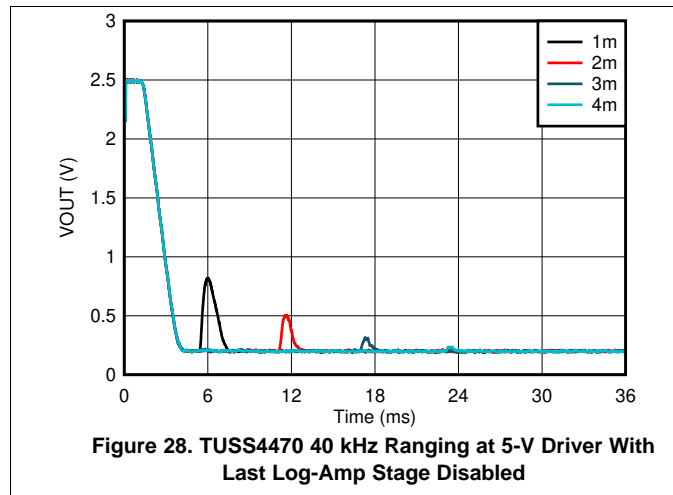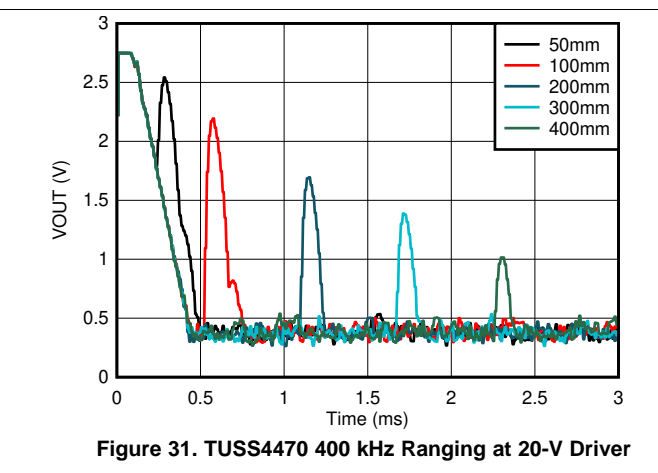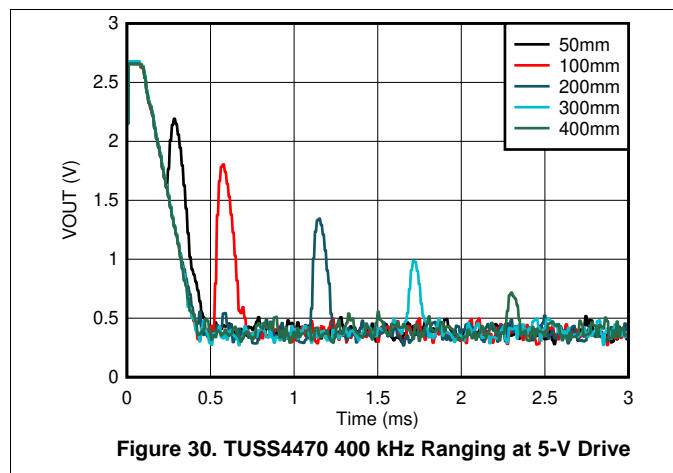

Figure 28. TUSS4470 40 kHz Ranging at 5-V Driver With Last Log-Amp Stage Disabled

Figure 29. TUSS4470 40 kHz Ranging at 20-V Driver With Last Log-Amp Stage Disabled

Figure 30 and Figure 31 show the typical ranging performance of a 400-kHz, closed-top transducer under nominal operating conditions as indicated in Table 23. The targeted object is an aluminum pole measuring 100 mm in height and 10 mm in diameter. Notable device settings: LNA_GAIN = 0x0; VOUT_SCALE_SEL = 0x0; LOGAMP_DIS_FIRST = 0x0; LOGAMP_DIS_LAST = 0x0.

Figure 30. TUSS4470 400 kHz Ranging at 5-V Drive

Figure 31. TUSS4470 400 kHz Ranging at 20-V Driver

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9 Power Supply Recommendations

The TUSS4470 device is designed to operate from two independent supplies, a driver supply and a regulated supply.

The driver input voltage supply (VPWR) range can operate from 5 V to 36 V. In applications where the TUSS4470 device may be exposed to battery transients and reverse battery currents, use external component-safeguards, such as component D1 or parallel TVS diodes, to help protect the device. If the input supply is placed more than a few inches from the TUSS4470 device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors near the VPWR pin. In the event both the VDRV and pre-driver modes is enabled, limit the VPWR voltage to the maximum rated voltage of the externally driven transistor's gate-source or base-emitter rating. The electrolytic capacitor at the VDRV pin is intended to act as a fast discharge capacitor during the bursting stage of the TUSS4470 device. The H-bridge high-side voltage can be supplied with an independent voltage at the VDRV pin to isolate the driver from VPWR, but must remain within the specified maximum voltage rating of the VDRV, OUTA, and OUTB outputs. If the H-bridge high-side voltage is to be supplied by an independent source, VDRV should be disabled.

The regulated supply (VDD) is used as the supply reference for the analog front end, filtering, and analog output blocks, so this supply should be stable for maximum performance. TI recommends using an LDO or other regulated external power source with bypass capacitor placed closely to the VDD pin. As VDD becomes less stable, the noise floor of the VOUT signal will increase, and result in a loss of long range object detection as a consequence.

To prevent damage to the device, always avoid hot-plugging or providing instantaneous power at the VPWR and VDRV pins at start-up, unless these pins are properly protected with an RC filter or TVS diode to minimize transient effects. VPWR must always be equal to or greater than the value present at VDRV.

10 Layout

10.1 Layout Guidelines

A minimum of two layers is required to accomplish a small-form factor ultrasonic module design. The layers should be separated by analog and digital signals. The pin map of the device is routed such that the power and digital signals are on the opposing side of the analog driver and receiver pins. Consider the following best practices for TUSS4470 device layout in order of descending priority:

- Separating the grounding types is important to reduce noise at the AFE input of the TUSS4470. In particular, the transducer sensor ground, supporting driver, and return-path circuitry should have a separate ground before being connected to the main ground. Separating the sensor and main grounds through a ferrite bead is best practice, but not require. A copper-trace or 0-Ω short is also acceptable when bridging grounds.
- The analog return path pins, INP and INN, are most susceptible to noise and therefore should be routed as short and directly to the transducer as possible. Ensure the INN capacitor is close to the pin to reduce the length of the ground wire.
- The analog output pin trace should be routed as short and directly to an external ADC or microcontroller input to avoid signal-to-noise losses due to parasitic-effects or noise coupling onto the trace from external radiating aggressors.
- In applications where protection from an ESD strike on the case of the transducer is important, ground routing of the capacitor on the INN pin should be separate from the device ground and connected directly with the shortest possible trace to the connector ground.
- The analog drive pins can be high-current, high-voltage, or both and therefore the design limitation of the OUTA and OUTB pins is based on the copper trace profile. The driver pins are recommended to be as short and direct as possible when driving a transducer with a high-voltage.
- The decoupling capacitors for the VDD and VPWR pins should be placed as close to the pins as possible.
- Any digital communication should be routed away from the analog receiver pins. TXD, RXD, SCLK, NCS, IO1, IO2, OUT3, and OUT4 pins should be routed on the opposite side of the PCB, away of the analog signals.

10.2 Layout Example

Figure 32. TUSS4470 Layout Example

Product Folder Links: *TUSS4470*

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.
   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSS4470TRTJR	ACTIVE	QFN	RTJ	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 105	USS4470	Samples
TUSS4470TRTJT	ACTIVE	QFN	RTJ	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-25 to 105	USS4470	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSS4470TRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TUSS4470TRTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSS4470TRTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
TUSS4470TRTJT	QFN	RTJ	20	250	210.0	185.0	35.0

RTJ (S−PWQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

$\frac{4,15}{3,85}$

15   11

16   10

$\frac{4,15}{3,85}$

20   6

Pin 1 Index Area
Top and Bottom

1   5

$\frac{0,80}{0,70}$

0,20 Nominal
Lead Frame

Seating Plane

△ 0,08 C

Seating Height $\frac{0,05}{0,00}$ C

1   5

F

20   6

THERMAL PAD

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

16   10

0,50

15   11

20X $\frac{0,30}{0,18}$

⊕ | 0,10 Ⓜ | C | A | B
| 0,05 Ⓜ | C |

Bottom View

4205505/F   07/11
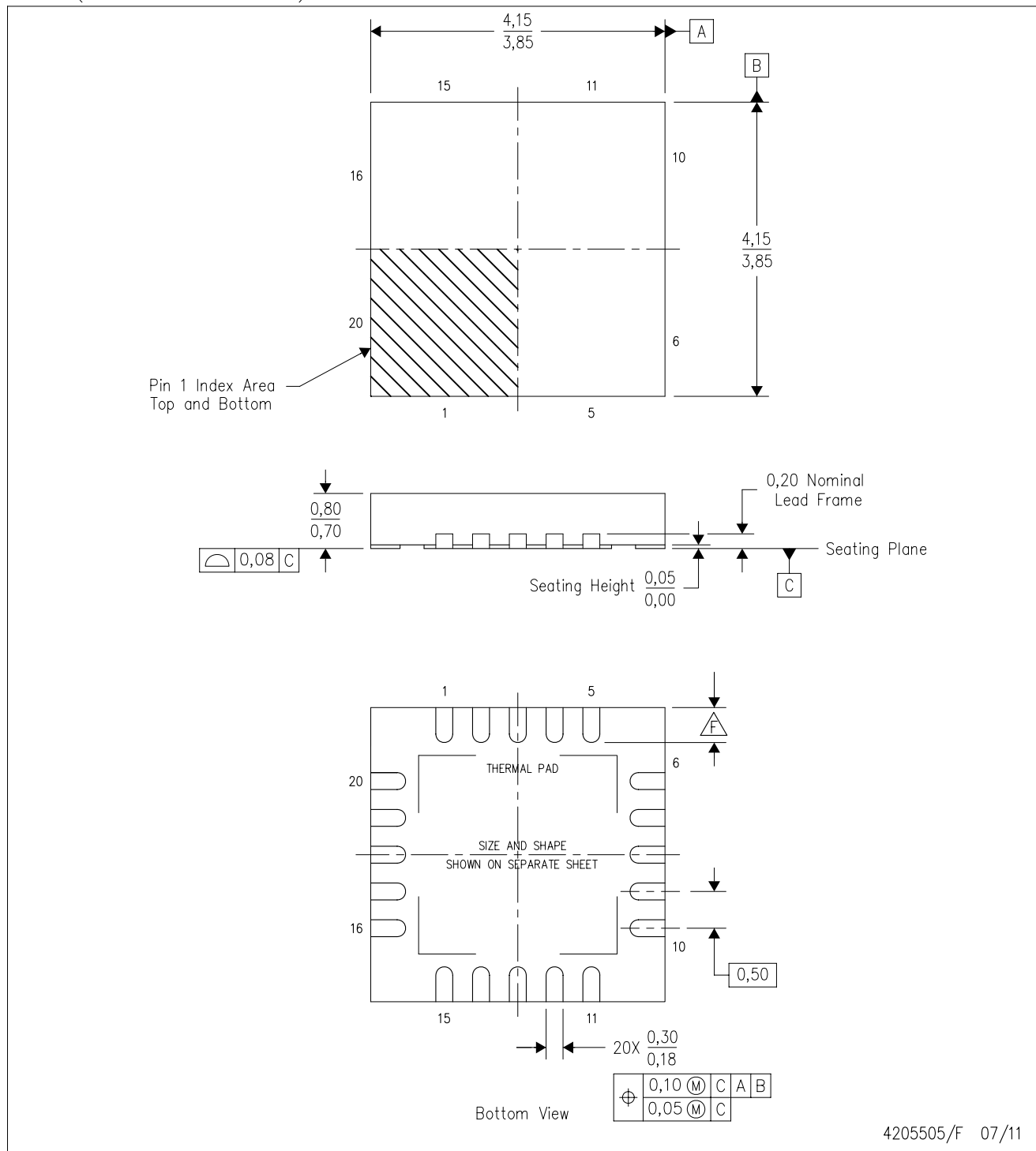
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5−1994.
        B. This drawing is subject to change without notice.
        C. QFN (Quad Flatpack No−Lead) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
        E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
        F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

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RTJ (S–PWQFN–N20)   PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C 0,30

$20 \times \dfrac{0,50}{0,30}$

20 ⟶

2,70±0,10

16

15   11

2,70±0,10

Exposed Thermal Pad
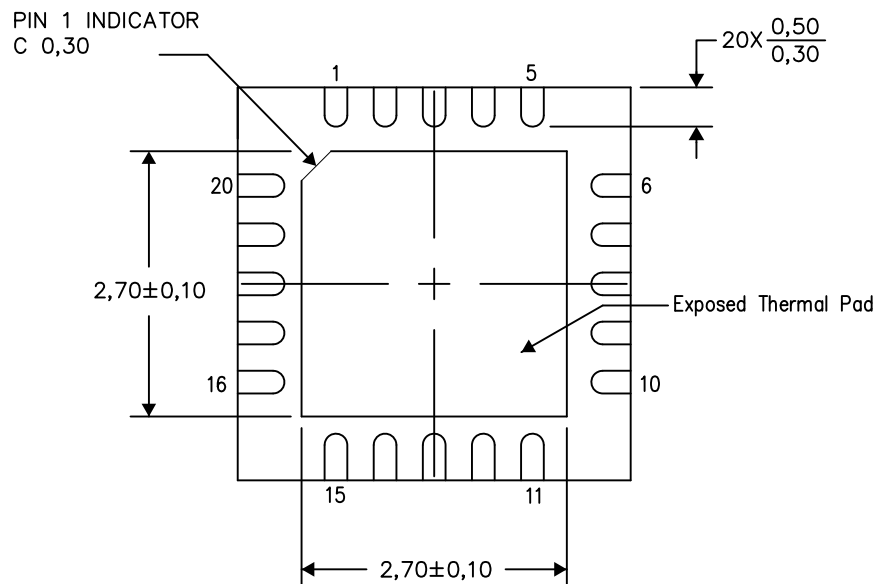
Bottom View

Exposed Thermal Pad Dimensions

4206256–2/V   05/15

NOTE: All linear dimensions are in millimeters

RTJ (S–PWQFN–N20)   PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout

Note D

16x0,5

3,1 4,8

3,1

4,8

Non Solder Mask Defined Pad

Example Solder Mask Opening
(Note F)

0,08

R0,14

0,85

0,28

0,07

All Around

Pad Geometry
(Note C)

Example Stencil Design
0.125 Thick Stencil
(Note E)

16x0,5

0,8

4x1,1

0,3

0,3
4x1,1

3,15 4,75

0,230

R0,115

3,15

4,75

(66% Printed Solder Coverage by Area)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note D, F)

9xØ0,3

2,7

6x0,9

2,7

6x0,9

4207065–2/N 03/15
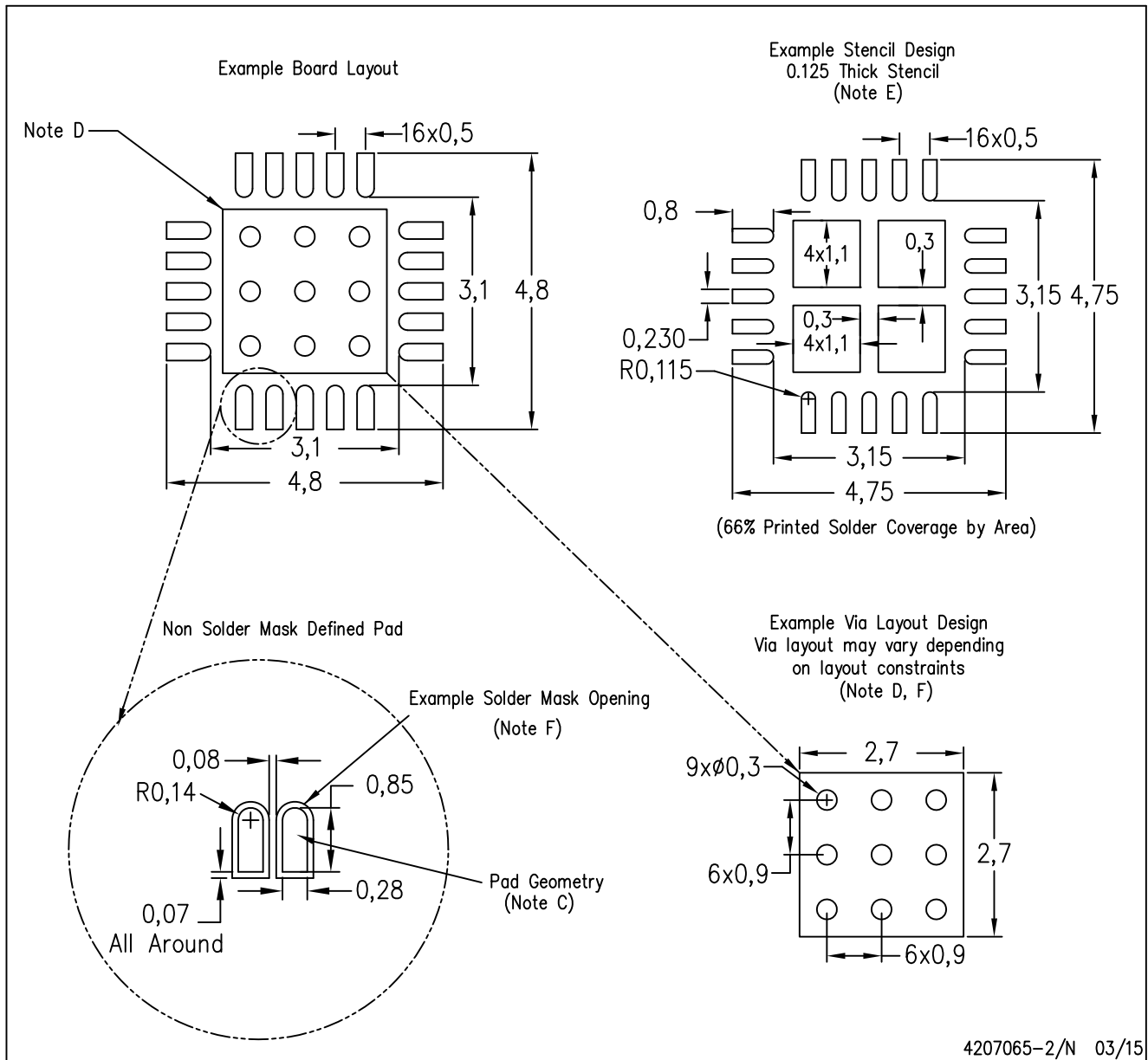
NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC–7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
            recommendations for vias placed in the thermal pad.

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