REF200 Dual Current Source and Current Sink

1 Features

- Completely Floating: No Power Supply or Ground Connections
- High Accuracy: 100 µA ±0.5%
- Low Temperature Coefficient: ±25 ppm/°C
- Wide Voltage Compliance: 2.5 V to 40 V
- Includes Current Mirror

2 Applications

- Sensor Excitation
- Biasing Circuitry
- Offsetting Current Loops
- Low Voltage References
- Charge-pump Circuitry
- Hybrid Microcircuits

3 Description

The REF200 combines three circuit building-blocks on a single monolithic chip: two 100-µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, because the current sources are two-terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

The sections can be pin-strapped for currents of 50 µA, 100 µA, 200 µA, 300 µA, or 400 µA. External circuitry can obtain virtually any current. These and many other circuit techniques are shown in the *Application Information* section of this data sheet.

The REF200 is available in an SOIC package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
REF200	SOIC (8)	3.91 mm × 4.90 mm

(1) For all available packages, see the package addendum at the end of the data sheet.

Functional Block Diagram

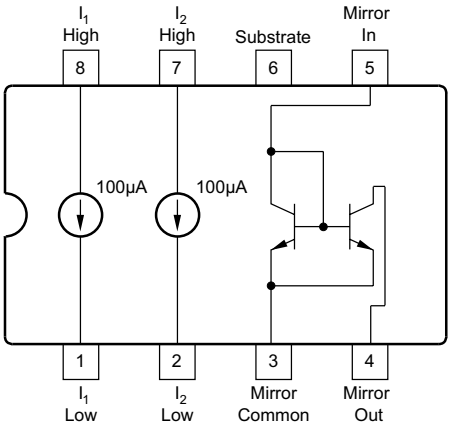


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2015) to Revision B — **Page**

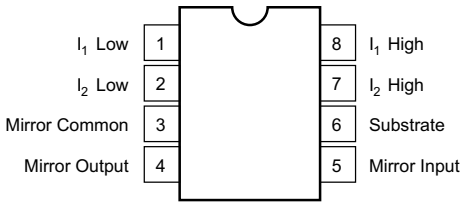
- Changed multiple instances of "mA" in data sheet back to "µA" (typo) ... 1

Changes from Original (September 2000) to Revision A — **Page**

- Added *ESD Ratings* and *Recommended Operating Conditions* tables, and *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
I_1 Low	1	Current source 1 low terminal
I_2 Low	2	Current source 2 low terminal
Mirror Common	3	Current mirror common terminal
Mirror Output	4	Current mirror output terminal
Mirror Input	5	Current mirror input terminal
Substrate	6	Substrate (Usually connected to most negative potential in the system)
I_2 High	7	Current source 2 high terminal
I_1 High	8	Current source 1 high terminal

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Applied voltage	–6	40	V
	Reverse current		–350	µA
	Voltage between any two sections		±80	V
	Operating temperature	–40	85	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(1)	±750	V

(1) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{COMP}	Compliance voltage	2.5		40	V
T_A	Specified temperature range	–25		85	°C

6.4 Electrical Characteristics

at T_A = 25°C, V_S = 15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SOURCES						
	Current accuracy			±0.25%	±1%	
	Current match			±0.25%	±1%	
	Temperature drift	Specified temperature range		25		ppm/°C
	Output impedance	2.5 V to 40 V	20	100		MΩ
		3.5 V to 30 V	200		500	
	Noise	BW = 0.1 Hz to 10 Hz		1		nAp-p
		f = 10 kHz		20		pA/√Hz
	Voltage compliance (1%)	T_{MIN} to T_{MAX}	See *Typical Characteristics*			
	Capacitance			10		pF
CURRENT MIRROR – I = 100 µA unless otherwise noted						
	Gain		0.995	1	1.005	
	Temperature drift			25		ppm/°C
	Impedance (output)	2 V to 40 V	40	100		MΩ
	Nonlinearity	I = 0 µA to 250 µA		0.05%		
	Input voltage			1.4		V
	Output compliance voltage		See *Typical Characteristics*			
	Frequency response (–3 dB)	Transfer		5		MHz

6.5 Typical Characteristics

at T_A = 25°C, V_S = 15 V (unless otherwise noted)

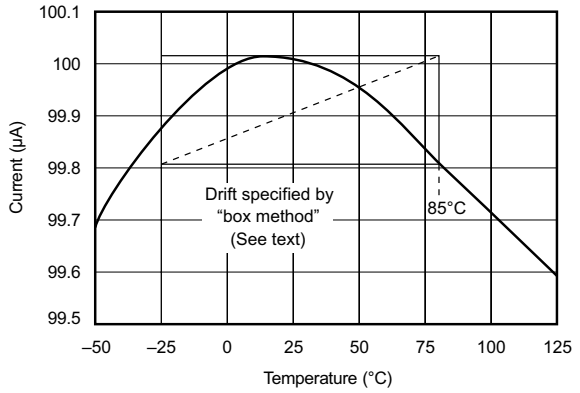


Figure 1. Current Source Typical Drift vs Temperature

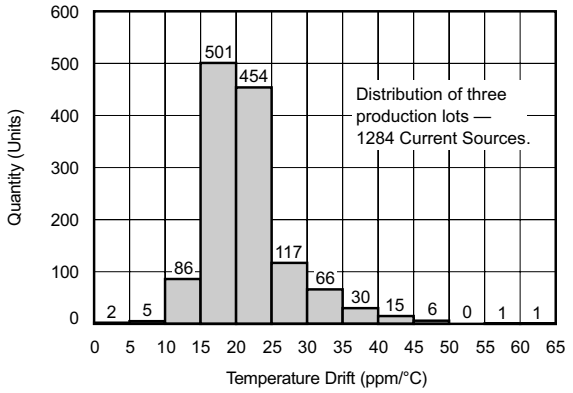


Figure 2. Current Source Temperature Drift Distribution

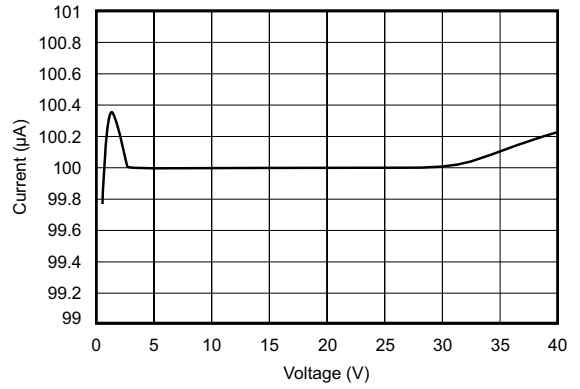


Figure 3. Current Source Output Current vs Voltage

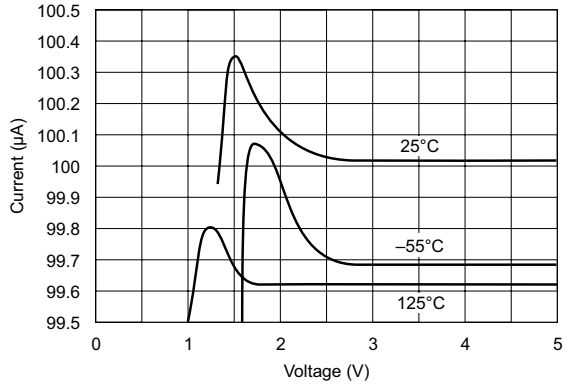


Figure 4. Current Source Output Current vs Voltage

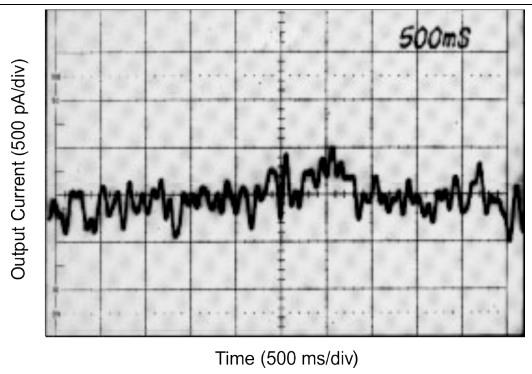


Figure 5. Current Source Current Noise (0.1 Hz to 10 Hz)

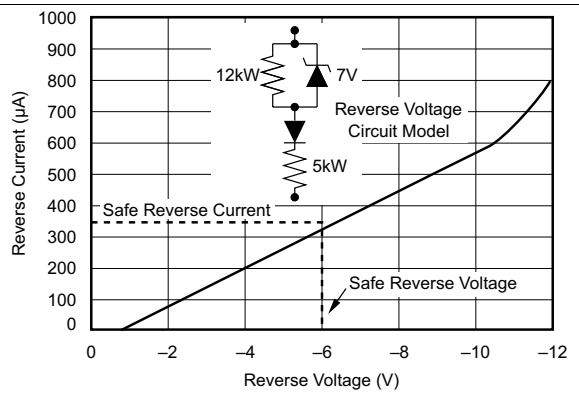


Figure 6. Current Source Reverse Current vs Reverse Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_S = 15 V (unless otherwise noted)

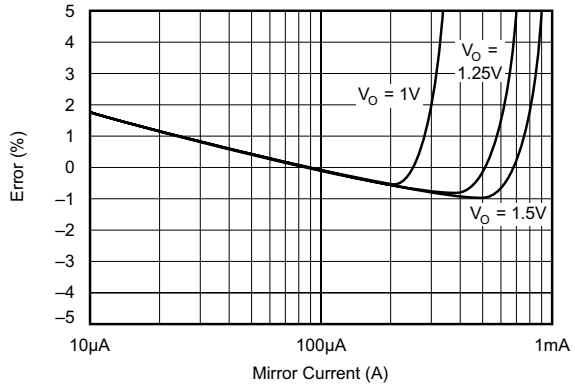


Figure 7. Mirror Gain Error vs Current

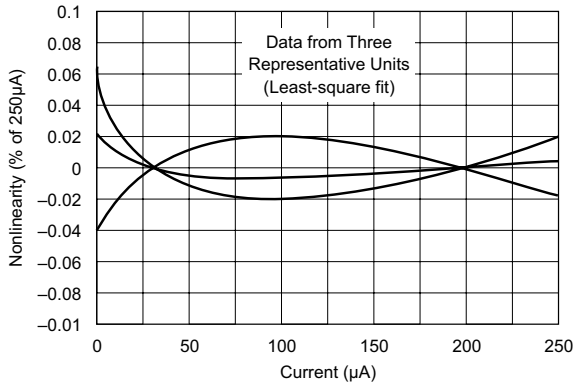


Figure 8. Mirror Transfer Nonlinearity

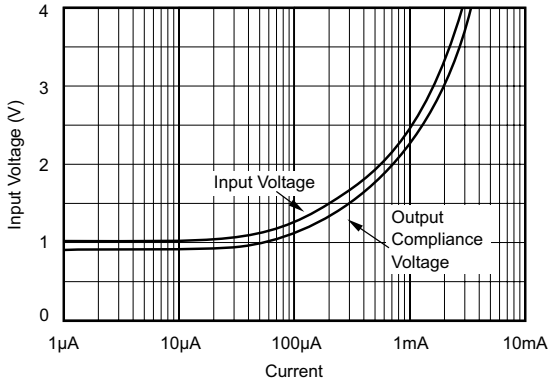


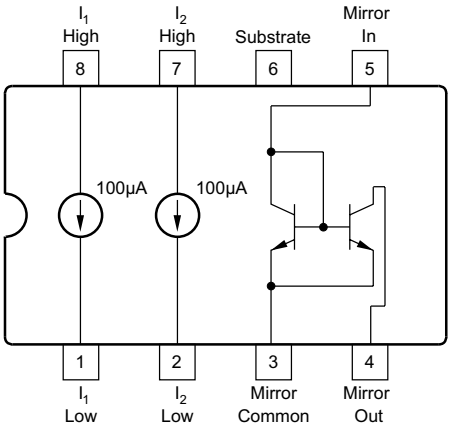
Figure 9. Mirror Input Voltage and Output Compliance Voltage vs Current

7 Detailed Description

7.1 Overview

The REF200 device combines three circuit building-blocks on a single monolithic chip—two 100-µA current sources and a current mirror. The sections are dielectrically isolated, making them completely independent. Also, because the current sources are two terminal devices, they can be used equally well as current sinks. The performance of each section is individually measured and laser-trimmed to achieve high accuracy at low cost.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Temperature Drift

Drift performance is specified by the *box method*, as illustrated in Figure 1. The upper and lower current extremes measured over temperature define the top and bottom of the box. The sides are determined by the specified temperature range of the device. The drift of the unit is the slope of the diagonal, typically 25 ppm/°C from –25°C to +85°C.

7.4 Device Functional Modes

The three circuit sections of the REF200 are electrically isolated from one another, using a dielectrically-isolated fabrication process. A substrate connection is provided (pin 6), which is isolated from all circuitry. This pin should be connected to a defined circuit potential to assure rated DC performance. The preferred connection is to the most negative constant potential in the system. In most analog systems, this would be $-V_S$. For best ac performance, leave pin 6 open and leave unused sections unconnected. Figure 10 shows the simplified circuit diagram of the REF200.

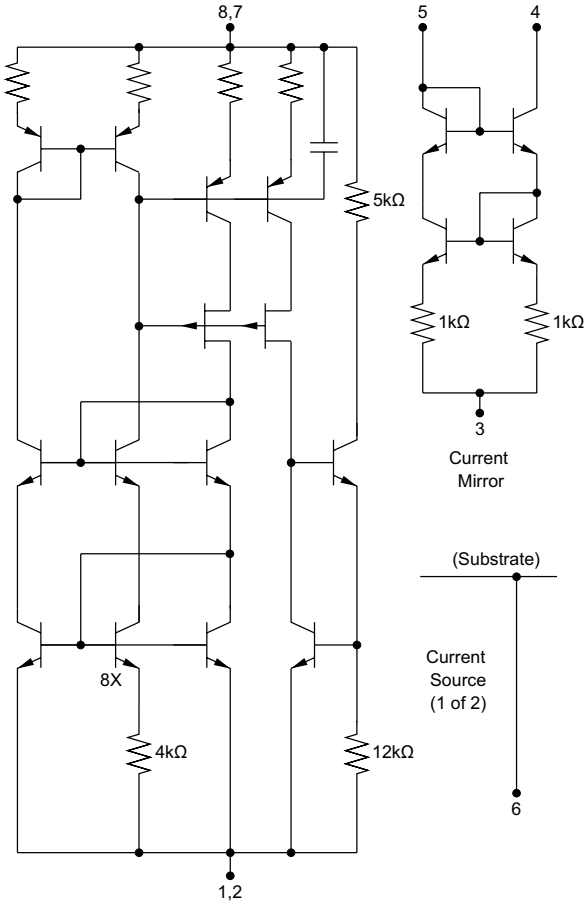


Figure 10. Simplified Circuit Diagram

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Applications for the REF200 are limitless. Application Bulletin AB-165 (SBOA046) shows additional REF200 circuits as well as other related current source techniques. In this section, a collection of circuits are shown to illustrate some techniques.

If the current sources are subjected to reverse voltage, a protection diode may be required. A reverse voltage circuit model of the REF200 is shown in Figure 6. If reverse voltage is limited to less than 6 V or reverse current is limited to less than 350 µA, then no protection circuitry is required. A parallel diode (see (a) in Figure 17) protects the device by limiting the reverse voltage across the current source to approximately 0.7 V. In some applications, a series diode may be preferable (see (b) in Figure 17), because it allows no reverse current. This configuration, however, reduces the compliance voltage range by one diode drop.

8.2 Typical Application

Figure 11 shows the schematic of a circuit that translates RTD resistance to a voltage level convenient for an ADC input. The REF200 precision current reference provides excitation and an instrumentation amplifier scales the signal. The design also uses a 3-wire RTD configuration to minimize errors due to wiring resistance.

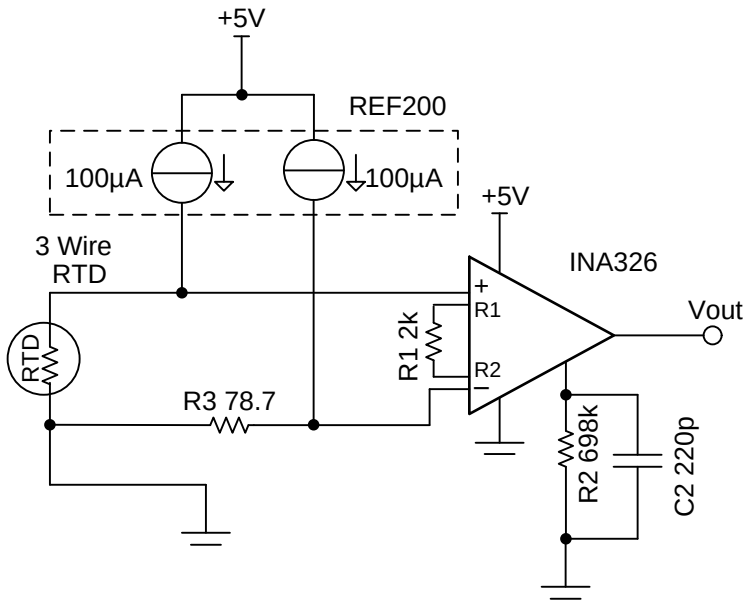


Figure 11. RTD Resistance to Voltage Converter Schematic

Typical Application (continued)

8.2.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V
- RTD temperature range: –50°C to +125°C
- RTD resistance range 80.3 Ω to 147.9 Ω
- Output: 0.1 V to 4.9 V

The design goals and performance are summarized in Table 1. Figure 15 depicts the measured transfer function of the design.

Table 1. Comparison of Design Goals, Calculations, Simulation, and Measured Performance

V_{OUT}	RTD	GOAL	CALCULATED	SIMULATED	MEASURED
V_{OUT} maximum scale	80.3 Ω	0.1 V	0.112 V	0.117 V	0.11 3 V
V_{OUT} minimum scale	142.9 Ω	4.9 V	4.83 V	4.82 V	4.862 V

8.2.2 Detailed Design Procedure

Figure 12 and Figure 13 shows the schematic of the RTD amplifier for minimum and maximum output conditions. This circuit was designed for a –50°C to 150°C RTD temperature range. At –50°C the RTD resistance is 80.3 Ω and the voltage across it is 8.03 mV (V_{RTD} = (100 µA) (80.3 Ω), see Figure 2). Notice that R3 develops a voltage drop that opposes the RTD drop. The drop across R3 is used to shift amplifiers input differential voltage to a minimum level. The output is the differential input multiplied by the gain (Vout = 698 · 160 µV = 0.111 V). At 150°C, the RTD resistance is 148 Ω and the voltage across it is 14. 8 mV (V_{RTD} = (100 µA × 148 Ω). This produces a differential input of 6.93 mV and an output voltage of 4.84 V (V_{OUT} = 698 · 6.93 mV = 4.84 V , see Figure 13). For more detailed design procedures and results, refer to the reference guide, *RTD to Voltage Reference Design Using Instrumentation Amplifier and Current Reference* (TIDU969).

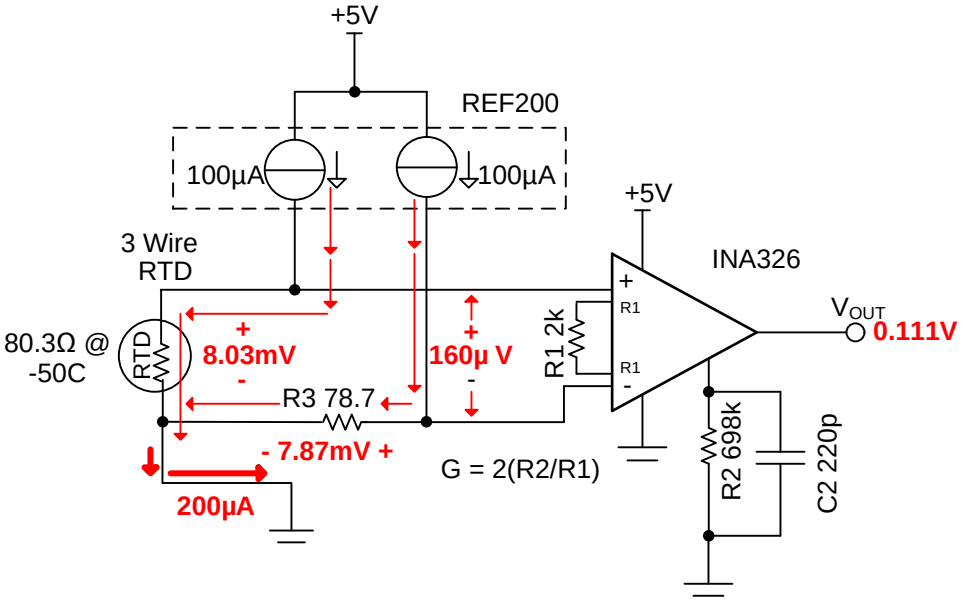


Figure 12. RTD Amplifier with Minimum Output Condition

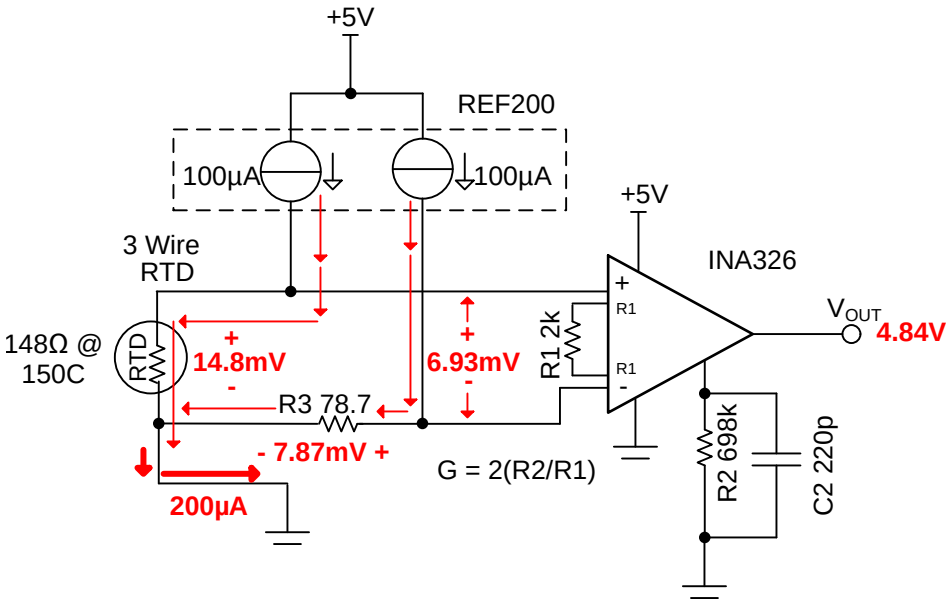


Figure 13. RTD Amplifier with Maximum Output Condition

8.2.2.1 Lead Resistance Cancelation (3-Wire RTD)

Figure 14 shows the 3-wire RTD configuration can be used to cancel lead resistance. The resistance in each lead must be equal to cancel the error. Also, the two current sources in the REF200 must be equal. Notice that the voltage developed on the two top leads of the RTD are equal and opposite polarity so that the amplifiers input is only from the RTD voltage. In this example, the RTD drop is 14.8 mV and the leads each have 1 mV. Notice that the 1 mV drops cancel. Finally, notice that the voltage on the 3rd lead (2 mV) creates a small shift in the common mode voltage. In some applications, a larger resistor is intentionally added to shift the common-mode voltage. However, the INA326 has a rail-to-rail common mode range, so it can accept common-mode voltages near ground.

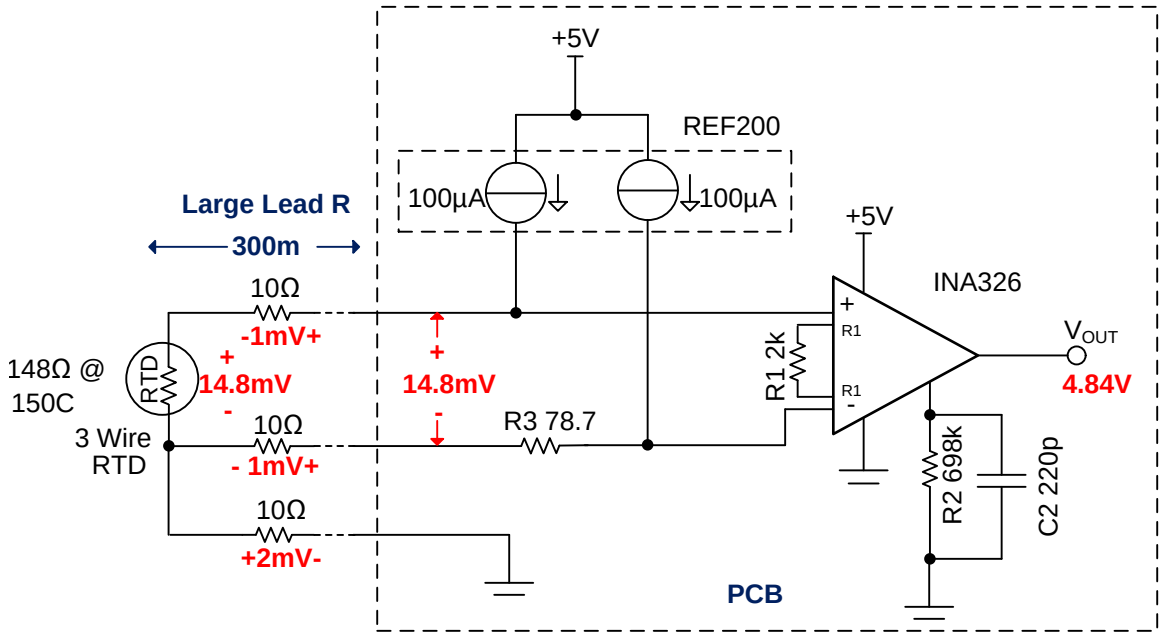


Figure 14. 3-Wire RTD Configuration Cancels Lead Resistance

8.2.3 Application Curves

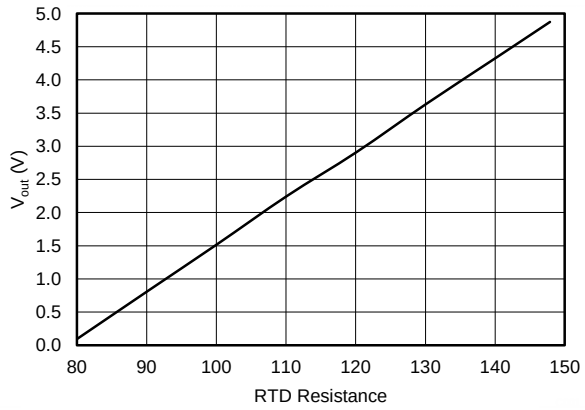


Figure 15. RTD to Vout Transfer Function

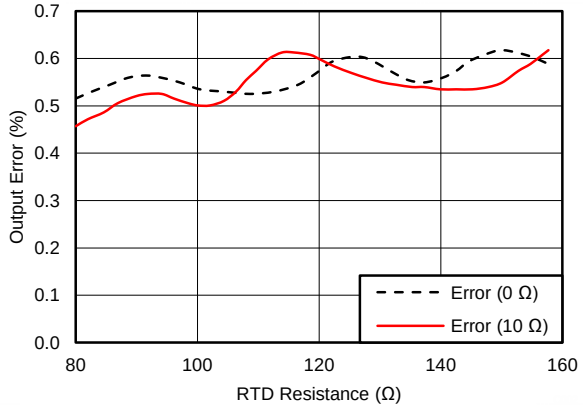


Figure 16. Measured Error vs RTD Resistance

8.3 System Examples

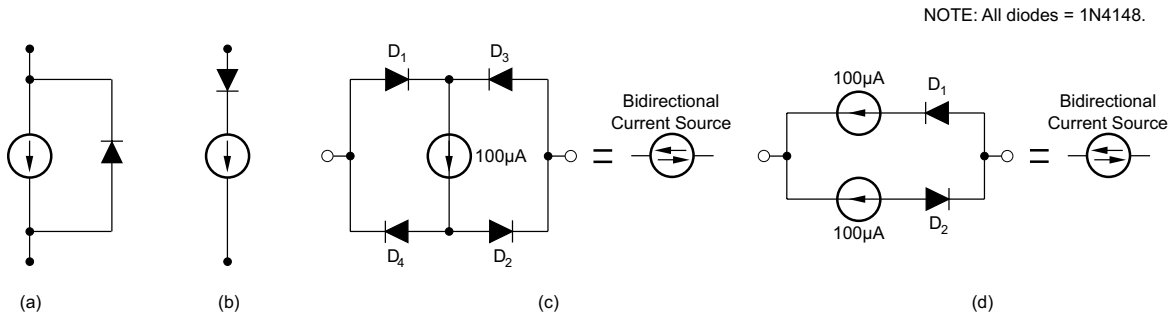


Figure 17. Reverse Voltage Protection

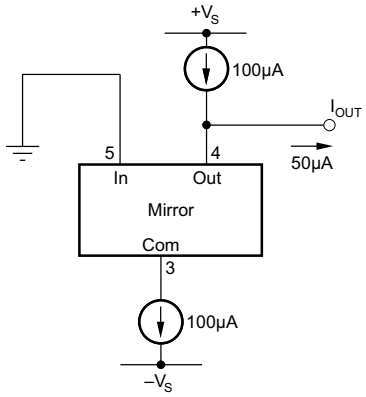


Figure 18. 50-µA Current Source

System Examples (continued)

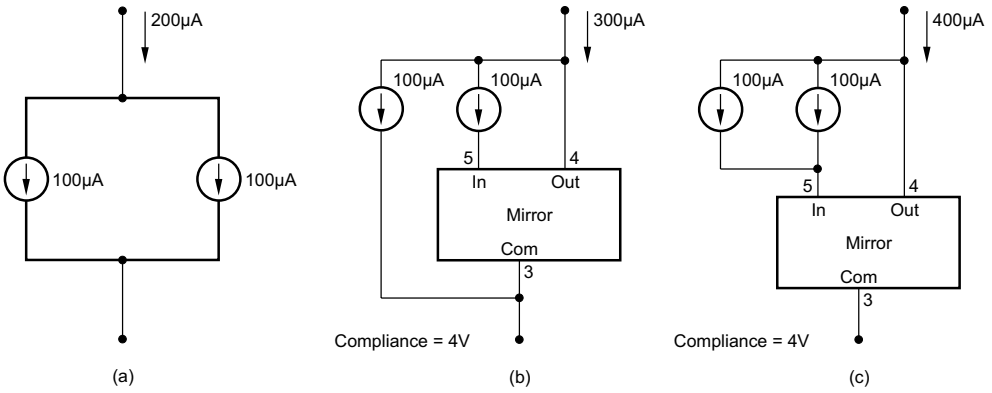


Figure 19. 200-µA, 300-µA, and 400-µA Floating Current Sources

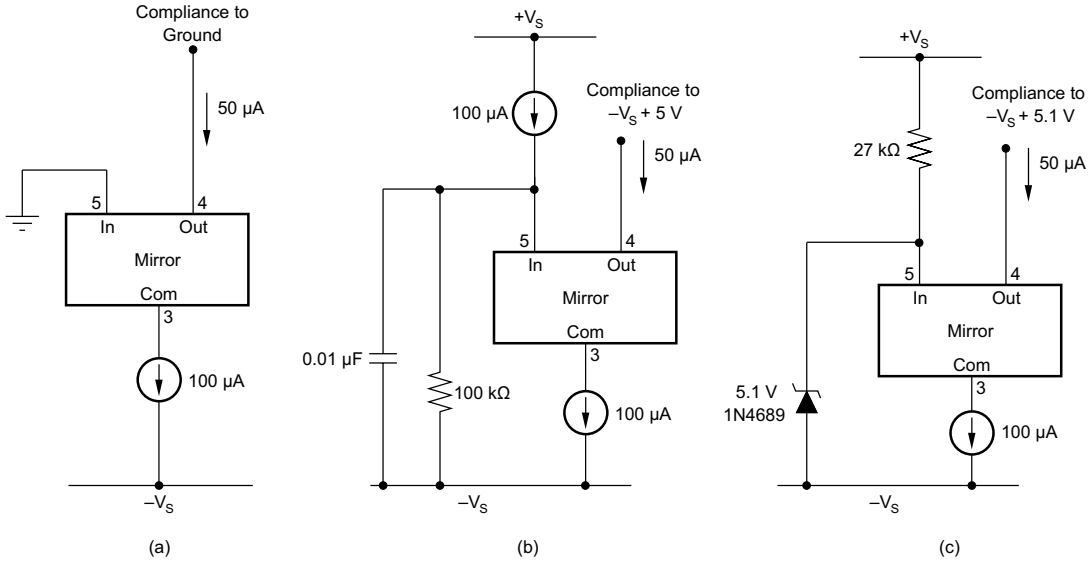


Figure 20. 50-µA Current Sinks

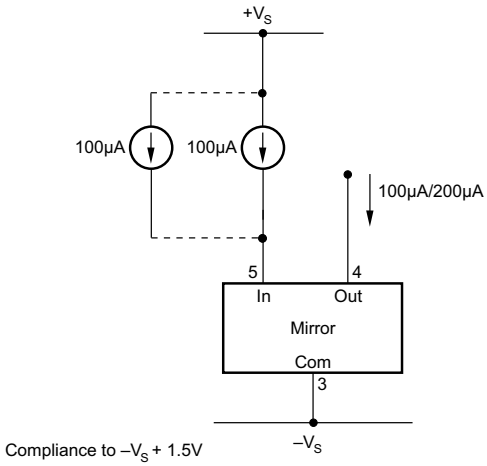


Figure 21. Improved Low-Voltage Compliance

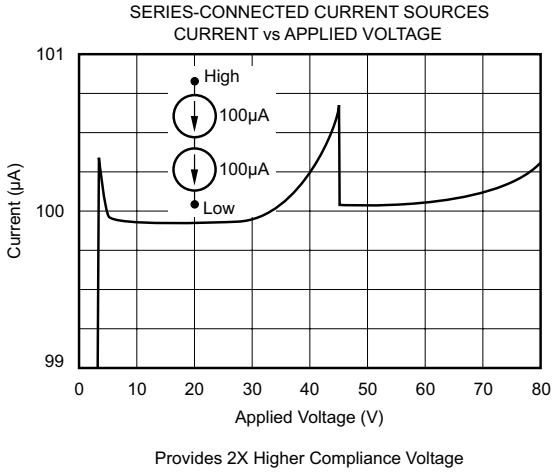
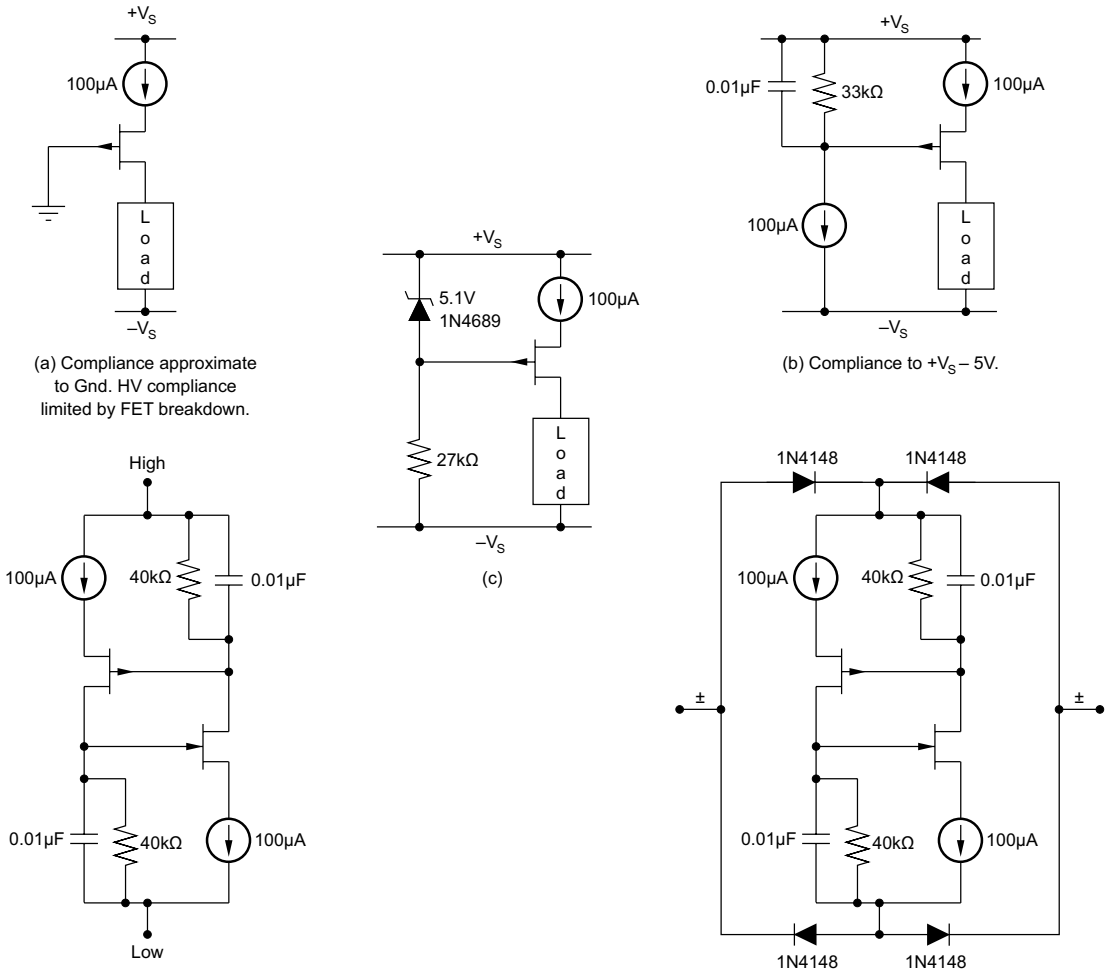


Figure 22. 100-µA Current Source—80-V Compliance

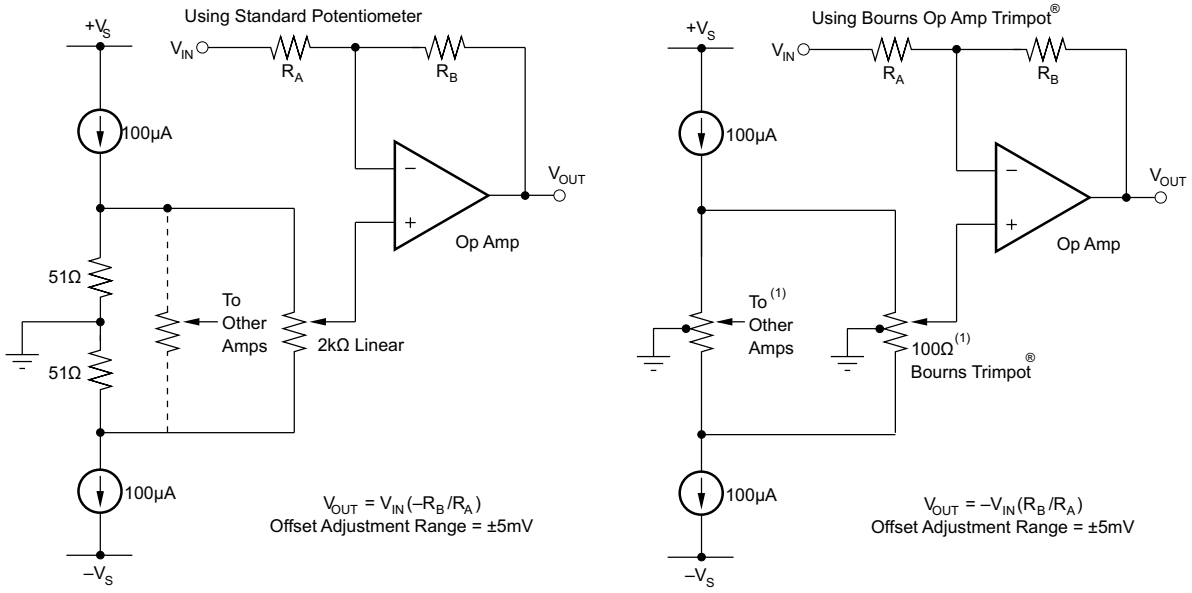
System Examples (continued)



NOTES: (1) FET cascoded current sources offer improved output impedance and high frequency operation. Circuit in (b) also provides improved PSRR. (2) For current sinks (Circuits (a) and (b) only), invert circuits and use “N” channel JFETS.

Figure 23. FET Cascode Circuits

System Examples (continued)



NOTE: (1) For N Op Amps, use Potentiometer Resistance = N • 100Ω.

Figure 24. Operational Amplifier Offset Adjustment Circuits

System Examples (continued)

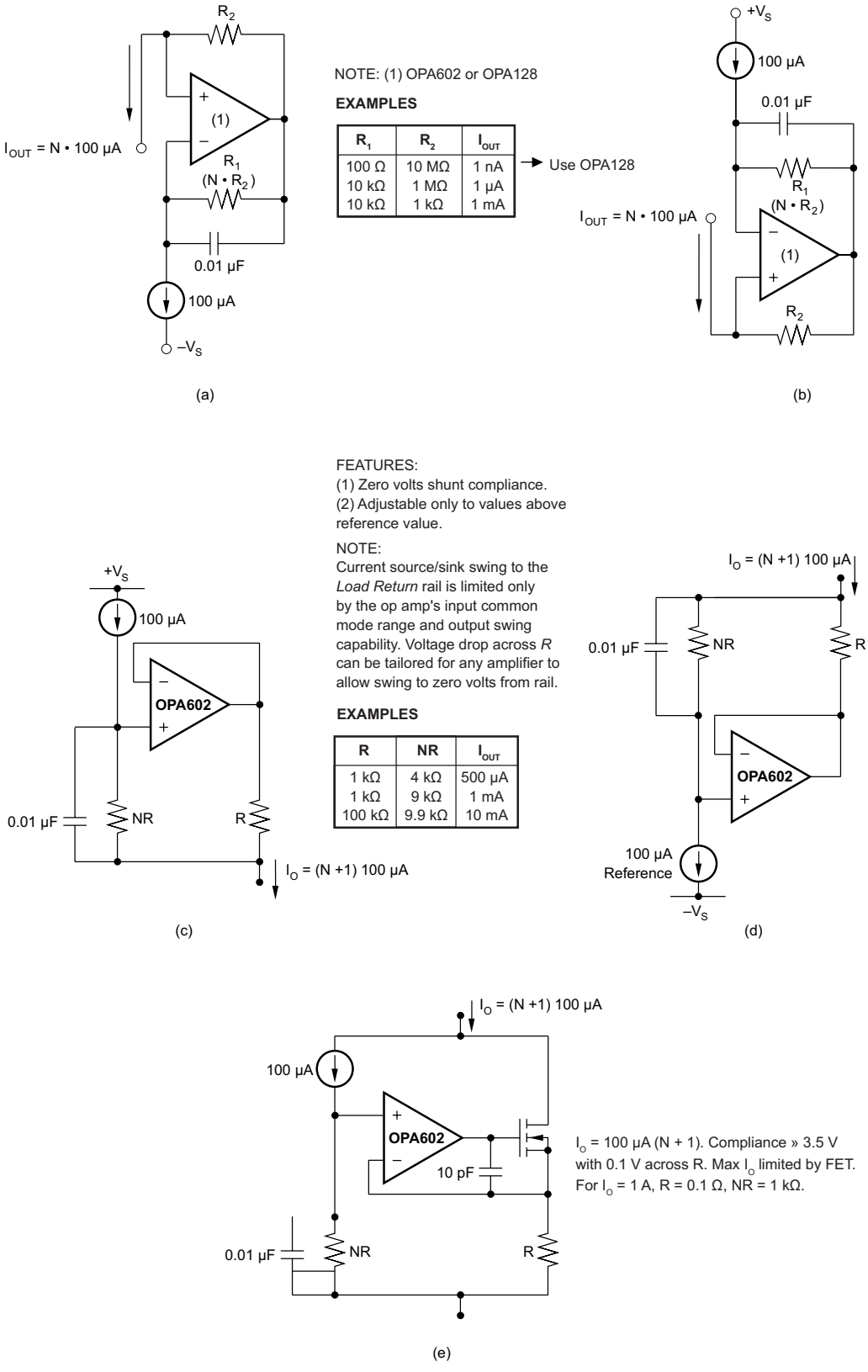


Figure 25. Adjustable Current Sources

System Examples (continued)

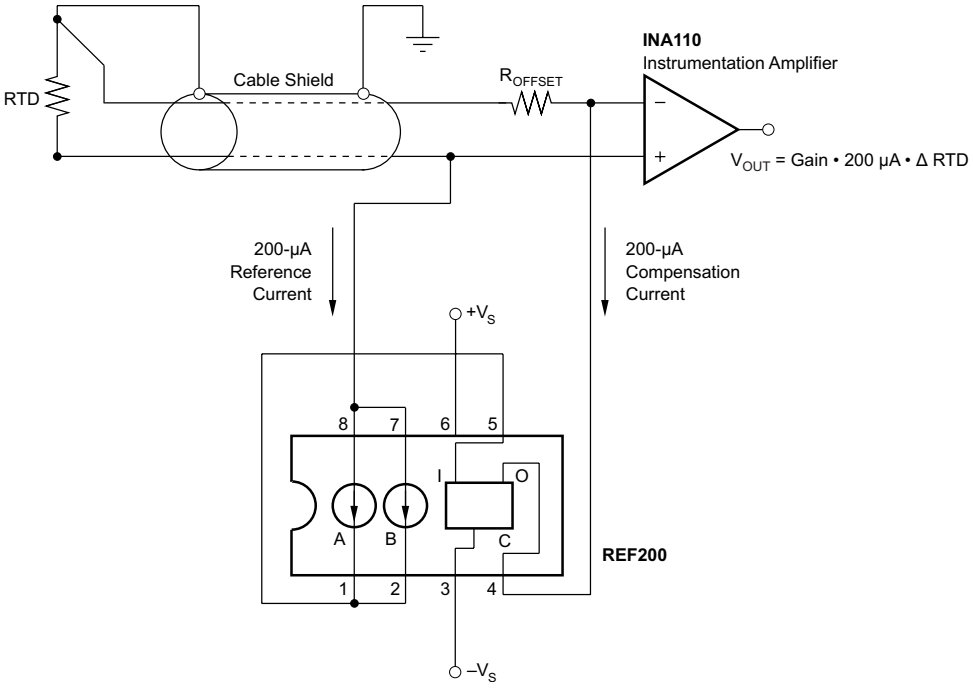
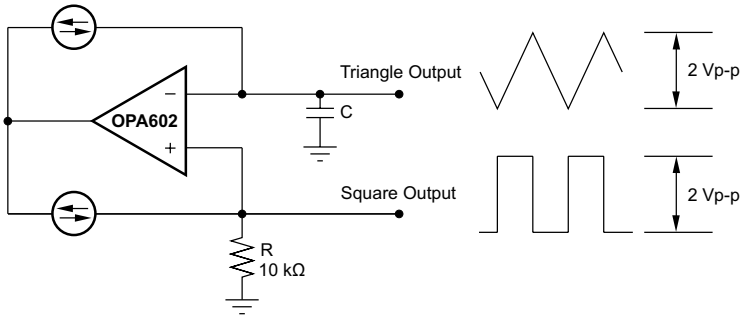


Figure 26. RTD Excitation With Three-Wire Lead Resistance Compensation



Frequency = 1/4RC (Hz)
Frequency = 25/C (Hz)
(C is in µF and R = 10 kΩ)

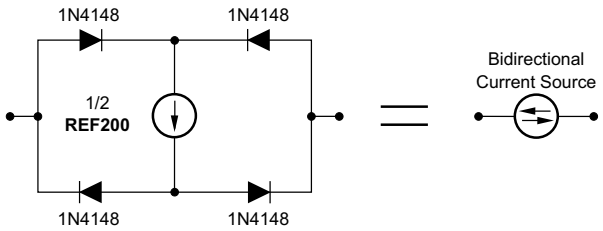
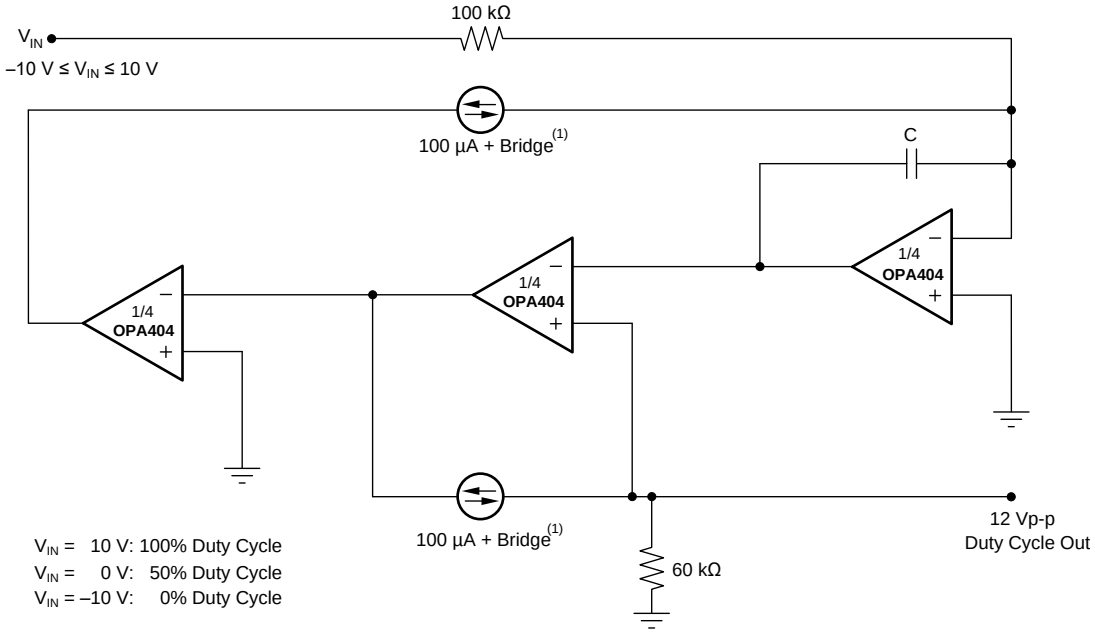


Figure 27. Precision Triangle Waveform Generator

System Examples (continued)



(1) See Figure 27.

Figure 28. Precision Duty-Cycle Modulator

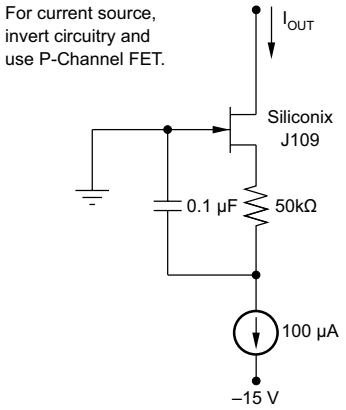


Figure 29. Low Noise Current Sink

System Examples (continued)

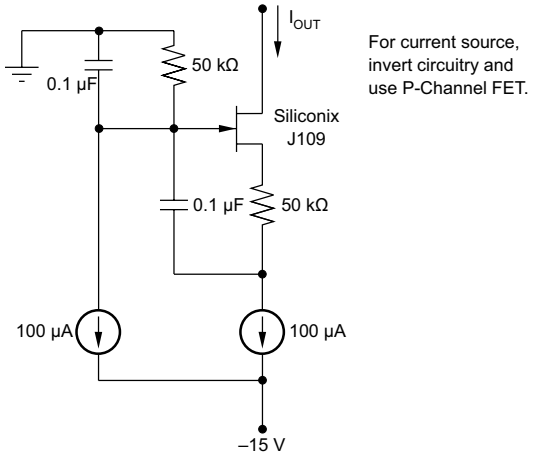
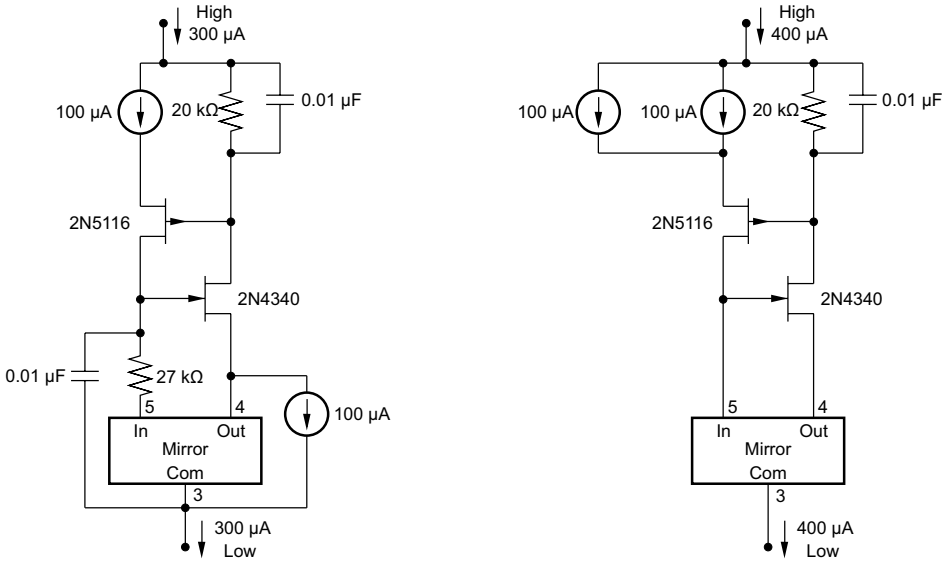


Figure 30. Low Noise Current Sink With Compliance Below Ground



(a) Regulation (15 V to 30 V = 0.00003%/V (10 GW)

(a) Regulation (15 V to 30 V = 0.000025%/V (10 GW)

Figure 31. Floating 300-µA and 400-µA Cascoded Current Sources

System Examples (continued)

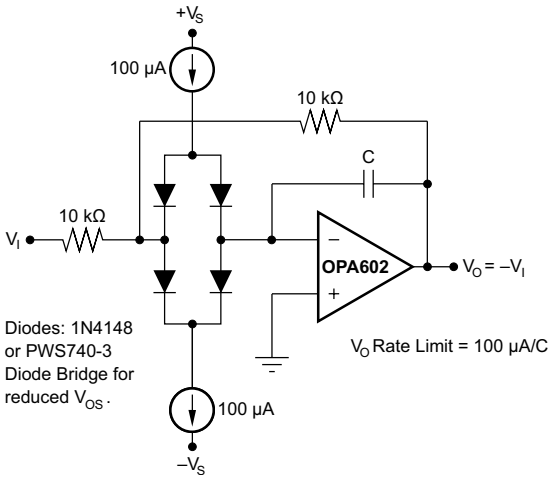


Figure 32. Rate Limiter

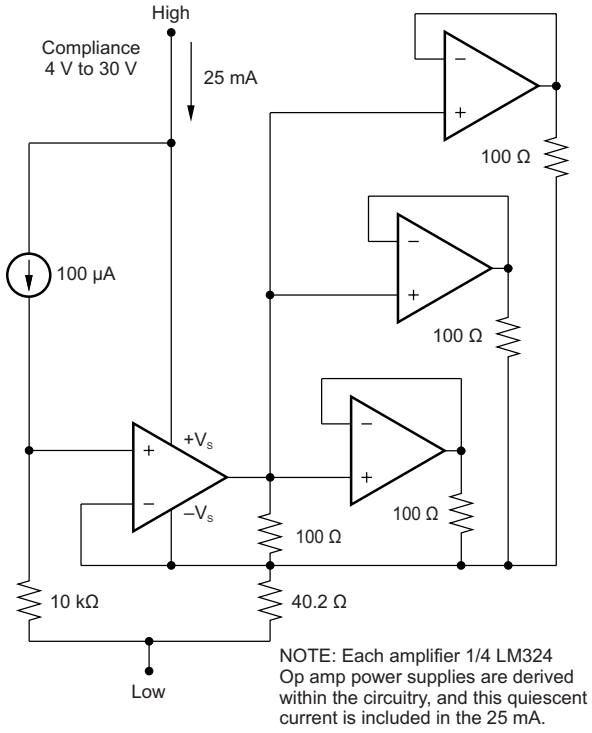


Figure 33. 25-mA Floating Current Source

System Examples (continued)

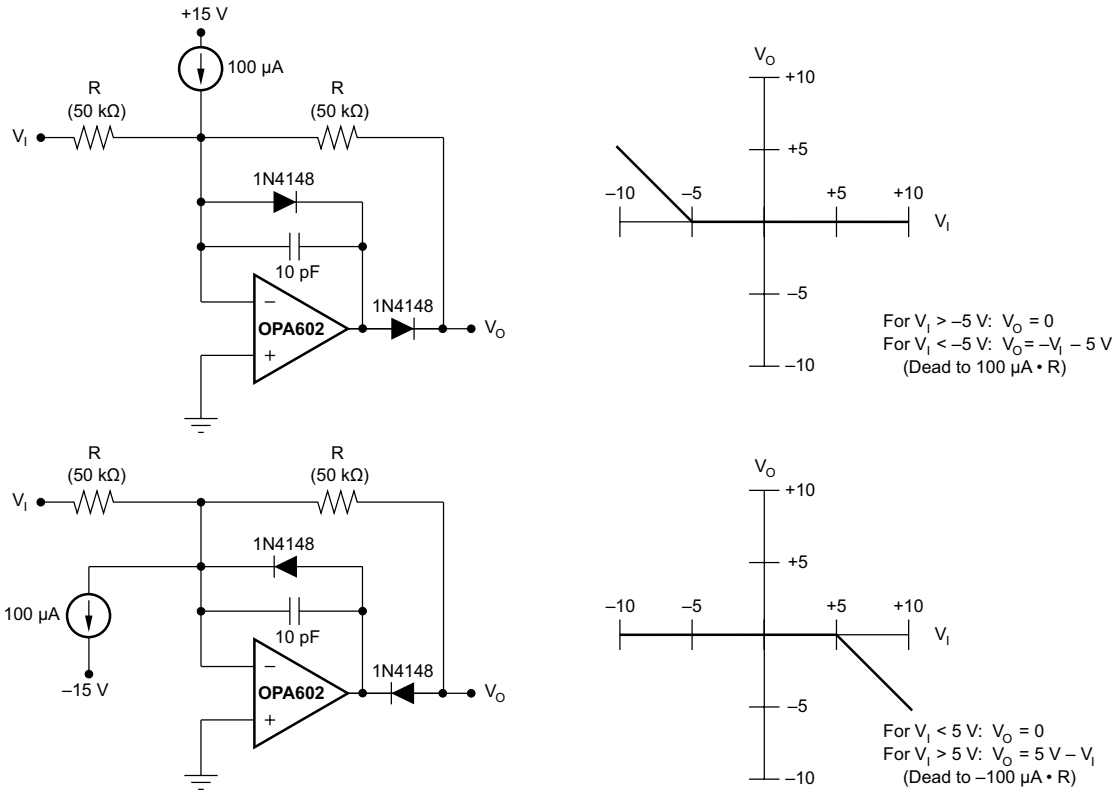


Figure 34. Dead-Band Circuit

System Examples (continued)

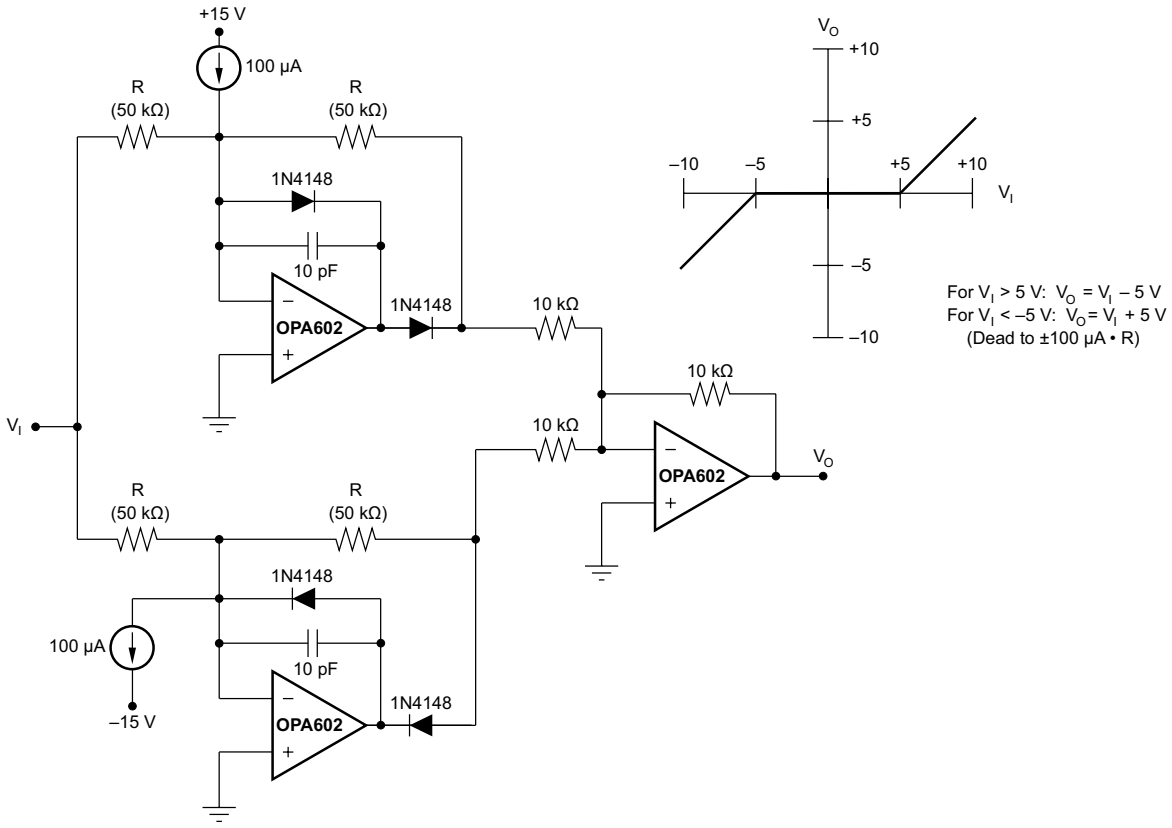


Figure 35. Double Dead-Band Circuit

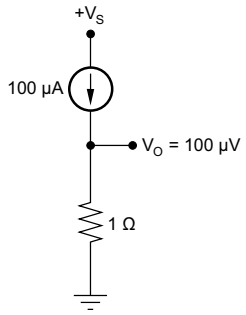


Figure 36. Low-Voltage Reference

System Examples (continued)

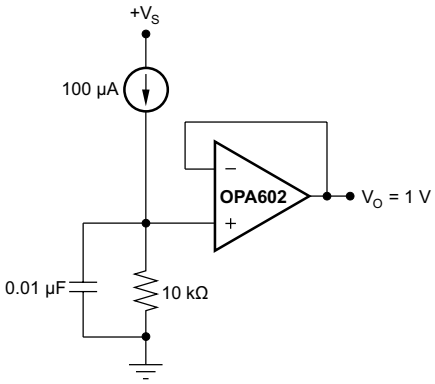
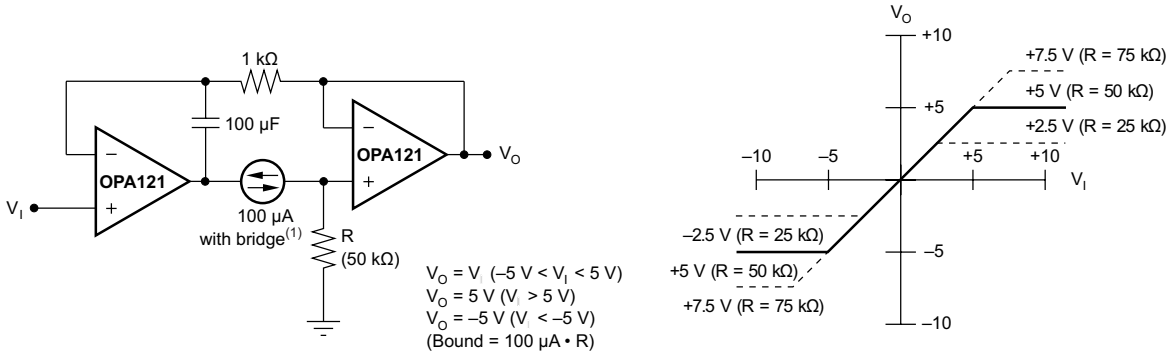


Figure 37. Voltage Reference



(1) See Figure 17.

Figure 38. Bipolar Limiting Circuit

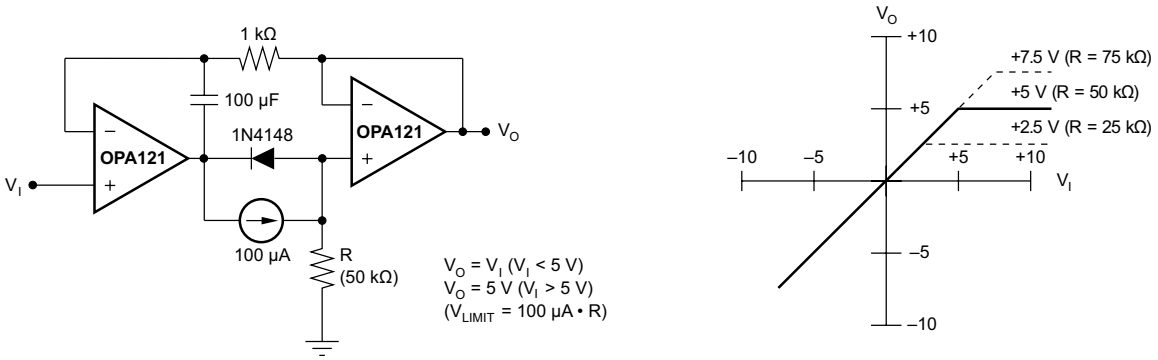


Figure 39. Limiting Circuit

System Examples (continued)

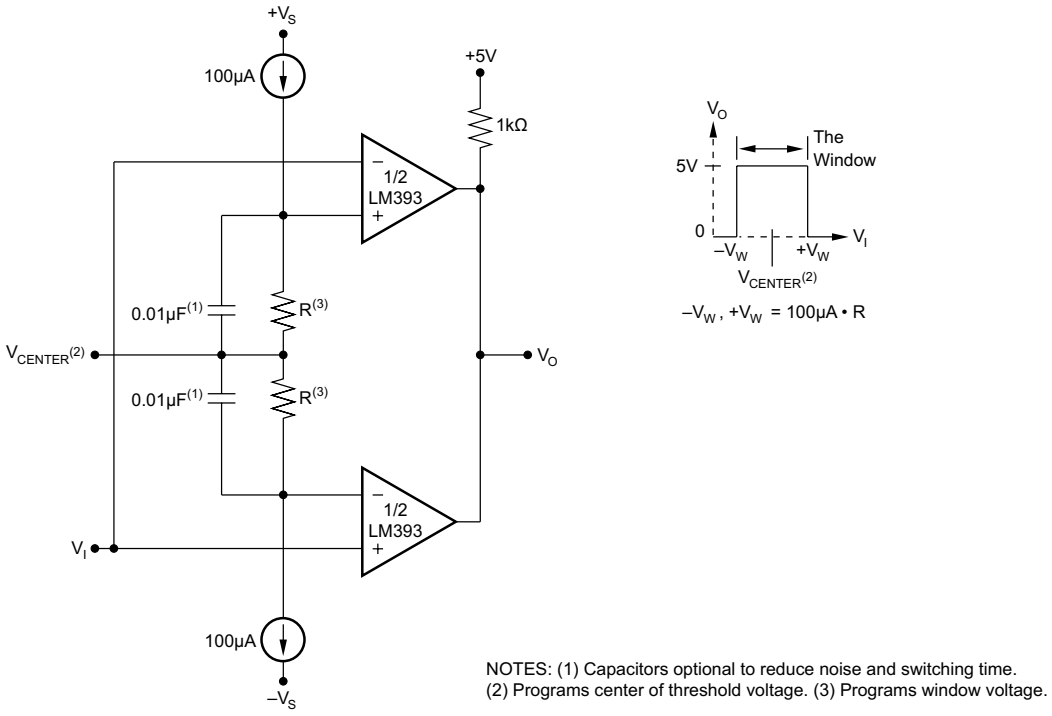


Figure 40. Window Comparator

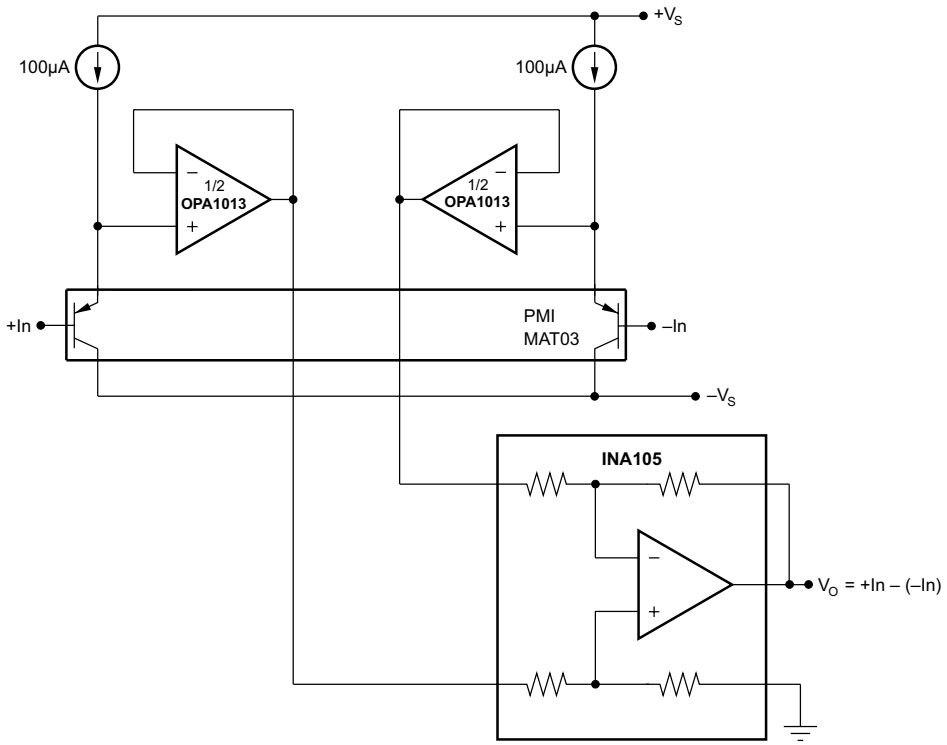


Figure 41. Instrumentation Amplifier With Compliance to $-V_S$

9 Power Supply Recommendations

The REF200 device has completely floating current sources and current mirror. The REF200 device has a wide compliance voltage range from 2.5 V to 40 V.

10 Layout

10.1 Layout Guidelines

Figure 42 illustrates an example of a printed-circuit-board (PCB) layout for a data acquisition system using the REF2030. Some key considerations are:

- Minimize trace lengths in the current source and current mirror paths to reduce impedance.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

10.2 Layout Example

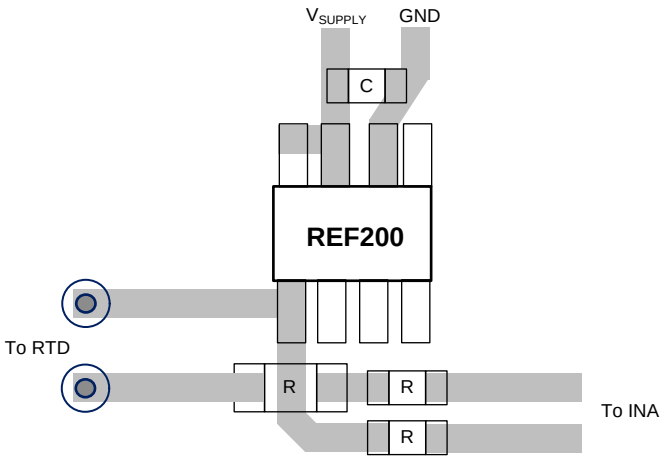


Figure 42. Example Layout of REF200 in a RTD Measurement System

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- *RTD to Voltage Reference Design Using Instrumentation Amplifier and Current Reference*, TIDU969
- *Implementation and Applications of Current Sources and Current Receivers*, SBOA046

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF200AP	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
REF200AU	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	REF 200U	Samples
REF200AU/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	REF 200U	Samples
REF200AU/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	REF 200U	Samples
REF200AUE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	REF 200U	Samples
REF200AUG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	REF 200U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

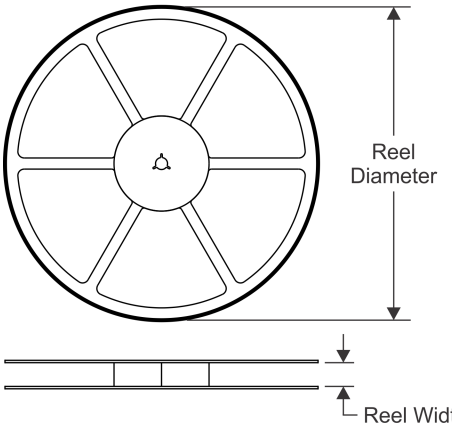
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

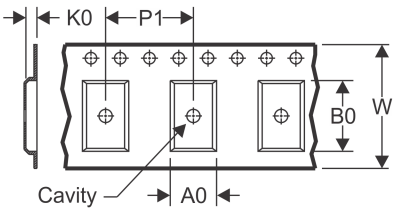
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

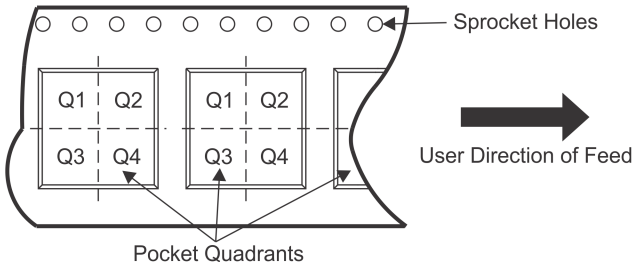


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

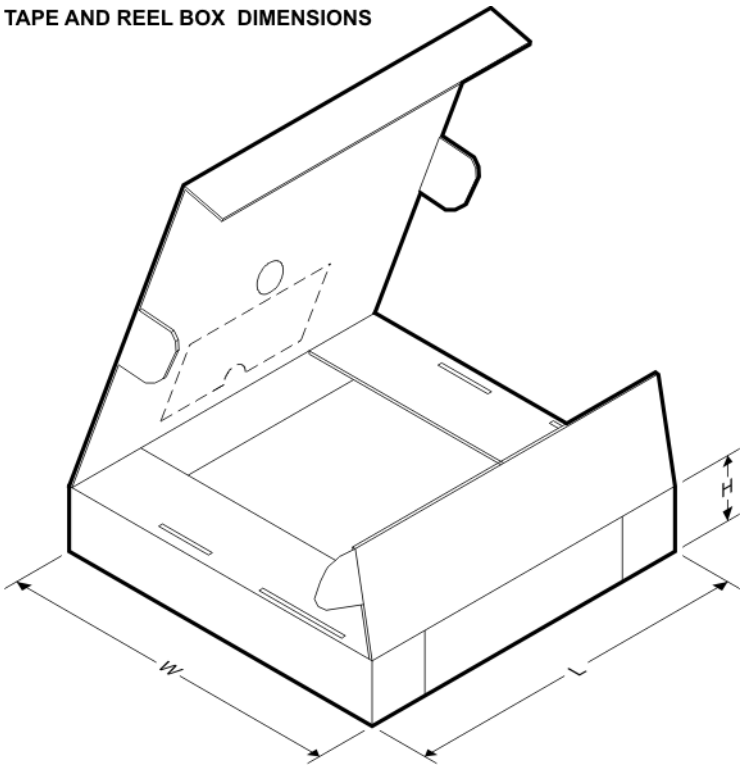
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF200AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

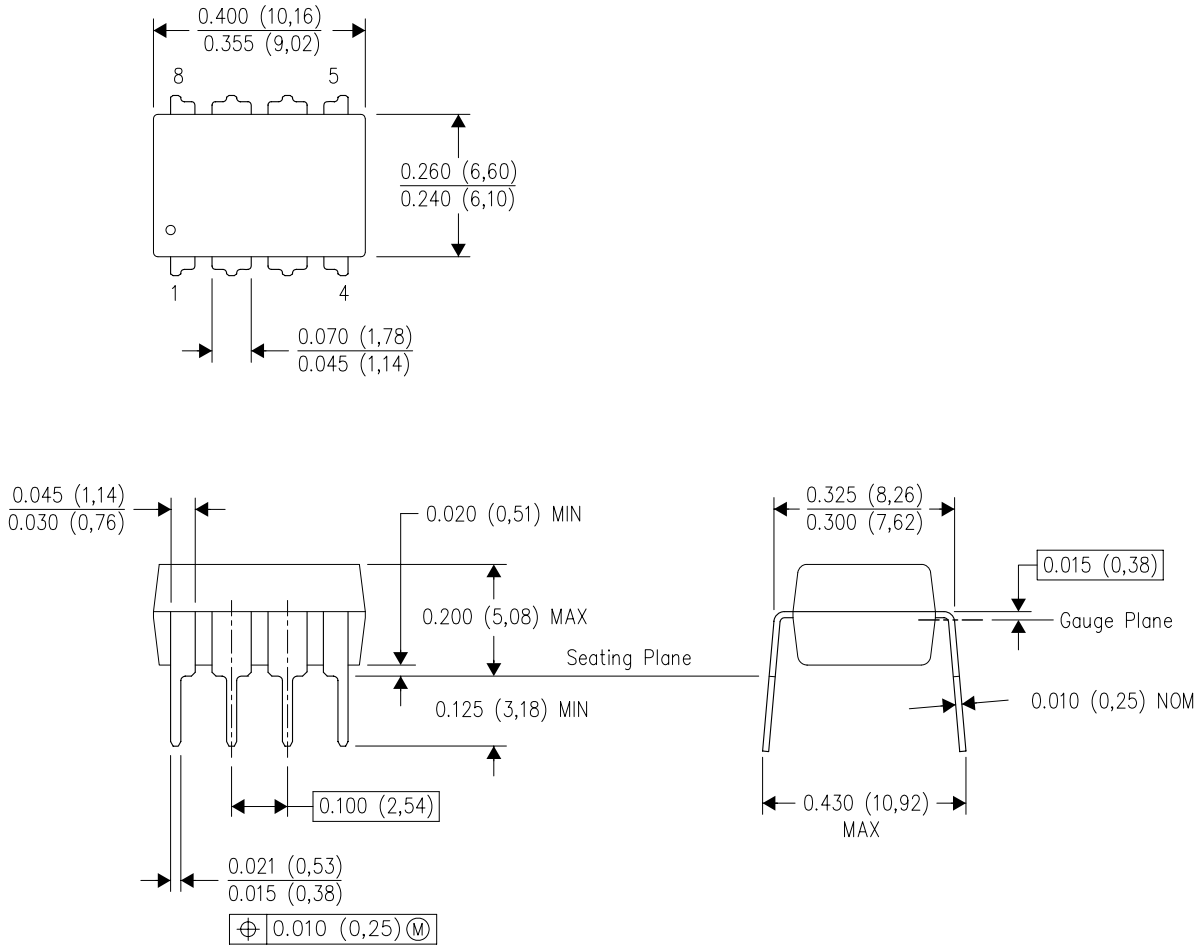
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

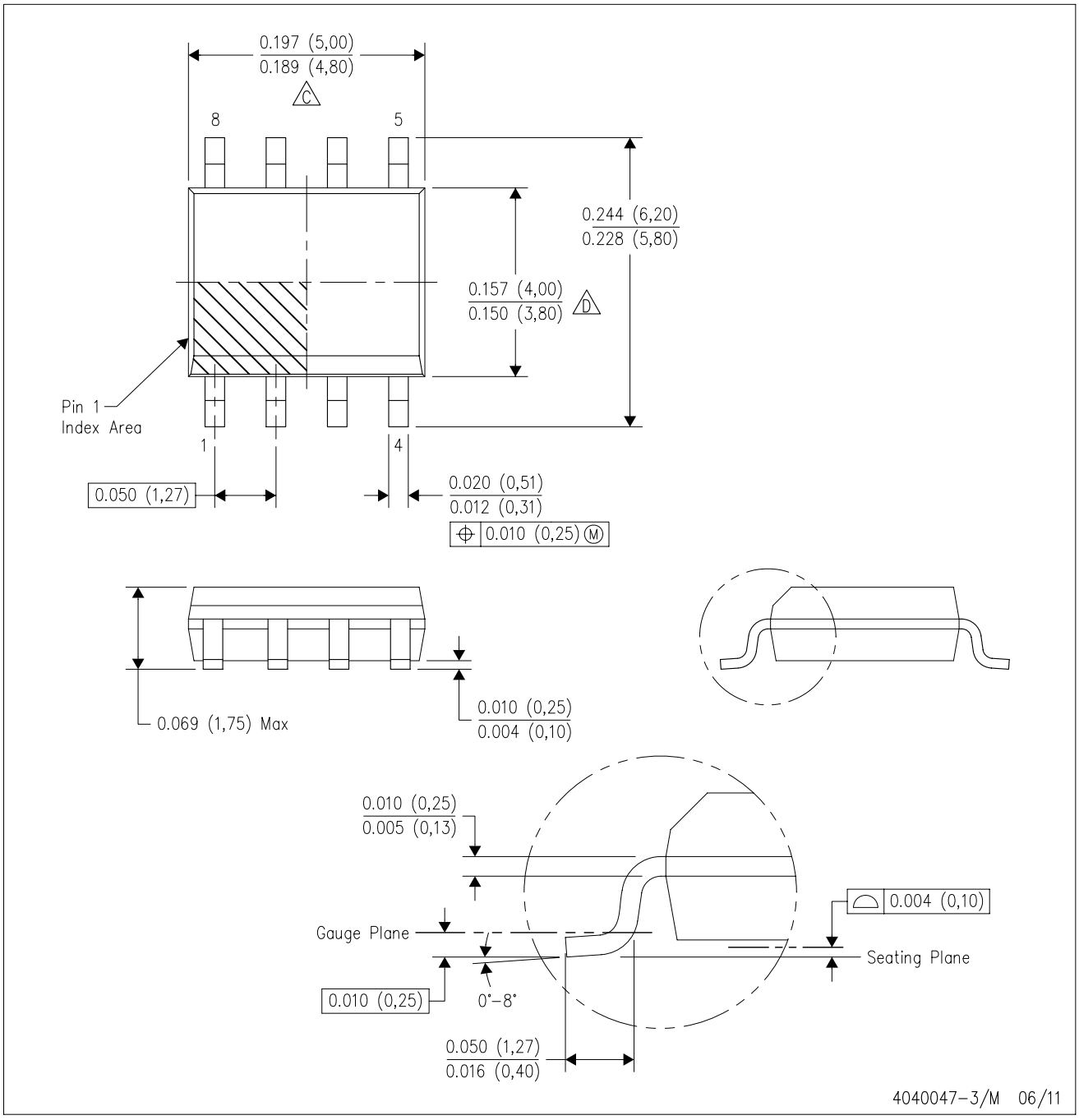
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF200AU/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



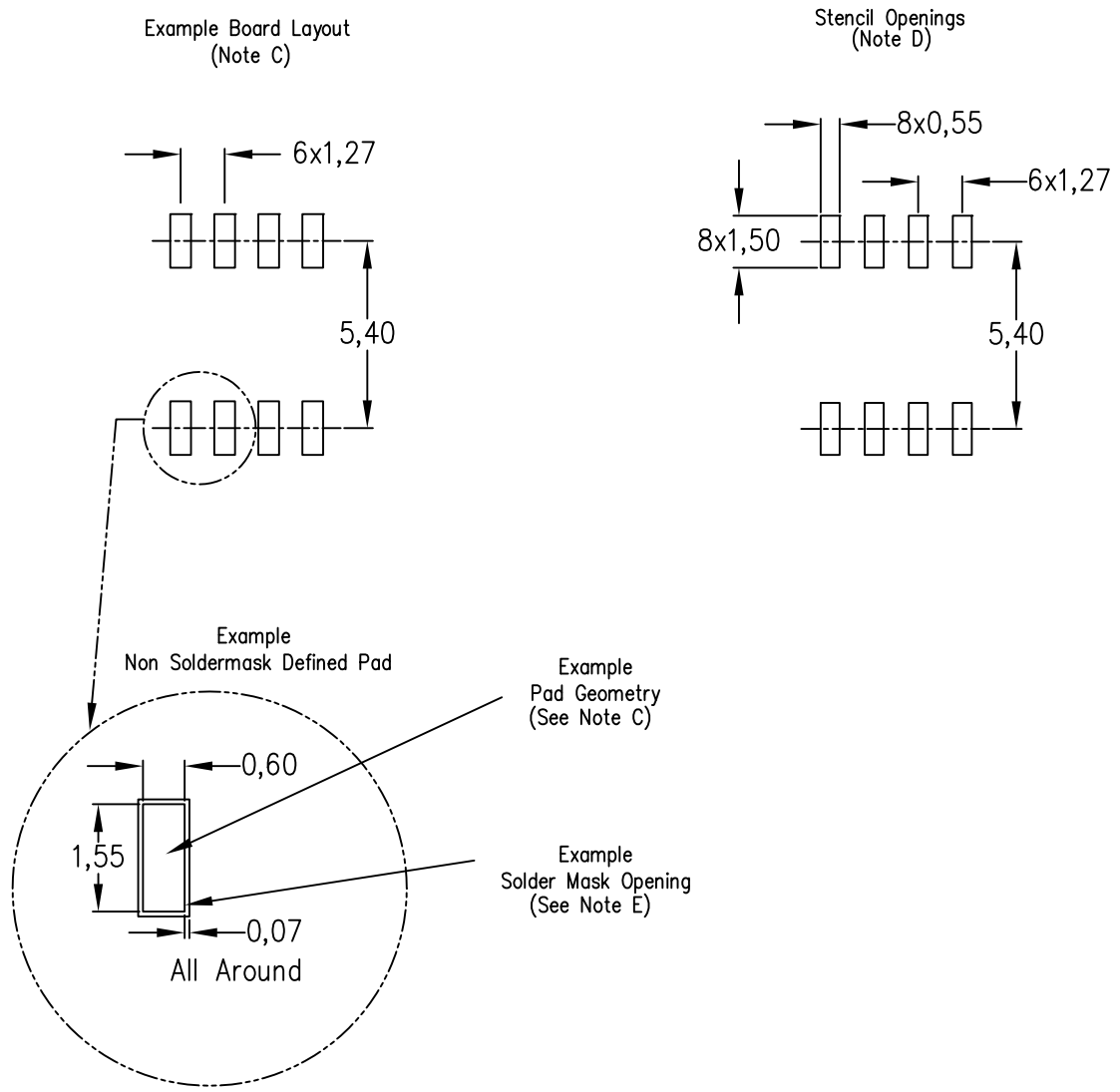
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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