SONY

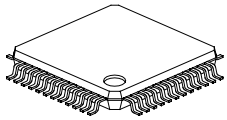
CXD3300R

10-bit 20MSPS Video A/D Converter

Description

The CXD3300R is a 10-bit CMOS A/D converter for video applications. This IC is ideally suited for the A/D conversion of video signals in TVs, VCRs, camcorders, etc.

48 pin LQFP (Plastic)



Features

- Resolution: 10 bits ± 1.0LSB (D.L.E.)
- Maximum sampling frequency: 20MSPS
- Low power consumption: 40mW
  (Except self-bias)
- Low input capacitance
- Built-in self-bias circuit

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{DD}	AV_{SS} – 0.5 to +4.5	V
	DV_{DD}	DV_{SS} – 0.5 to +4.5	V
• Reference voltage	VRT, VRB	AV_{DD} + 0.5 to AV_{SS} – 0.5	V
• Input voltage (analog)	V_{IN}	AV_{DD} + 0.5 to AV_{SS} – 0.5	V
• Input voltage (digital)	V_{IH}, V_{IL}	AV_{DD} + 0.5 to AV_{SS} – 0.5	V
• Output voltage (digital)	V_{OH}, V_{OL}	DV_{DD} + 0.5 to DV_{SS} – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

• Supply voltage	AV_{DD}, AV_{SS}	3.0 ± 0.3	V
	DV_{DD}, DV_{SS}	3.0 ± 0.3	V
	$\lvert DV_{SS} - AV_{SS} \rvert$	0 to 100	mV
• Reference input voltage	VRB	$0.3AV_{DD}$ to $0.5AV_{DD}$	V
	VRT	$0.6AV_{DD}$ to $0.8AV_{DD}$	V
• Analog input	V_{IN}	0.9Vp-p or more	
• Clock pulse width	t_{PW1}	25 (min.)	ns
	t_{PW0}	25 (min.)	ns
• Operating ambient temperature	Topr	–40 to +85	°C

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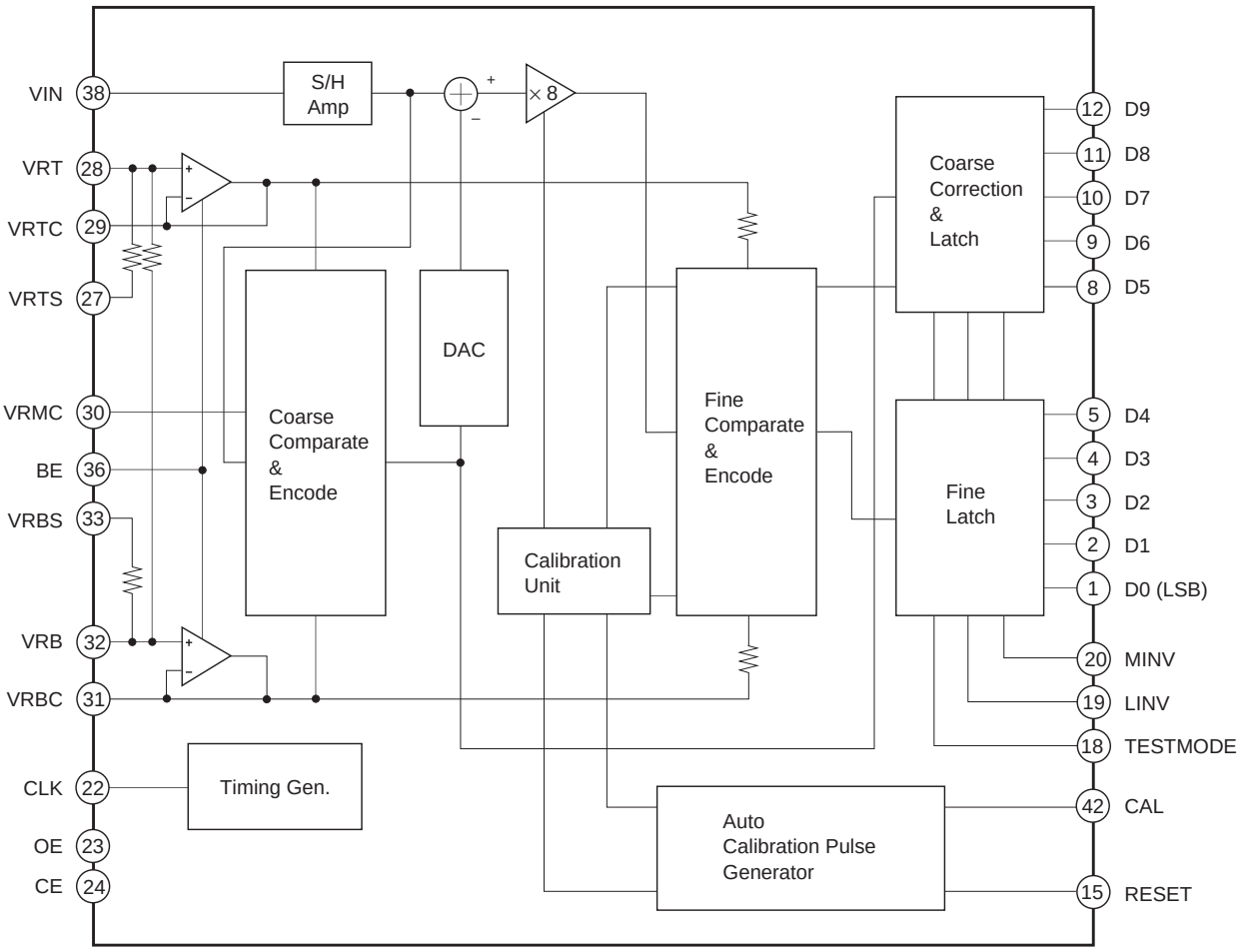
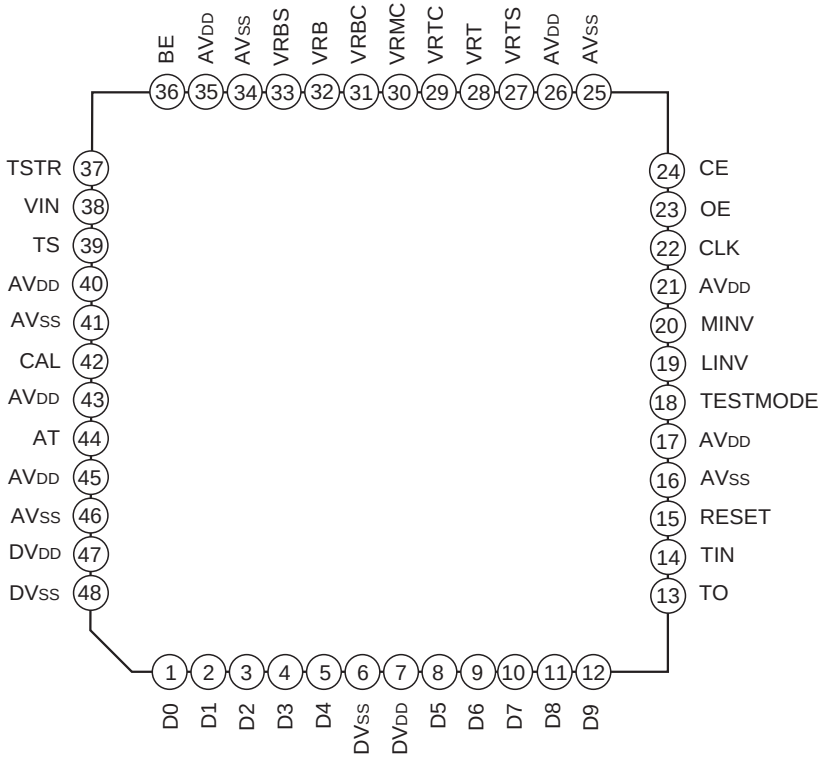
E97310-PS

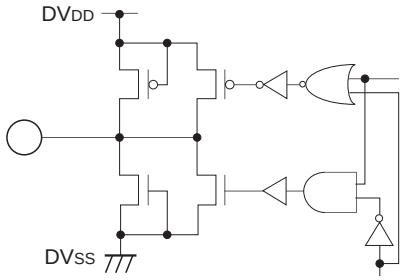
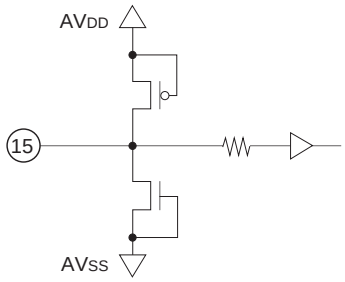
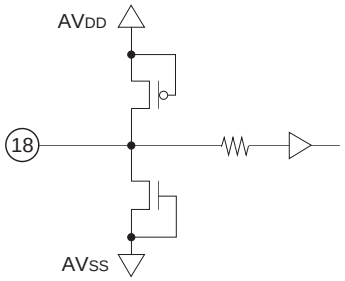
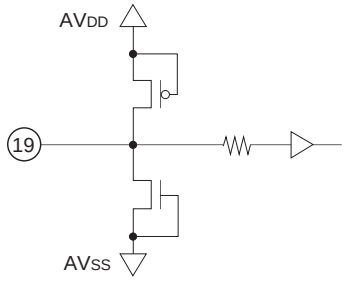
Block Diagram

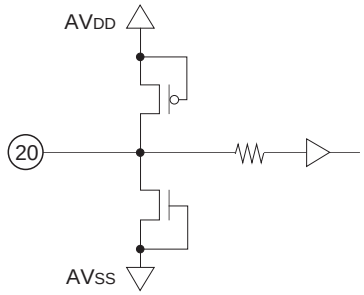
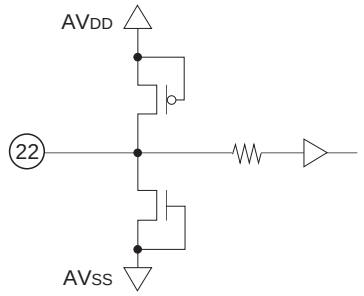
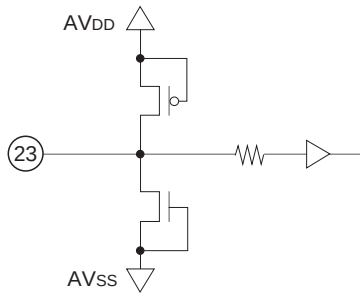
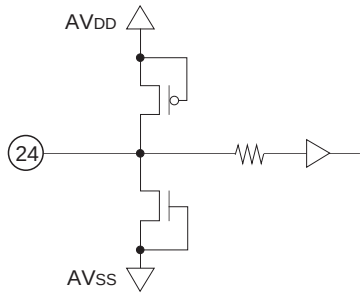


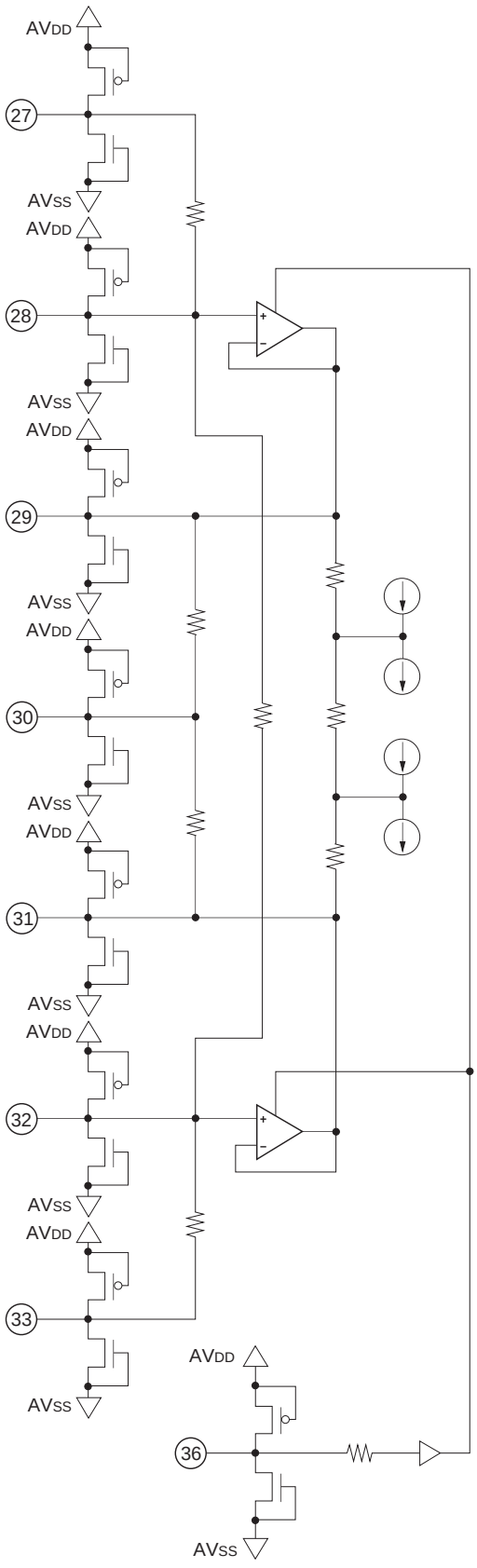
Pin Configuration

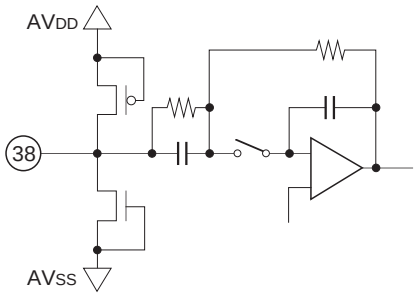
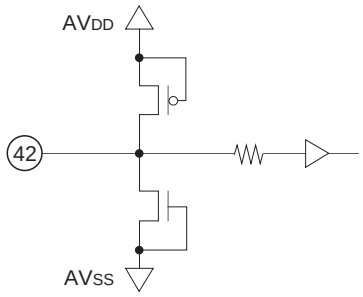


Pin Description

Pin No.	Symbol	Equivalent circuit	Description
1 to 5 8 to 12	D0 to D9		D0 (LSB) to D9 (MSB) output.
6, 48	DVSS		Digital VSS.
7, 47	DVDD		Digital VDD.
13	TO		Test pin. High impedance when TS = High.
14	TIN		Test signal input. Normally fixed to AVDD or AVSS.
15	RESET		Calibration circuit reset and startup calibration restart.
16, 25, 34, 41, 46	AVSS		Analog VSS.
17, 21, 26, 35, 40, 43, 45	AVDD		Analog VDD.
18	TESTMODE		Test mode. High: Output state Low: Output fixed
19	LINV		Output inversion. High: D0 to D8 are inverted and output. Low: D0 to D8 are normal output.

Pin No.	Symbol	Equivalent circuit	Description
20	MINV		Output inversion. High: D9 is inverted and output. Low: D9 is normal output.
22	CLK		Clock.
23	OE		D0 to D9 output enable. Low: Output state High: High impedance state
24	CE		Chip enable. Low: Active state High: Standby state

Pin No.	Symbol	Equivalent circuit	Description
27	VRTS		Self-bias. (Reference top)
28	VRT		Reference top.
29	VRTC		Reference top output.
30	VRMC		Reference middle output.
31	VRBC		Reference bottom output.
32	VRB		Reference bottom.
33	VRBS		Self-bias. (Reference bottom)
36	BE		Bias enable.

Pin No.	Symbol	Equivalent circuit	Description
37	TSTR		Test signal input. Normally fixed to AV$_{DD}$ or AV$_{SS}$.
44	AT		Test signal input. High impedance when TS = High.
38	VIN		Analog input.
42	CAL		Calibration pulse input.
39	TS		Test signal input. Normally fixed to AV$_{DD}$.

Digital Output

The following table shows the correlation between the analog input voltage and the digital output code. (TESTMODE = 1, LINV, MINV = 0)

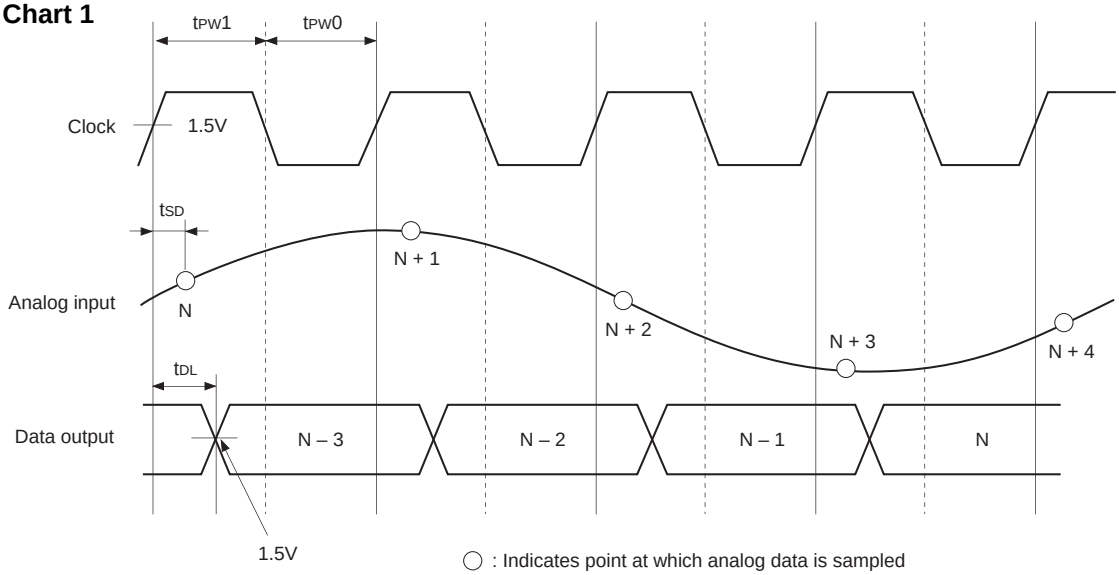
Input signal voltage	Step	Digital output code MSB LSB
VRT	1023	1 1 1 1 1 1 1 1 1 1
	512	1 0 0 0 0 0 0 0 0 0
	511	0 1 1 1 1 1 1 1 1 1
VRB	0	0 0 0 0 0 0 0 0 0 0

The following table shows the output state for the combination of TESTMODE, LINV, and MINV states.

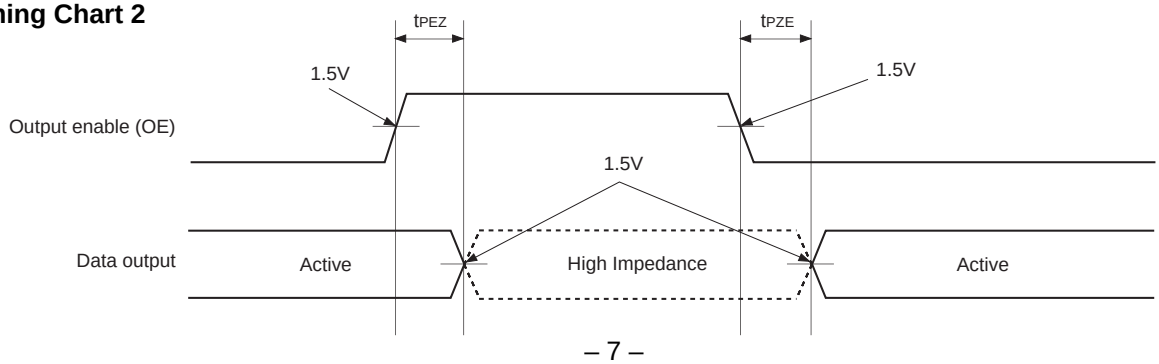
TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	P	P	P	P	P	P	P	P	P	P
1	1	0	N	N	N	N	N	N	N	N	N	P
1	0	1	P	P	P	P	P	P	P	P	P	N
1	1	1	N	N	N	N	N	N	N	N	N	N
0	0	0	1	0	1	0	1	0	1	0	1	0
0	1	0	0	1	0	1	0	1	0	1	0	0
0	0	1	1	0	1	0	1	0	1	0	1	1
0	1	1	0	1	0	1	0	1	0	1	0	1

P: Forward-phase output N: Inverted output

Timing Chart 1



Timing Chart 2



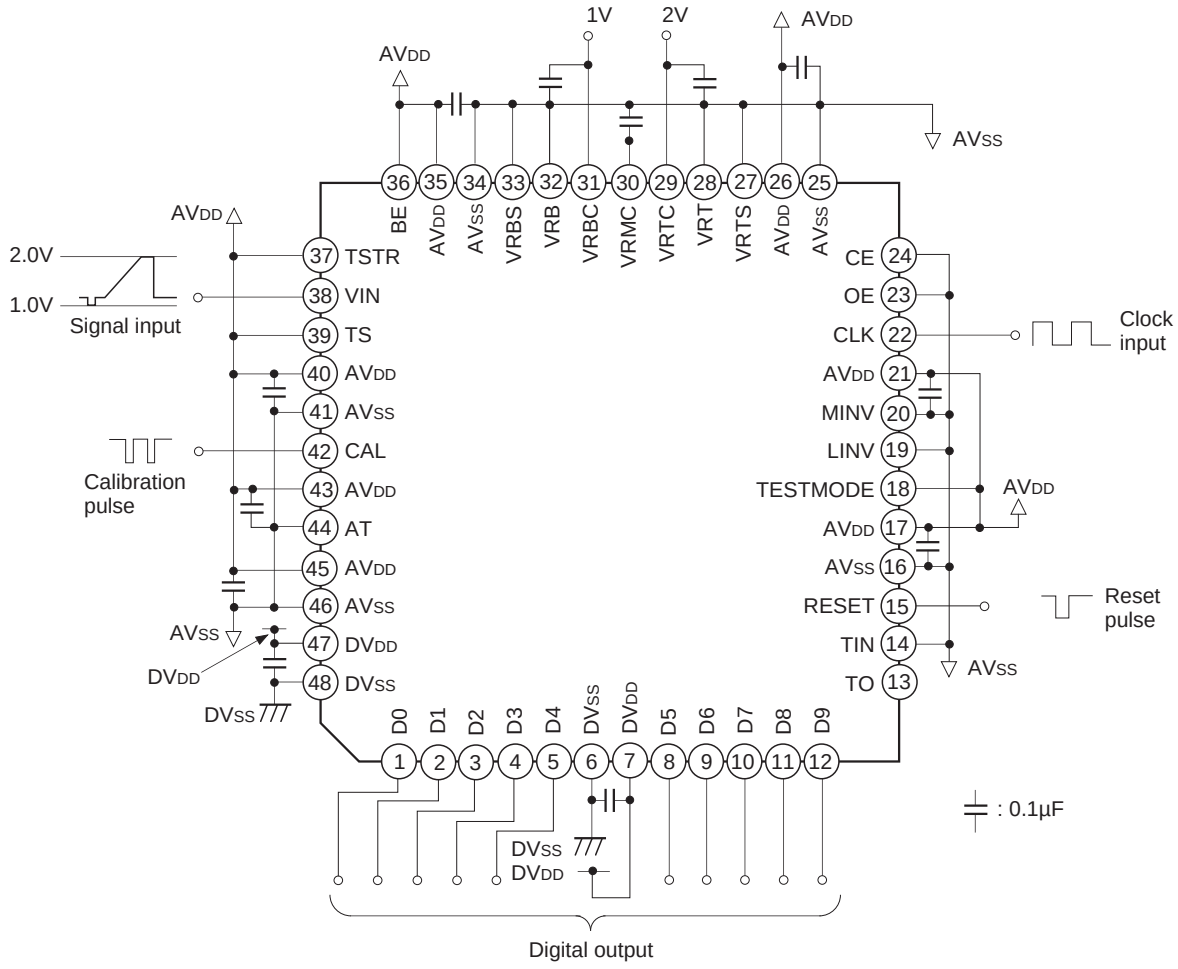
Electrical Characteristics (Fc = 20MSPS, AV_{DD} = 3V, DV_{DD} = 3V, VRB = 1V, VRT = 2V, Ta = 25°C)

Item		Symbol	Conditions		Min.	Typ.	Max.	Unit
Maximum conversion rate		Fc max	F_{IN} = 1.0kHz sine wave input		20			MSPS
Minimum conversion rate		Fc min					0.5	
Supply current	Analog	I_{ADD}	F_{IN} = 1.0kHz sine wave input BE = High		11	14	17	mA
	Digital	I_{DDD}				1.0	4	
Standby current	Analog	I_{AST}	CE = AV_{DD}				3.0	mA
	Digital	I_{DST}					1.0	µA
Reference pin current 1		$I_{RT}1$	VRTS, VRBS: Open Between VRT and VRB		87	97	111	µA
		$I_{RB}1$			–111	97	–87	
Reference pin current 2		$I_{RT}2$	BE = AV_{DD} Between VRTC and VRBC		1.81	2.04	2.33	mA
		$I_{RB}2$			–2.33	–2.04	1.81	
Analog input band		BW	–1dB			85		MHz
Analog input capacitance		C_{IN}				10		pF
Reference resistance value 1		$R_{REF}1$	Between VRTS and VRT, VRT and VRB, VRB and VRBS		9k	10.3k	11.5k	Ω
Reference resistance value 2		$R_{REF}2$	Between VRTC and VRBC		430	490	550	Ω
Offset voltage1		E_{OT1}	BE = AV_{DD} E_{OT1} = Theoretical value – Measured value		–30	+5	+40	mV
		E_{OB1}	E_{OB1} = Measured value – Theoretical value		–30	+5	+40	
Offset voltage2		E_{OT2}	BE = AV_{SS} E_{OT2} = Theoretical value – Measured value		–30	+5	+40	mV
		E_{OB2}	E_{OB2} = Measured value – Theoretical value		–20	+10	+40	
Digital input voltage		V_{IH}	AV_{DD} = 2.7 to 3.3V		0.7AV_{DD}			V
		V_{IL}					0.2AV_{DD}	
Analog input current		A_{IH}	V_{IN} = 2V		40	48	55	µA
		A_{IL}	V_{IN} = 1V		–55	–48	–40	
Digital input current		I_{IH}	AV_{DD} = 3.3V	V_{IH} = AV_{DD}			5	µA
		I_{IL}		V_{IL} = AV_{SS}			5	
Digital output current		I_{OH}	OE = AV_{SS} DV_{DD} = 2.7V	V_{OH} = DV_{DD} – 0.4V	1.0			mA
		I_{OL}		V_{OL} = 0.4V	1.0			
Digital output current		I_{OZH}	OE = AV_{DD} DV_{DD} = 3.3V	V_{OH} = DV_{DD}			1	µA
		I_{OZL}		V_{OL} = 0V			1	
Tri-state output disable time		t_{PEZ}	Clock not synchronized for active → high impedance		6	8	10	ns
Tri-state output enable time		t_{PZE}	Clock not synchronized for high impedance → active		3	5	7	ns
Integral nonlinearity error		E_L				±1.0	±3.0	LSB
Differential nonlinearity error		E_D				±0.5	±1.0	LSB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Differential gain error	DG	NTSC 40 IRE mod ramp, Fc = 14.3MSPS		1.0		%
Differential phase error	DP			0.3		deg
Output data delay	t_{DL}	C_L = 3pF, Ta = –40 to +85°C	6	9	18	ns
Sampling delay	t_{SD}		6	7	8	ns
SNR	SNR	F_{IN} = 100kHz		50		dB
		F_{IN} = 500kHz		50		
		F_{IN} = 1MHz		50		
		F_{IN} = 3MHz		50		
		F_{IN} = 7MHz		45		
		F_{IN} = 10MHz		44		
SFDR	SFDR	F_{IN} = 100kHz		52		dB
		F_{IN} = 500kHz		52		
		F_{IN} = 1MHz		52		
		F_{IN} = 3MHz		52		
		F_{IN} = 7MHz		49		
		F_{IN} = 10MHz		50		

Application Circuit 1

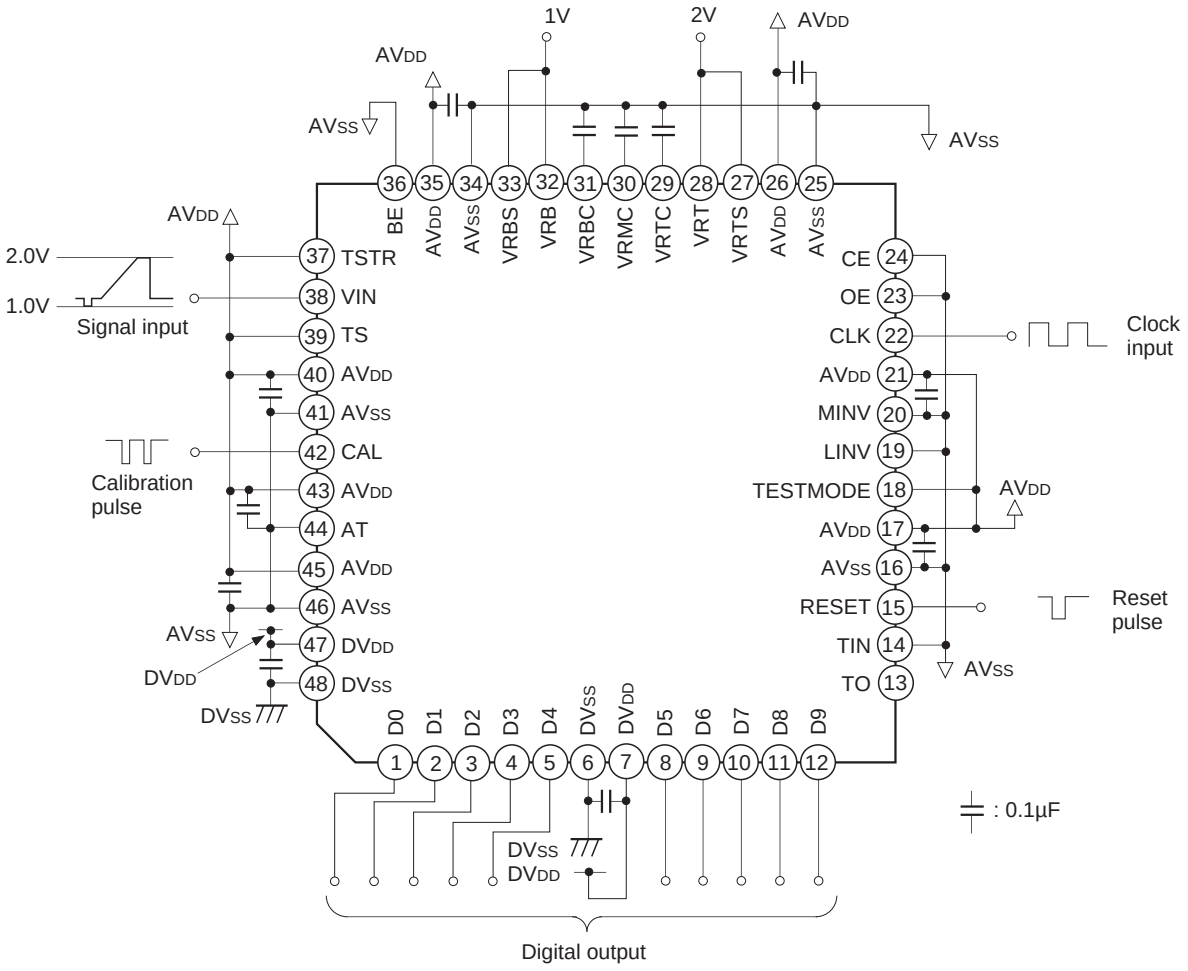
When not using self-bias and the internal bias circuits, and supplying the reference voltage from an external source.



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2

When not using self-bias circuit, using only the internal bias circuit, and supplying the reference voltage from an external source.



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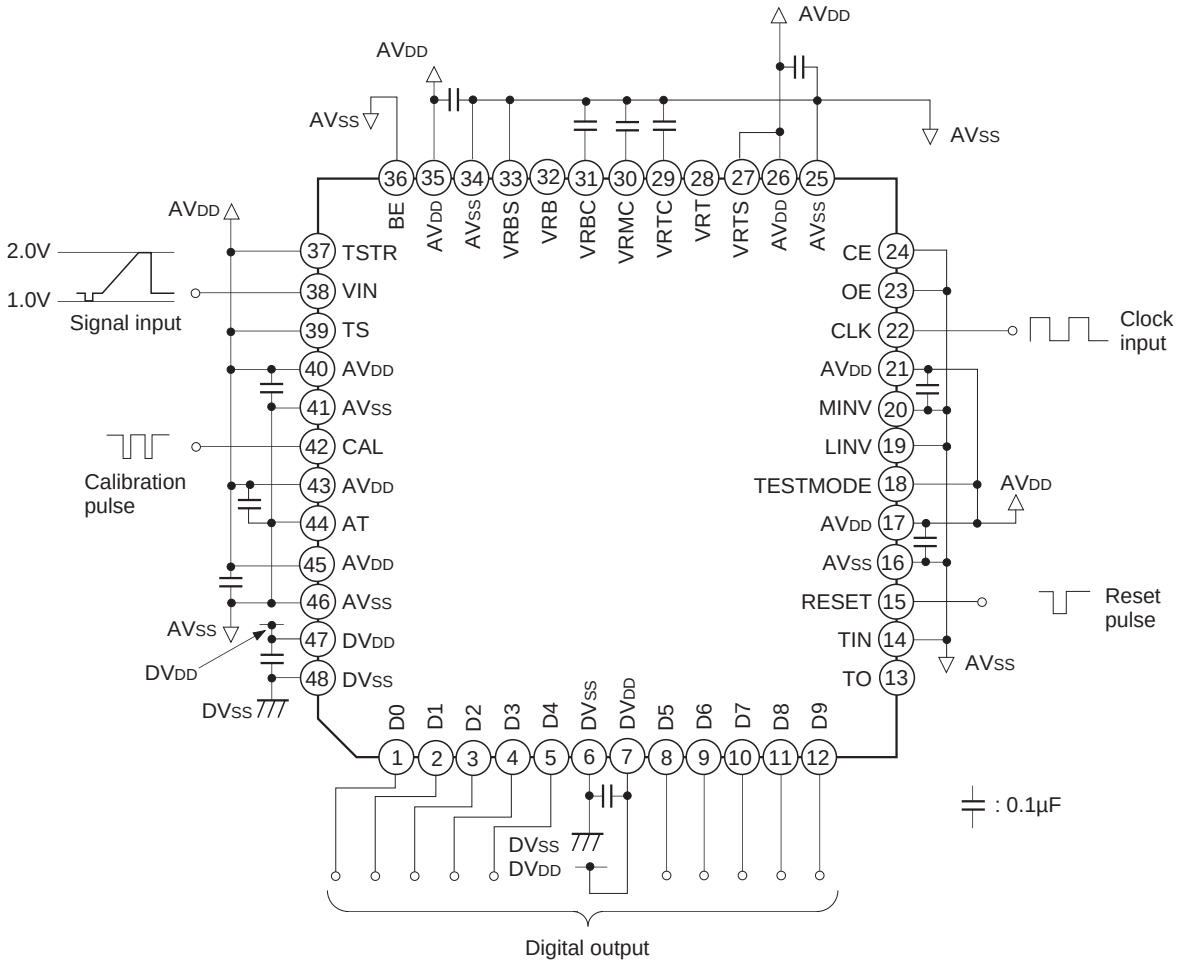
Application Circuit 3

When using the self-bias and internal bias circuits, and supplying the reference voltage.



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1. Calibration function

1) Activating startup calibration

To achieve superior linearity, the CXD3300R has a built-in calibration circuit. When using this IC, therefore, startup calibration must be activated when the power supply and reference voltage have risen and stabilized. Care should be taken as only the upper five bits may be output in the worst case if startup calibration is not activated.

Startup calibration can be activated either at the rise of the RESET pin (Pin 15) or at the fall of the CE pin (Pin 24). The startup calibration activation method for each case is shown in Fig. 1.

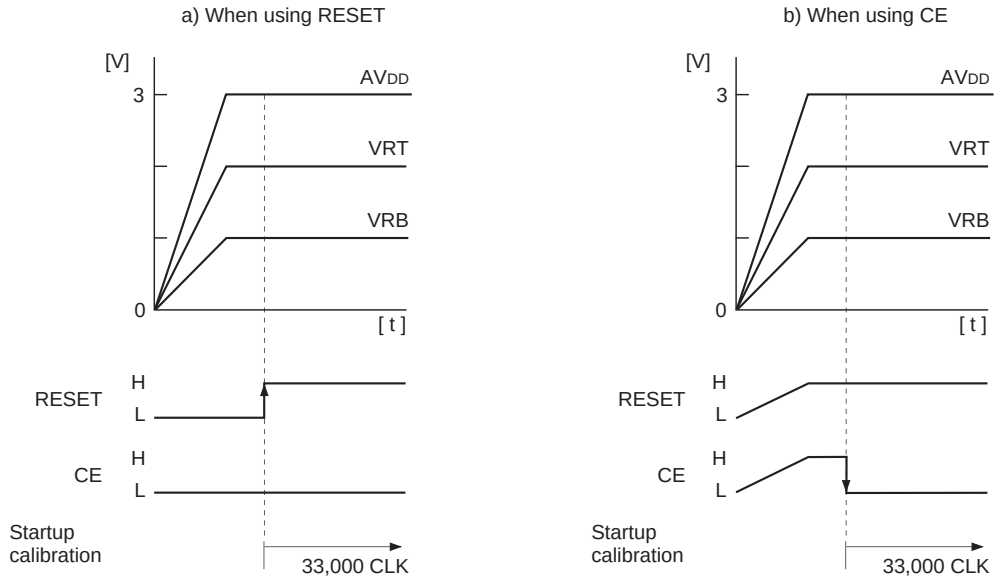


Fig. 1. Startup Calibration Activation Methods

As shown in the figure above, startup calibration must be activated after the supply voltage has risen and stabilized (full scale of 90% or more). After activation, startup calibration is performed for an interval of about 33,000 clocks. Therefore, care should be taken as the output data during this interval (about 2.3ms at 14.3MHz) cannot be used.

2) Calibration pulse supply

The IC's operating status with changes due to fluctuations in the supply voltage and ambient temperature during use can be constantly monitored and then compensated appropriately by inputting a pulse at regular intervals to the CAL pin (Pin 41). Fig. 2 shows the timing chart.

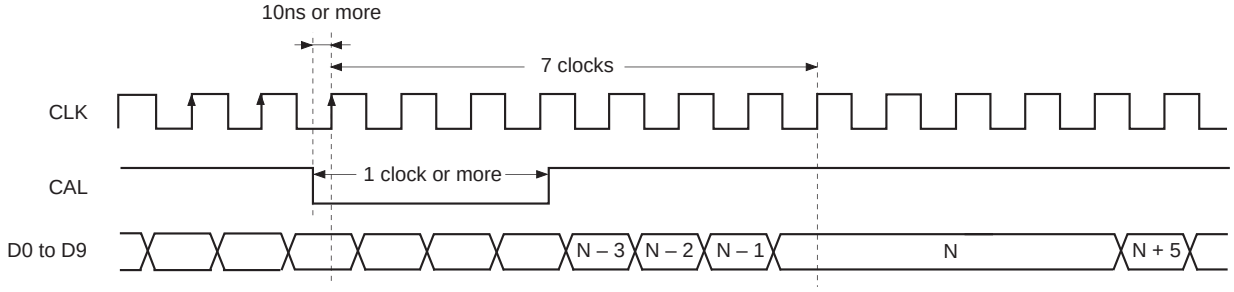
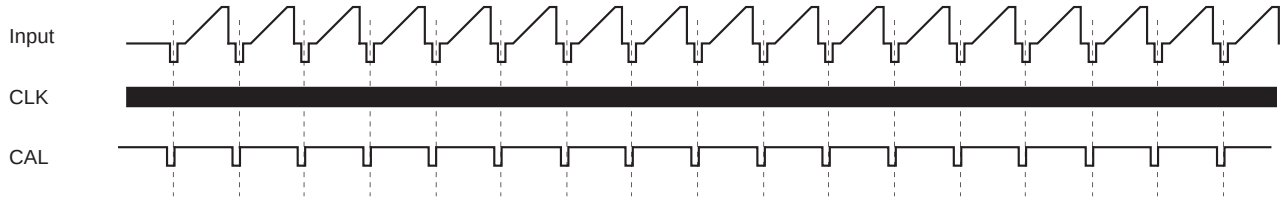


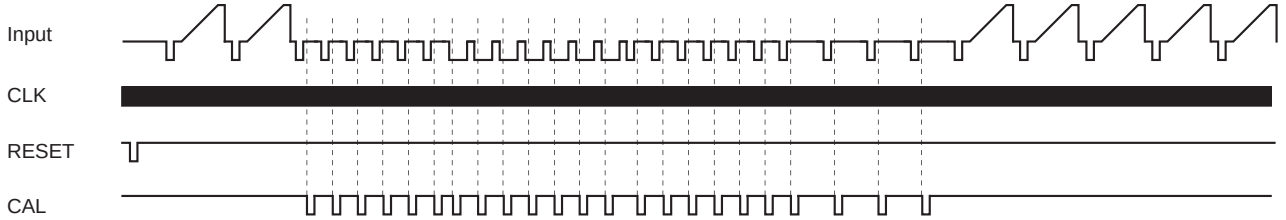
Fig. 2. Calibration Timing Chart

Calibration starts when the fall of the pulse input to the CAL pin (Pin 41) is detected at the clock rise. At this time, the comparator is used in an exclusive manner for a four clock interval. So, the output data holds the immediately previous data for a four clock interval after seven clocks from the rise of the clock where the fall of the calibration pulse was detected, and then the data during this interval is missing.
Therefore, the effects of this function can be avoided by inputting a sync or other signal as the calibration pulse so that calibration is performed outside of the interval of the actually used video signal. An input example is shown below.

[1] Input every H sync



[2] Input every V sync



2. Latch-up

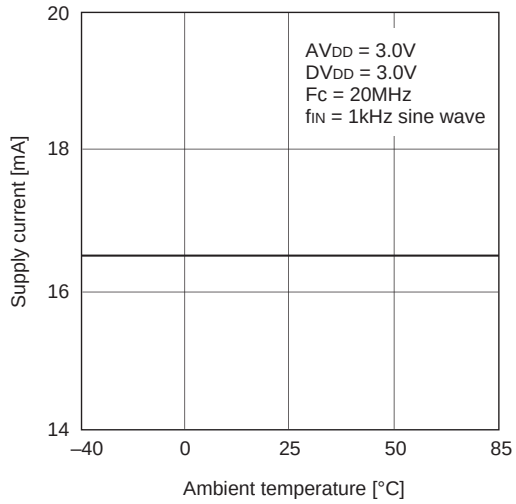
Ensure that the AV_{DD} and DV_{DD} pins share the same power supply on a board to prevent latch-up which may be caused by power-ON time lag.

3. Board

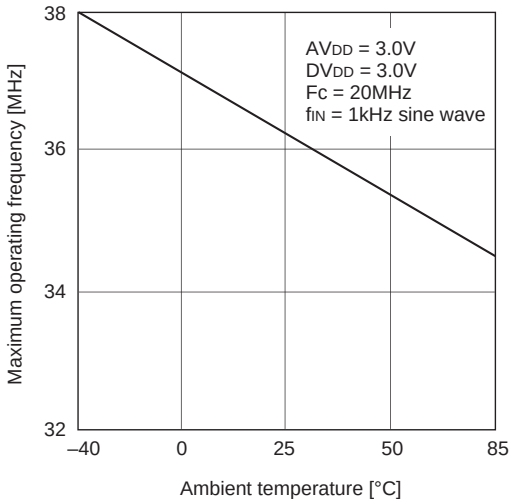
To obtain full-expected performance from this IC, be sure that the mounting board has a large ground pattern for lower impedance. It is recommended that the IC be mounted on a board without using a socket to evaluate its characteristics adequately.

Example of Representative Characteristics

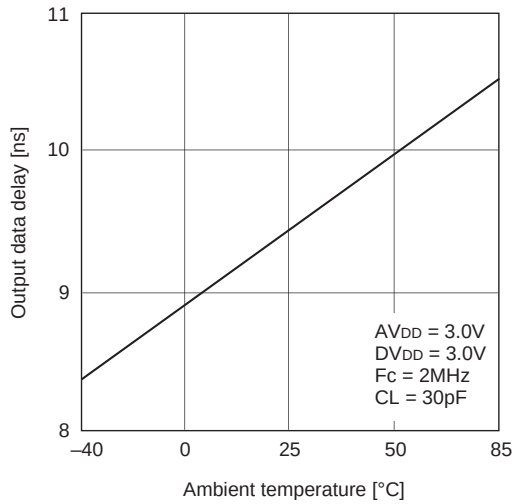
Supply current vs. Ambient temperature



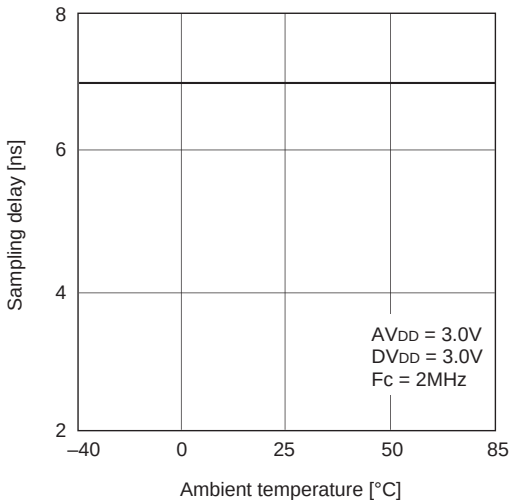
Maximum operating frequency vs. Ambient temperature



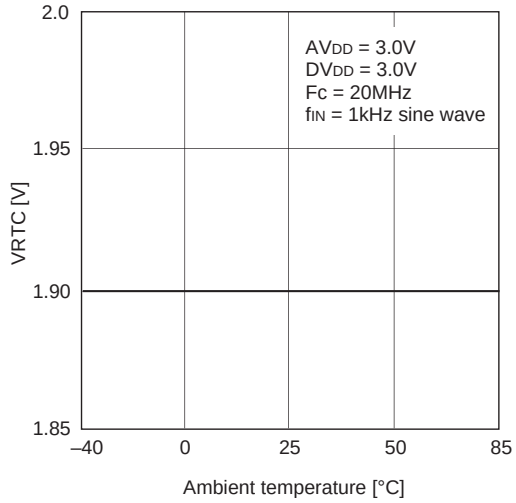
Output data delay vs. Ambient temperature



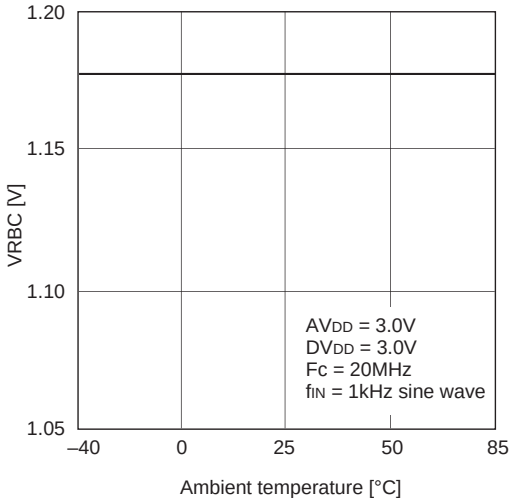
Sampling delay vs. Ambient temperature



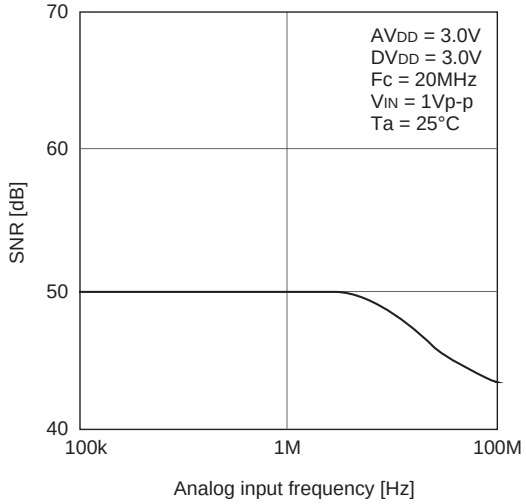
VRTC vs. Ambient temperature



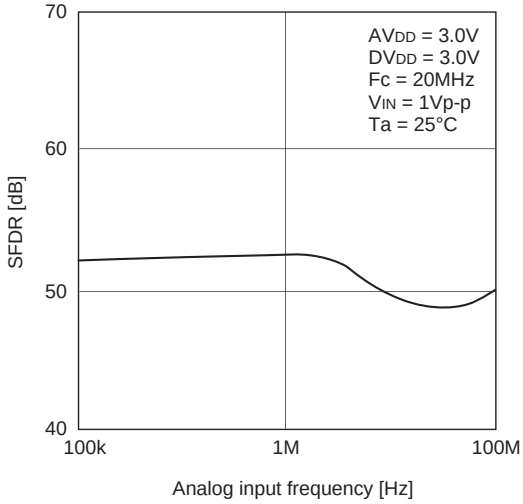
VRBC vs. Ambient temperature



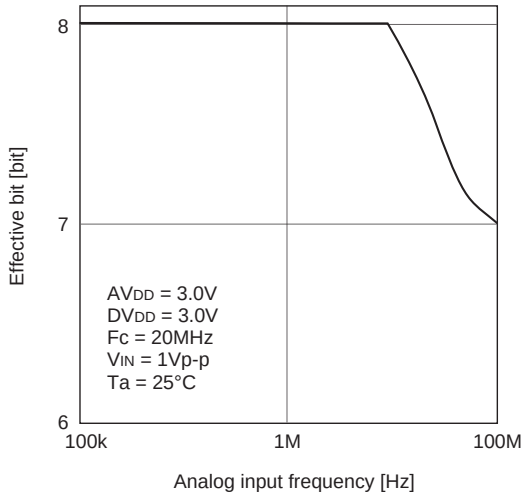
SNR vs. Analog input frequency



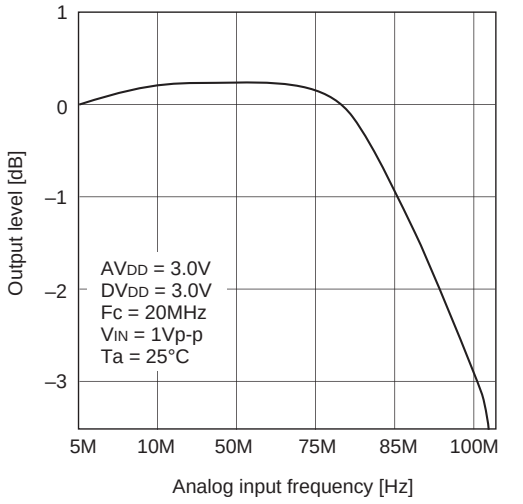
SFDR vs. Analog input frequency



Effective bit vs. Analog input frequency

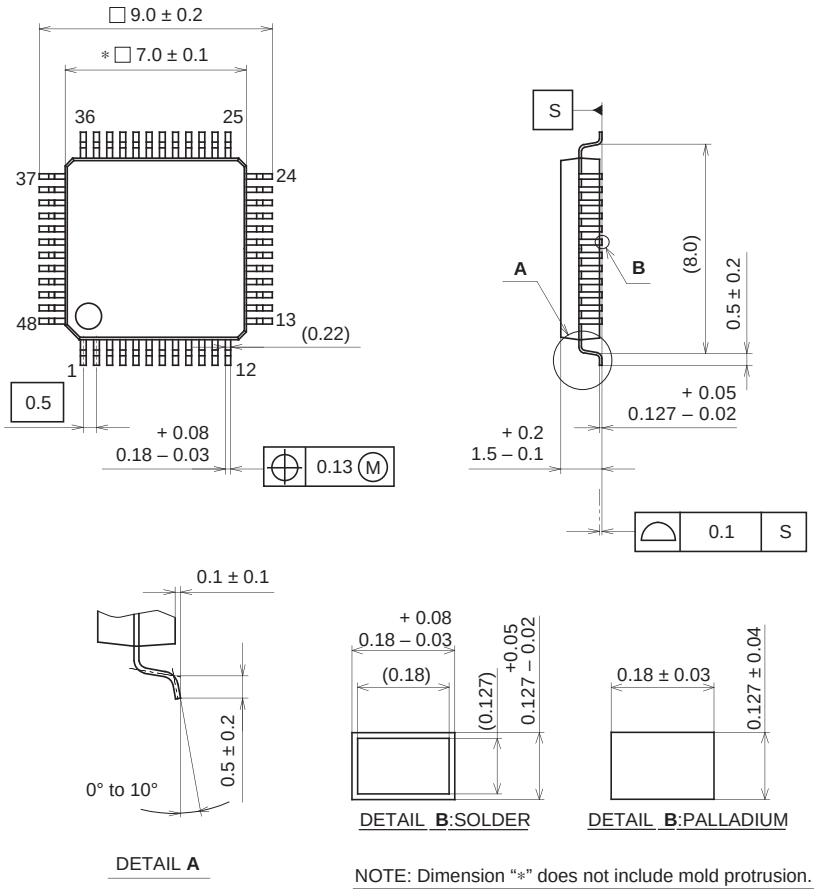


Analog input band



Package Outline Unit: mm

48PIN LQFP (PLASTIC)



DETAIL **A**

DETAIL **B**:SOLDER

DETAIL **B**:PALLADIUM

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-48P-L01
EIAJ CODE	LQFP048-P-0707
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g