FORTEC ELEKTRONIK AG

DATA DISPLAY GROUP

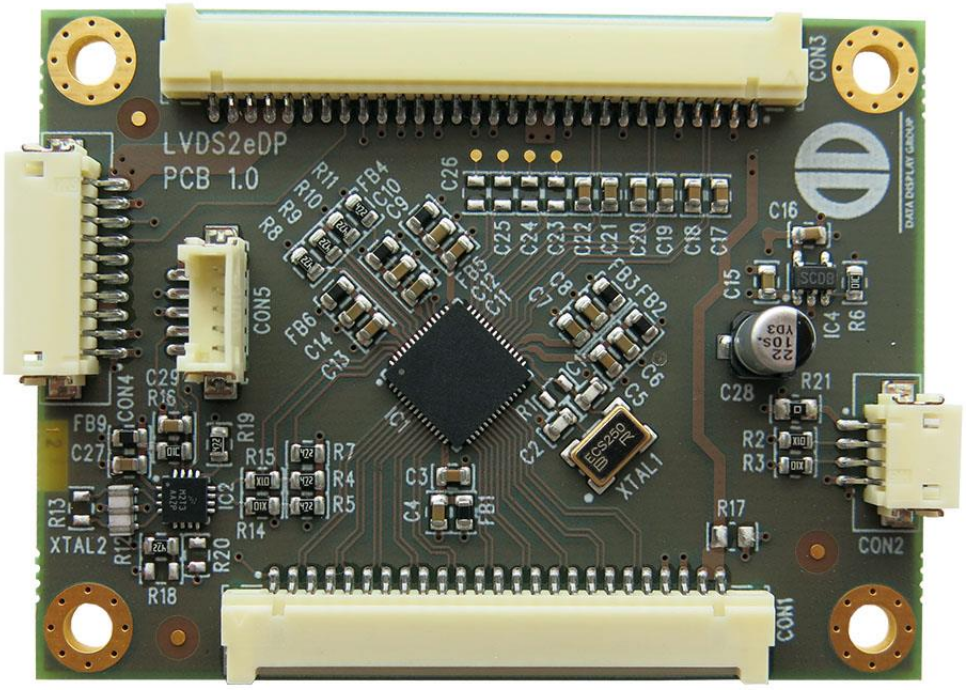
Datasheet

LVDS2eDP-01

LVDS to eDP Converter

ZU-09-032_A1, ZU-09-032

ZU-09-029_A2, ZU-09-029_A1



Version 1.13

06.07.2017

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Revision History

Date	Rev.No.	Description	Page
24.06.2014	1.0	Initial version	All
16.07.2014	1.1	Reformat and add Connectors pinning	All
25.07.2014	1.1	Added Board Picture, removed Preliminary notice	All
07.08.2014	1.1	Clarified Odd, Even Pixel	7
12.11.2014	1.2	PCB 1.1 changes are implemented Added IPC usage	All
14.11.2014	1.3	Corrected pinout description of CON1	7
26.01.2014	1.4	Removed 1 lane	5
19.11.2015	1.5	Added power consumption	9
04.12.2015	1.6	Added Cables section	4, 9, 10
19.01.2016	1.7	Corrected CON3 HPD pin	8
16.02.2016	1.8	Corrected connector type of CON4 and CON5	8, 9
15.03.2016	1.9	Document completely revised	All
14.06.2016	1.10	Company logo update Operating Temperature Range updated	All 16
12.07.2016	1.11	Add new Part Number ZU-09-032_A1 and ZU-09-029_A2 Add Ordering Information	1, 18
22.11.2016	1.12	Added panels NL192108AC18-01D and LP125WF2-SPB2 Added cable and FW information to HW options	8 4, 5
06.07.2017	1.13	Mechanical Dimensions updated News and Updates removed	17 18

1 Description

LVDS2eDP is a converter board from dual channel LVDS to 2-lane-eDP. It supports resolutions up to 1920x1200.

Overview:

- Dual channel LVDS input
- Two lanes eDP output
- Input and output resolution up to 1920x1200
- Can be connected to our standard Prisma and Artista controller boards
- Optional on-board 8-bit microcontroller to allow usage with IPCs (without Prisma)
- HDCP is not supported
- Panel voltage comes directly from the input source and is not regulated on the board
- Backlight voltage comes directly from the input source and is not regulated on the board

2 Usage with Data Display Prisma and Artista Boards

Order number:
ZU-09-029_A1 _LVDS2eDP-01 Interface Board POW_EXT (obsolete)
ZU-09-029_A2 LVDS2eDP-01 Interface Board POW_EXT

- ☞ An I2C cable to CON2 is required, see sec. 6.3 for ordering details.
- ☞ Do not load FW to the LVDS2eDP board in this configuration.

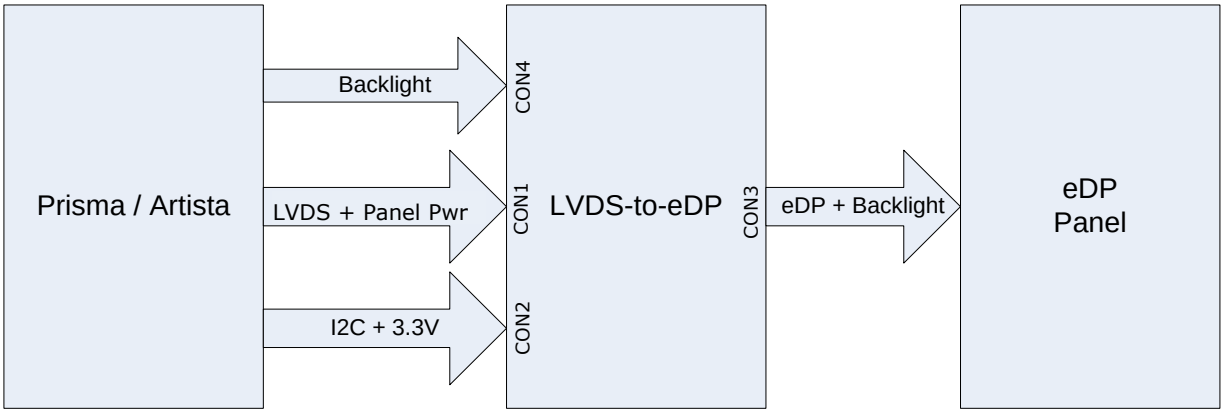


Figure 1: Usage with Prisma /Artista

Input for LVDS2eDP is the LVDS output of our Prisma boards. Additionally backlight voltage and backlight controls from Prisma are passed through to the panel to simplify cabling. No firmware is needed for the LVDS2eDP interface, instead an I2C connection from Prisma to CON2 of the LVDS2eDP interface is required. This I2C connection is used to configure the LVDS2eDP interface. In this configuration 3.3V power to the LVDS2eDP board is supplied via CON2 as well.

3 Usage with Industrial PCs

Order number:
ZU-09-032 _LVDS2eDP-02 Interface Board POW_LVDS (obsolete)
ZU-09-032_A1 LVDS2eDP-02 Interface Board POW_LVDS

- ☞ Do not connect an I2C cable to CON2 in this configuration.
- ☞ FW must be loaded to the LVDS2eDP interface.

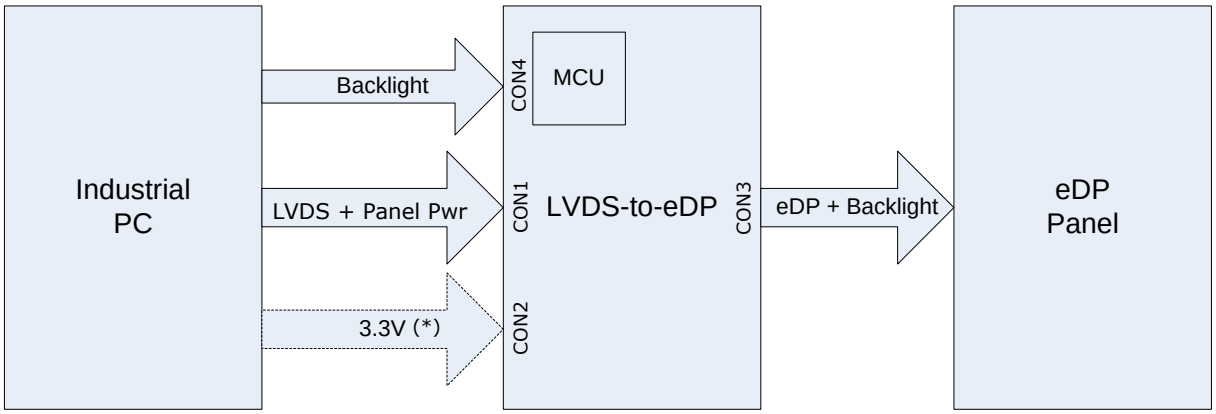


Figure 2: Usage with IPC

LVDS2eDP can also be used with Industrial PCs. In this case an on-board microcontroller unit is used to configure the LVDS to eDP translator chip and therefore a FW is needed for the LVDS2eDP interface. If the panel power is 3.3V then the LVDS2eDP interface can be supplied directly by the panel power via CON1, no additional I2C cable is required on CON2 (standard option).

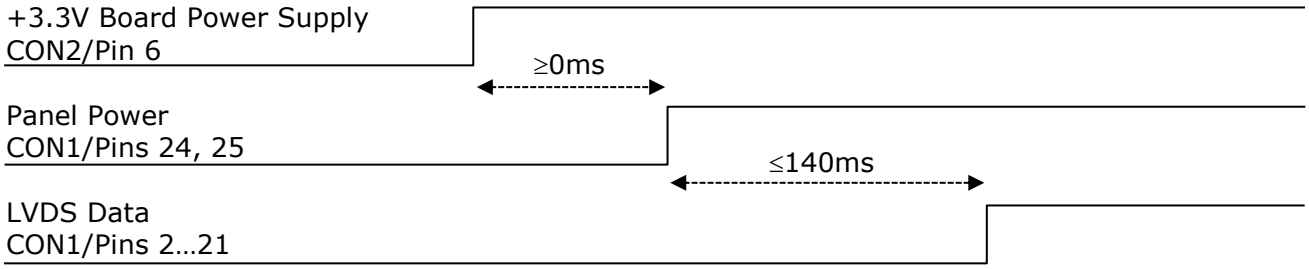
(*) In case of 5V or 12V panel power an assembly option must be used and an additional 3.3V power supply must be connected to CON2. **To avoid damage on any of your components please contact your local sales representative if your panel power is not 3.3V.**

4 Operating Conditions

To ensure a stable operation of the LVDS2eDP interface the user must ensure that the power and control signals to the inputs of the interface comply with the following requirements.

4.1 Power Sequencing

It is important to switch on the power supplies and data signals in a defined sequence. The required sequence of the LVDS2eDP interface is shown in the following diagram. Please note that additionally the sequencing specification from the panel datasheet must be met as well.



Backlight Power
CON4/Pins 3, 4, 10

Brightness Adjustment
CON4/Pin 7

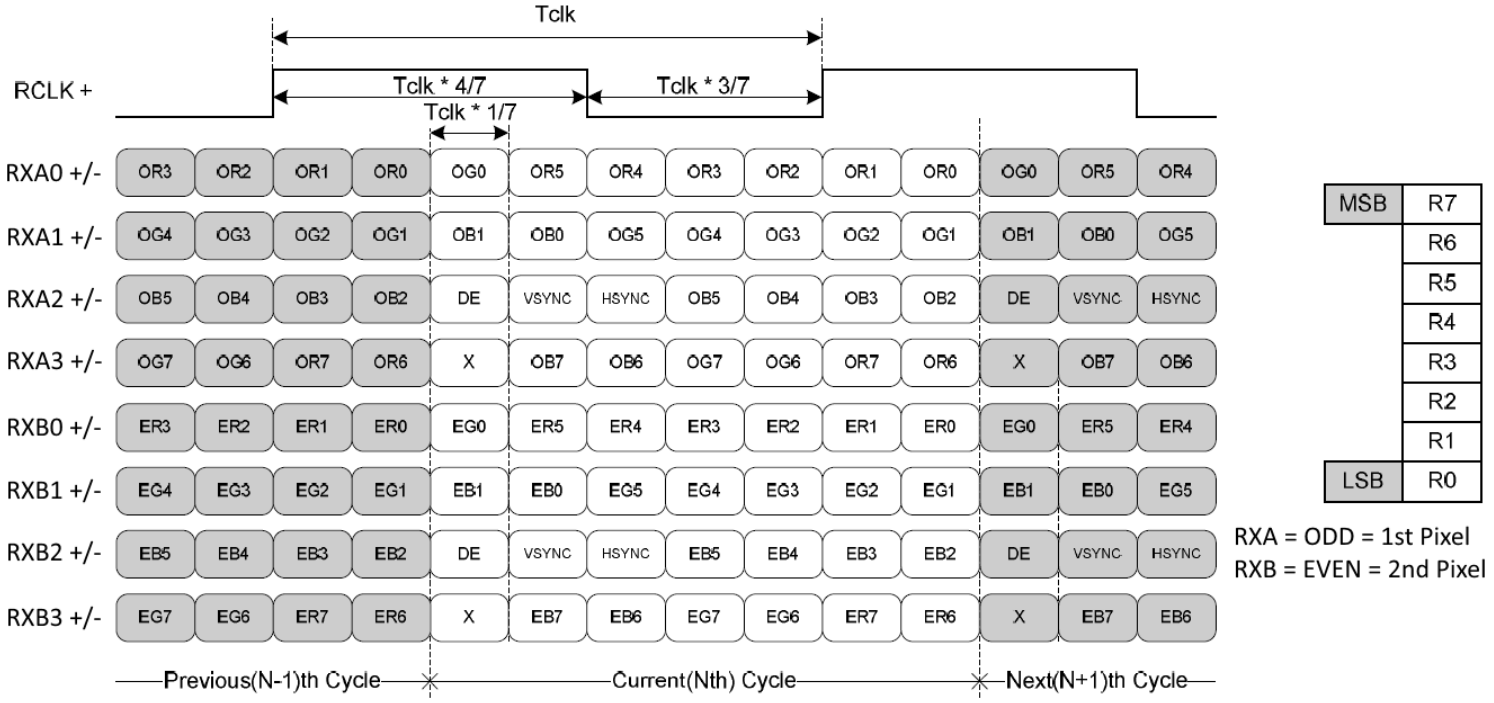
Backlight Enable
CON4/Pin 8

Sequencing must be according to the datasheet of your panel.
Ask your sales contact for the latest panel datasheet.

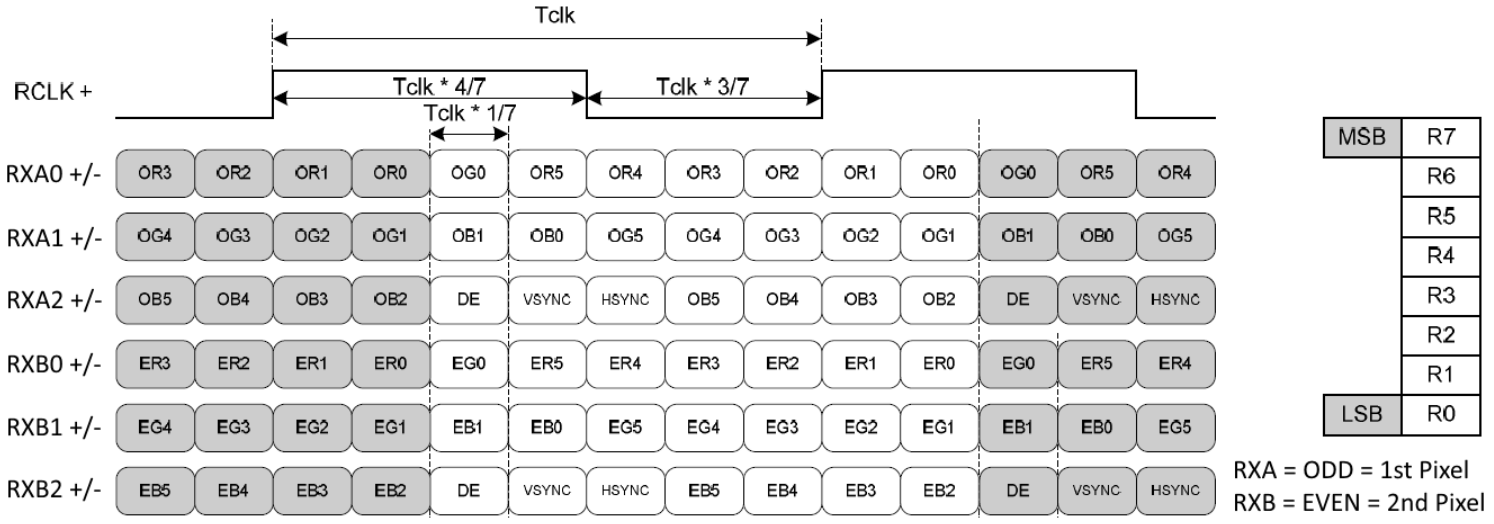
4.2 LVDS Data Mapping

The input format of the LVDS data on CON1 has to comply with the VESA standard and is shown below. If your source (IPC) outputs a different color mapping (e.g. JEIDA) then the LVDS2eDP must be configured for this mapping by FW change. In this case please contact your local sales representative.

24 Bit Input Data:



18 Bit Input Data:



4.3 LVDS Input Timing

Note: This section only affects ZU-09-032 and ZU-09-032_A1. If you use ZU-09-029_A1 or ZU-09-029_A2 together with a Prisma board then Prisma is taking care of the correct timing configuration of the LVDS2eDP via an external I2C connection.

Every LVDS2eDP interface ZU-09-032 and ZU-09-032_A1 is configured for one specific panel. The LVDS source connected to CON1 has to provide a timing mode that meets exactly the specification of the table below. Image distortion will occur if the timing or sync polarity differs from this table.
Contact your sales representative if your desired panel is not listed here.

Panel		Horizontal Timing					Vertical Timing				
Mfg	Type	Active Pixels	Total Pixels	Back Porch	Sync Width	Sync Polarity	Active Lines	Total Lines	Back Porch	Sync Width	Sync Polarity
LG	LP156WF4-SPU1	1920	2080	80	32	Act.-High	1080	1111	23	5	Act.-High
LG	LP156WF4-SPH1	1920	2080	80	32	Act.-High	1080	1111	23	5	Act.-High
LG	LP156WF6-SPB1	1920	2080	80	32	Act.-High	1080	1111	23	5	Act.-High
LG	LP125WF2-SPB1	1920	2106	106	32	Act.-High	1080	1095	7	5	Act.-High
LG	LP125WF2-SPB2	1920	2106	106	32	Act.-High	1080	1095	7	5	Act.-High
AUO	B140HAN01.1	1920	2104	48	32	Act.-High	1080	1116	13	5	Act.-High
AUO	G156HAN01.0	1920	2104	48	32	Act.-High	1080	1116	13	5	Act.-High
AUO	G156HTN01.0	1920	2100	48	32	Act.-High	1080	1130	13	5	Act.-High
NLT	NL192108AC18-01D	1920	2080	80	32	Act.-High	1080	1112	23	5	Act.-High

5 Connectors

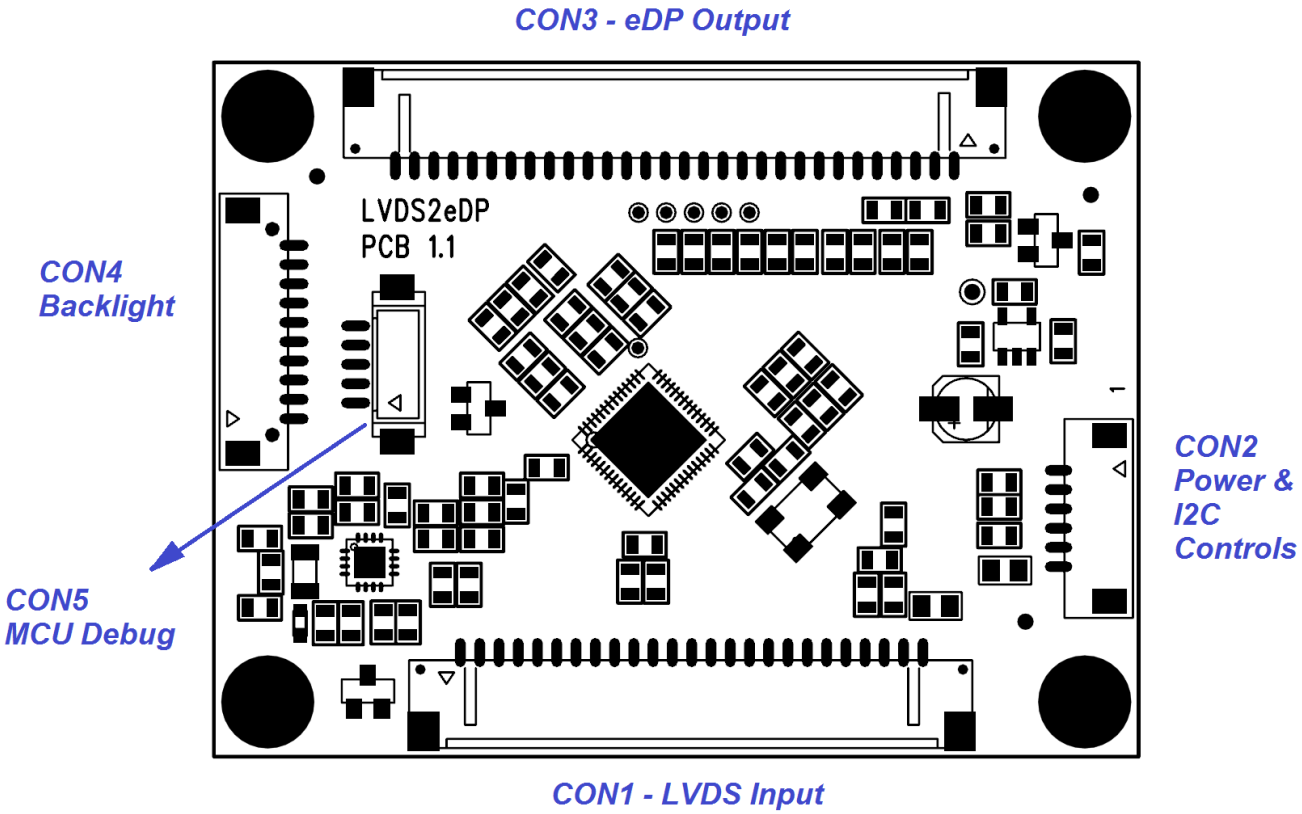


Figure 3: Connectors overview

Connector	Usage	Manufacturer Part Number Hirose
CON1	LVDS & Panel Power Input	DF14-25P-1.25H
CON2	I2C & Board Power Supply Input	DF13-6P-1.25H
CON3	eDP Output	DF14-30P-1.25H
CON4	Backlight Power & Control Input	DF13-10P-1.25H
CON5	MCU Debug	DF13-5P-1.25V

5.1 Pinouts

5.1.1 CON1 – LVDS & Panel Power Input

Manufacturer : Hirose
Type : DF14-25P-1.25H

Pin	Signal	Description
1	BKLT_EN	Backlight Enable
2	RXB0-	LVDS Input Even Pixel Pair0 -
3	RXB0+	LVDS Input Even Pixel Pair0 +
4	RXB1-	LVDS Input Even Pixel Pair1 -
5	RXB1+	LVDS Input Even Pixel Pair1 +
6	RXB2-	LVDS Input Even Pixel Pair2 -
7	RXB2+	LVDS Input Even Pixel Pair2 +
8	RXBCLK-	LVDS Input Even Pixel Clock -
9	RXBCLK+	LVDS Input Even Pixel Clock +
10	RXB3-	LVDS Input Even Pixel Pair3 -
11	RXB3+	LVDS Input Even Pixel Pair3 +
12	RXA0-	LVDS Input Odd Pixel Pair0 -
13	RXA0+	LVDS Input Odd Pixel Pair0 +
14	RXA1-	LVDS Input Odd Pixel Pair1 -
15	RXA1+	LVDS Input Odd Pixel Pair1 +
16	RXA2-	LVDS Input Odd Pixel Pair2 -
17	RXA2+	LVDS Input Odd Pixel Pair2 +
18	RXACLK-	LVDS Input Odd Pixel Clock -
19	RXACLK+	LVDS Input Odd Pixel Clock +
20	RXA3-	LVDS Input Odd Pixel Pair3 -
21	RXA3+	LVDS Input Odd Pixel Pair3 +
22	GND	Ground
23	GND	Ground
24	SVCC	Panel Power (Note 2)
25	SVCC	Panel Power (Note 2)

Notes:
1) Odd pixel is the first pixel.
2) If you use ZU-09-032 only 3.3V panel power is allowed. See sec. 3 for more details.

5.1.2 CON2 – I2C

Manufacturer : Hirose
Type : DF13-6P-1.25H

Pin	Signal	Description
1	GND	Ground
2	SDA	I^2C data
3	SCL	I^2C clock
4	RST	Optional Reset
5	HPD#	Inverted Hot Plug Detect
6	+3.3V Vin	+3.3V Board Power Supply

5.1.3 CON3 – eDP Output

Manufacturer : Hirose
Type : DF14-30P-1.25H

Pin	Signal	Description
1	--	Not connected
2	GND	Ground
3	DPAUX+	eDP Aux Channel +
4	DPAUX-	eDP Aux Channel -
5	GND	Ground
6	DP0-	eDP Channel 0 -
7	DP0+	eDP Channel 0 +
8	GND	Ground
9	DP1-	eDP Channel 1 -
10	DP1+	eDP Channel 1 +
11	GND	Ground
12	SVCC	Panel Power Output (Note 1) Max. 1A (Note 3)
13	SVCC	
14	--	Not connected
15	GND	Ground
16	GND	Ground
17	HPD	Hot Plug Detect
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	BKLT_EN	Backlight Enable – Output (Note 2)
23	BRT_ADJ	Backlight Dimming - PWM Output (Note 2)
24	--	Not connected
25	--	Not connected
26	+12V_BKLT	+12V Backlight Power Output (Note 2) Max. 2A (Note 3)
27	+12V_BKLT	
28	+12V_BKLT	
29	+12V_BKLT	
30	--	Not connected

Notes:
1) Directly connected to SVCC of CON1
2) All backlight signals are directly connected to CON4
3) This is the max. allowed current of the LVDS2eDP interface. The max. allowed current of the connected input source (IPC) must be considered as well. The LVDS2eDP interface does not provide any current limitation circuitry or fuses.

5.1.4 CON4 – Backlight Input

Manufacturer : Hirose
Type : DF13-10P-1.25H

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	+12V_BKLT	+12V Backlight Supply Input
4	+12V_BKLT	+12V Backlight Supply Input
5	--	Not connected
6	--	Not connected
7	BRT_ADJ	Backlight Dimming – PWM Input
8	BKLT_EN	Backlight Enable – Input
9	GND	Ground
10	+12V_BKLT	+12V Backlight Supply Input

5.1.5 CON5 – MCU Debug

This connector is for engineering and production purposes.

Manufacturer : Hirose
Type : DF13-5P-1.25V

Pin	Signal	Description
1	RESET	Programming Reset
2	SWD_DIO	Programming Data
3	PROG_3.3V	Programming Voltage
4	SWD_CLK	Programming Clock
5	GND	Ground

6 Cables

6.1 LVDS Cable

Driving Board	Connector	Part Type	Cable order code
ArtistaMedia-II	CON4	DF14-25P-1.25H	KA-30-520
ArtistaNET-III	CON7		
Prisma-IIIa	CON4		
PrismaMediaECO	CN10		
PrismaCompactMedia	CON10	DF14-30P-1.25H	Please ask your sales representative

6.2 Backlight Cable

Driving Board	Connector	Part Type	Cable order code
ArtistaMedia-II	CON23	DF13-10P-1.25H	KA-30-521
ArtistaNET-III	CON14		
Prisma-IIIa	CON23		
PrismaMediaECO	CN13		
PrismaCompactMedia	CON13		

6.3 I2C Cable

I2C connections to Artista/Prisma boards are listed in below table. These cables are needed for ZU-09-029_A1 and ZU-09-029_A2 to provide power and the I2C connection. Do not connect these cables to ZU-09-032 and ZU-09-032_A1.

Driving Board	Connector	Part Type	Cable order code
ArtistaMedia-II	CON22	DF13-5P	Please ask your sales representative
ArtistaNET-III	CON1	DF13-5P	
Prisma-IIIa	CON15	DF13-12P	KA-30-543
PrismaMediaECO	CN9	DF13-6P	KA-30-542
PrismaCompactMedia	CN5	501568-0407 (Molex)	Please ask your sales representative

6.4 eDP Cable

LVDS2eDP can be connected to eDP panels using KA-30-541 which has a 30 pin IPEX connector:

WIRING CHART							
INTERFACE LVDS2eDP-01 [A]					DISPLAY LP156WF6-SPB1 [B]		
ITEM [A]					ITEM [B]		
Pin	Signal	Description	Size	Pair	Pin	Signal	Description
A1	NC						
A2	GND		AWG32		B29	GND	High Speed Ground
A3	DPAUX_P		AWG32	Pair 1	B22	AUX-CH-P	True Signal Auxiliary Channel
A4	DPAUX_N		AWG32	Pair 1	B21	AUX-CH-N	Complement Signal Auxiliary Channel
A5	GND		AWG32		B26	GND	High Speed Ground
A6	DP0_N		AWG32	Pair 2	B25	Lane0-N	Complement Signal Link Lane 0
A7	DP0_P		AWG32	Pair 2	B24	Lane0-P	True Signal Link Lane 0
A8	GND		AWG32		B23	GND	High Speed Ground
A9	DP1_N		AWG32	Pair 3	B28	Lane1-N	Complement Signal Link Lane 1
A10	DP1_P		AWG32	Pair 3	B27	Lane1-P	True Signal Link Lane 1
A11	GND		AWG32		B20	GND	High Speed Ground
A12	SVCC		AWG32		B19	VCC	LCD logic and driver power
A13	SVCC		AWG32		B18	VCC	LCD logic and driver power
A14	NC						
A15	GND		AWG32		B16	GND	LCD logic and driver ground
A16	GND		AWG32		B15	GND	LCD logic and driver ground
A17	HPD		AWG32		B14	HPD	HPD signal pin
A18	GND		AWG32		B13	BL-GND	LED Backlight ground
A19	GND		AWG32		B12	BL-GND	LED Backlight ground
A20	GND		AWG32		B11	BL-GND	LED Backlight ground
A21	GND		AWG32		B10	BL-GND	LED Backlight ground
A22	BKLT_EN		AWG32		B9	BL ENABLE	LED Backlight control on/off control
A23	BRT_ADJ		AWG32		B8	BL PWM	System PWM signal input for dimming
A24	NC						
A25	NC						
A26	+12V_BKLT		AWG32		B5	VLED	LED Backlight power (12V Typical)
A27	+12V_BKLT		AWG32		B4	VLED	LED Backlight power (12V Typical)
A28	+12V_BKLT		AWG32		B3	VLED	LED Backlight power (12V Typical)
A29	+12V_BKLT		AWG32		B2	VLED	LED Backlight power (12V Typical)
A30	NC						

ITEM [A]: HIROSE / DF14-30S-1.25C ITEM [B]: IPEX / 20453-030T-01

Cable length: 100mm

7 Electrical Requirements

7.1 Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Board Power Supply ZU-09-029_A2	V_{IN}	3	3.3	3.46	V	CON2, Pin6
Board Power Supply ZU-09-032_A1	V_{IN}	3	3.3	3.46	V	CON1, Pin24+25 See note 1 below
Supply Current (board only, without panel)	I_{IN}		58	70	mA	

Notes:
1) This is the voltage range of the LVDS2eDP interface. The voltage range of the connected eDP panel must be considered as well. The input voltage on CON1 is directly connected to the panel, the LVDS2eDP interface does not provide any voltage regulation circuitry.

7.2 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Note
Board Power Supply	V_{IN}	-0.2	3.46	V	
Panel Voltage Input ZU-09-029_A2	V_{PNL}	-0.2	13	V	CON1, Pin24+25 See note 1 below
Panel Voltage Input ZU-09-032_A1	V_{PNL}	-0.2	3.46	V	CON1, Pin24+25 See note 1 below
Panel Current	I_{PNL}		1	A	See note 2 below
Backlight Voltage Input	V_{BKL}	-0.2	25	V	CON4, Pin 3+4+10 See note 1 below
Backlight Current	I_{BKL}		2	A	See note 2 below

Notes:
1) This is the max. allowed voltage of the LVDS2eDP interface. The max. allowed voltage of the connected eDP panel must be considered as well. The input voltage on CON1 is directly connected to the panel, the LVDS2eDP interface does not provide any voltage regulation circuitry.
2) This is the max. allowed current of the LVDS2eDP interface. The max. allowed current of the connected input source (IPC) must be considered as well. The LVDS2eDP interface does not provide any current limitation circuitry or fuses.

7.3 LVDS Input Electrical Specification

Item	Symbol	Min	Typ	Max	Unit
LVDS data rate per pair	$Rate_{LVDS}$	400		1000	Mbps
LVDS input clock frequency	$f_{CLK-LVDS}$	57		143	MHz
Differential input high threshold	$V_{TH-LVDS}$			0.1	V
Differential input low threshold	$V_{TL-LVDS}$	-0.1			V
LVDS common mode voltage	$V_{CM-LVDS}$	0.9		1.4	V

8 Thermal Requirements

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	T_{op}	-20	80	^{0}C	See note 1 below
Storage Temperature	T_{st}	-35	85	^{0}C	See note 1 below

Notes:
1) Permanent damage to the device may occur if maximum values are exceeded.

9 Mechanical Dimensions

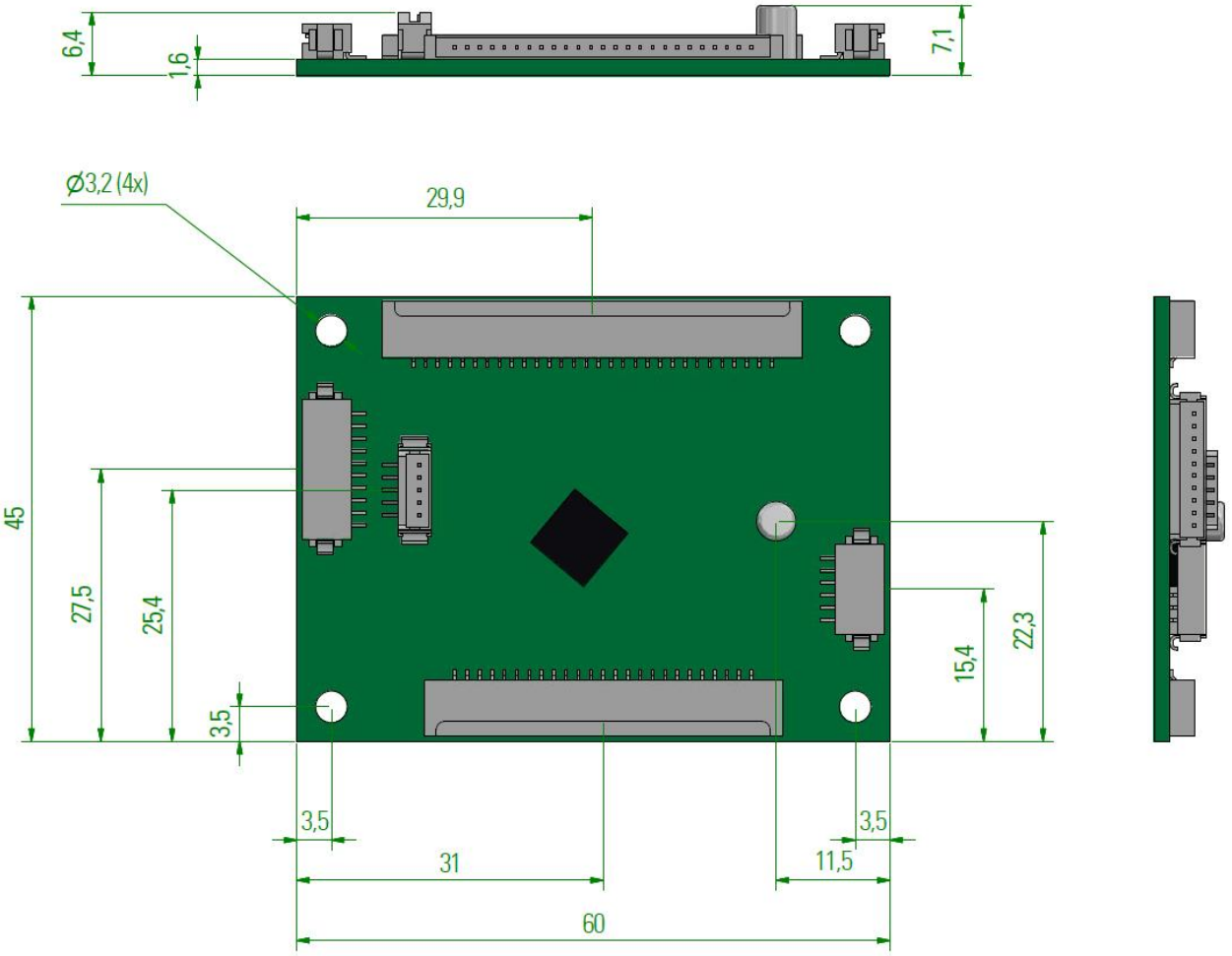


Figure 4: Dimensions

10 Ordering Information

Part Number	Status	Operating Temperature Range
ZU-09-029_A1	Obsolete	-20..+70°C
ZU-09-032	Obsolete	-20..+70°C
ZU-09-032_A1	Active	-20..+80°C
ZU-09-029_A2	Active	-20..+80°C

Our company network supports you worldwide with offices in Germany, Great Britain, Turkey and the USA. For more information please contact:

DATA DISPLAY GROUP

A FORTEC GROUP MEMBER

Distec GmbH
Augsburger Str. 2b
82110 Germering
Germany

Phone: +49 (0)89 / 89 43 63-0
Fax: +49 (0)89 / 89 43 63-131
E-Mail: info@datadisplay-group.de
Internet: www.datadisplay-group.de

FORTEC Elektronik AG
Lechwiesenstr. 9
86899 Landsberg am Lech
Germany

Phone: +49 (0)8191 / 911 72-0
Fax: +49 (0)8191 / 217 70
E-Mail: sales@fortecag.de
Internet: www.fortecag.de

Display Technology Ltd.
5 The Oaks Business Village
Revenge Road, Lordswood
Chatham, Kent, ME5 8LF
United Kingdom
Phone: +44 (0)1634 / 67 27 55
Fax: +44 (0)1634 / 67 27 54
E-Mail: info@displaytechnology.co.uk
Internet: www.datadisplay-group.com

Apollo Display Technologies, Corp.
87 Raynor Avenue,
Unit 1Ronkonkoma,
NY 11779
United States of America
Phone: +1 631 / 580-43 60
Fax: +1 631 / 580-43 70
E-Mail: info@apollodisplays.com
Internet: www.apollodisplays.com

Sales Partner:

DATA DISPLAY BİLİŞİM TEKNOLOJİLERİ İÇ VE DIŞ TİCARET LİMİTED ŞİRKETİ
Barbaros Mh. Ak Zambak Sk. A Blok D:143
34376 Ataşehir / Istanbul
Turkey
Phone: +90 (0)216 / 688 04 68
Fax: +90 (0)216 / 688 04 69
E-Mail: info@data-display.com.tr
Internet: www.data-display.com.tr