FAIRCHILD SEMICONDUCTOR®

July 2005

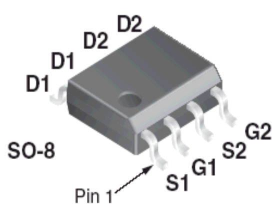
FDS8978
Dual N-Channel PowerTrench® MOSFET
30V, 7.5A, 18mΩ

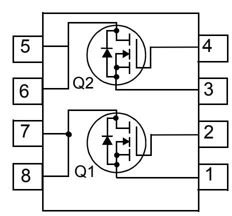
Features

- $r_{DS(ON)}$ = 18mΩ, V_{GS} = 10V, I_D = 7.5A
- $r_{DS(ON)}$ = 21mΩ, V_{GS} = 4.5V, I_D = 6.9A
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- 100% Rg Tested
- RoHS Compliant

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current Continuous (T_A = 25°C, V_{GS} = 10V, $R_{\theta JA}$ = 78°C/W)	7.5	A
	Continuous (T_A = 25°C, V_{GS} = 4.5V, $R_{\theta JA}$ = 78°C/W)	6.9	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	57	mJ
P_D	Power dissipation	1.6	W
	Derate above 25°C	13	mW/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Ambient (Note 2)	78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 3)	170	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 4)	183	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8978	FDS8978	SO-8	330mm	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 24V, V_{GS} = 0V, T_A = 150°C	-	-	250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250μA	1.2	-	2.5	V
$r_{DS(ON)}$	Drain to Source On Resistance	I_D = 7.5A, V_{GS} = 10V	-	0.014	0.018	Ω
		I_D = 6.9A, V_{GS} = 4.5V	-	0.017	0.021	Ω
		I_D = 7.5A, V_{GS} = 10V, T_A = 150°C	-	0.022	0.029	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	907	-	pF
C_{OSS}	Output Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	191	-	pF
C_{RSS}	Reverse Transfer Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz	-	112	-	pF
R_G	Gate Resistance	f = 1MHz		1.2	4.0	Ω
Q_g	Total Gate Charge	V_{GS} =10V; V_{DD} = 15V, I_D = 7.5A	-	17	26	nC
		V_{GS} = 5V; V_{DD} = 15V, I_D = 7.5A		9	14	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 15V, I_D = 7.5A	-	2.3	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	V_{DD} = 15V, I_D = 7.5A	-	1.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15V, I_D = 7.5A	-	3.3	-	nC
Switching Characteristics (V_{GS} = 10V)						
t_{ON}	Turn-On Time	V_{DD} = 15V, I_D = 7.5A, V_{GS} = 10V, R_{GS} = 16Ω	-	44	66	ns
$t_{d(ON)}$	Turn-On Delay Time		-	7	10.5	ns
t_r	Rise Time		-	37	55.5	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	48	72	ns
t_f	Fall Time		-	24	36	ns
t_{OFF}	Turn-Off Time		-	72	108	ns
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Voltage	I_{SD} = 7.5A	-	-	1.25	V
		I_{SD} = 2.1A	-	-	1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = 7.5A, dI_{SD}/dt=100A/μs	-	19	25	ns
Q_{RR}	Reverse Recovered Charge	I_{SD} = 7.5A, dI_{SD}/dt=100A/μs	-	10	13	nC

Notes:
1: Starting T_J = 25°C, L = 1mH, I_{AS} = 7.5A, V_{DD} = 30V, V_{GS} = 10V.
2: $R_{\theta JA}$ is 78°C/W when mounted on a 0.5 in^2 copper pad on FR-4 at 100 seconds.
3: $R_{\theta JA}$ is 191°C/W when mounted on a 0.027 in^2 copper pad on FR-4 at 1000 seconds.
4: $R_{\theta JA}$ is 228°C/W when mounted on a 0.006 in^2 copper pad on FR-4 at 1000 seconds.

Typical Characteristics T_A = 25°C unless otherwise noted

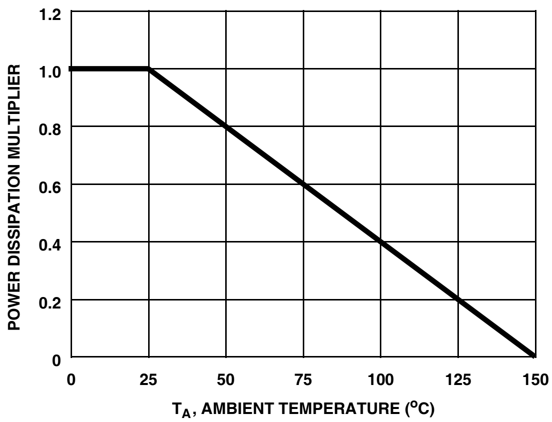


Figure 1. Normalized Power Dissipation vs Ambient Temperature

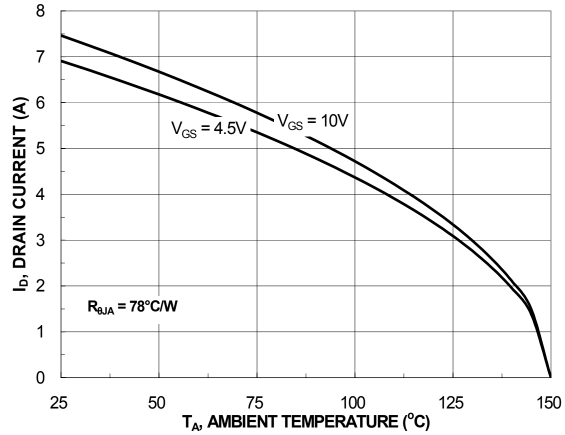


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

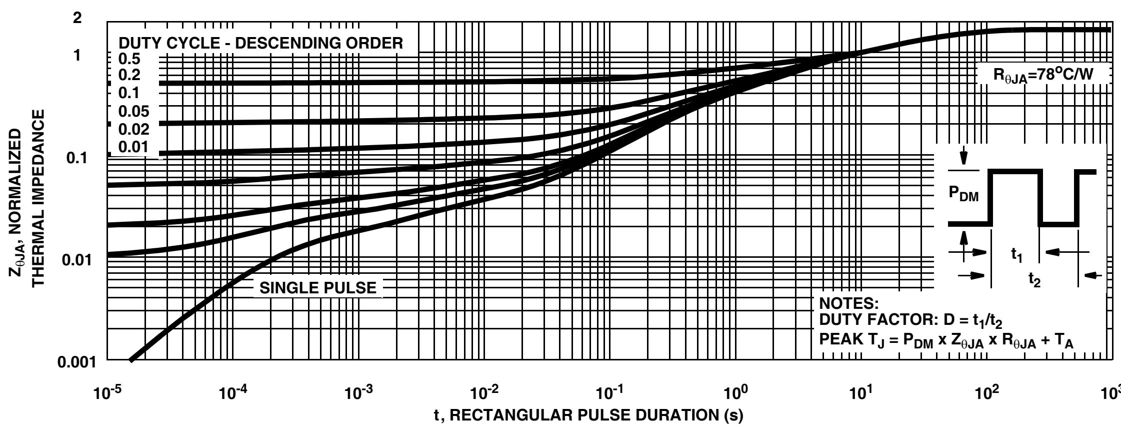


Figure 3. Normalized Maximum Transient Thermal Impedance

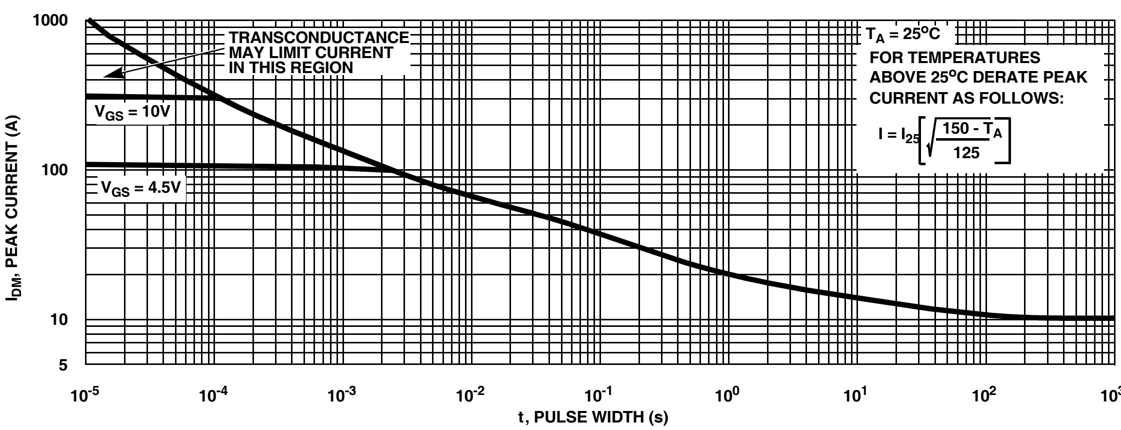
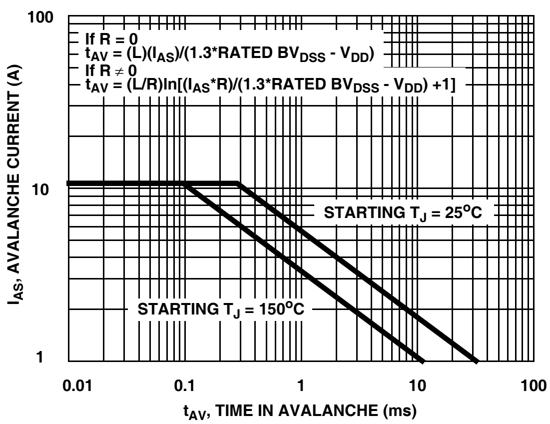


Figure 4. Peak Current Capability

Typical Characteristics T_A = 25°C unless otherwise noted



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 5. Unclamped Inductive Switching Capability

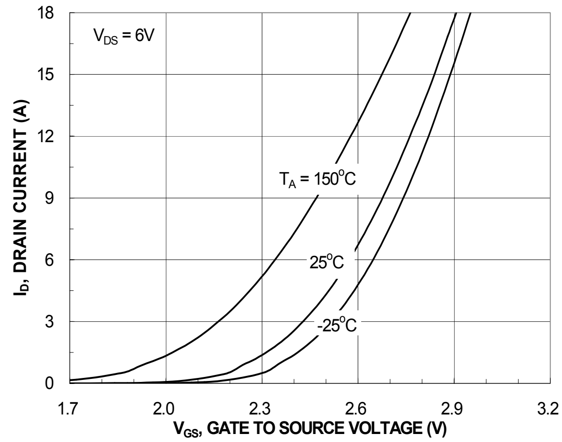


Figure 6. Transfer Characteristics

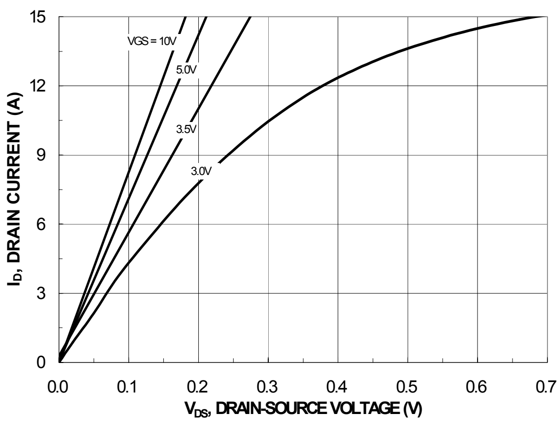


Figure 7. Saturation Characteristics

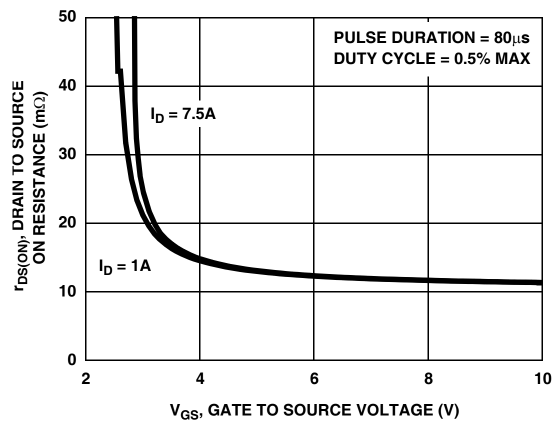


Figure 8. Drain to Source On Resistance vs Drain Current

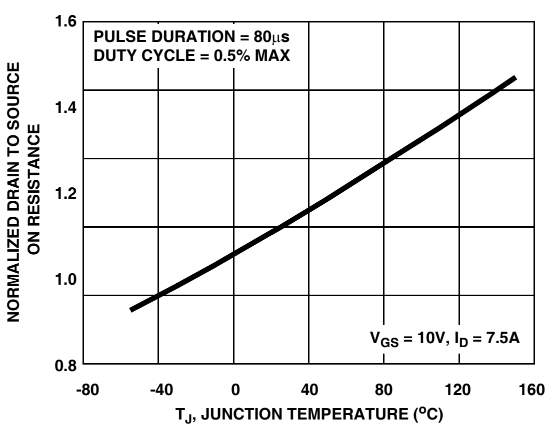


Figure 9. Normalized Drain to Source On Resistance vs Junction Temperature

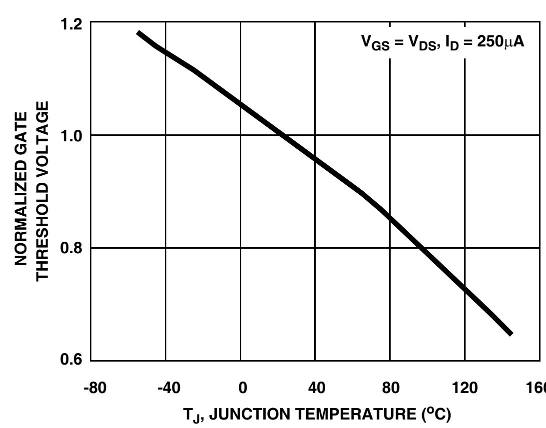


Figure 10. Normalized Gate Threshold Voltage vs Junction Temperature

Typical Characteristics $T_A = 25°C$ unless otherwise noted

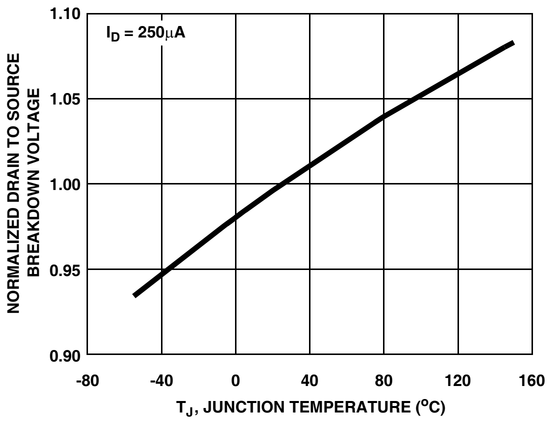


Figure 11. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

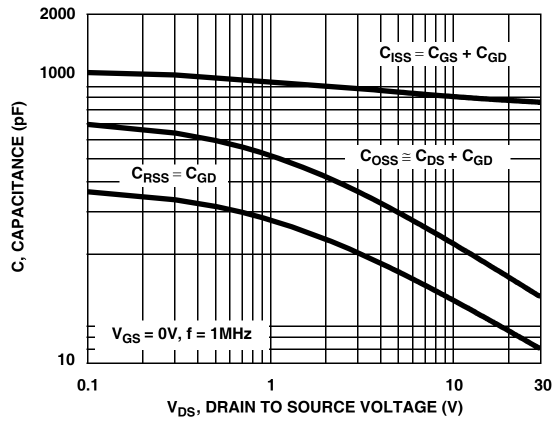


Figure 12. Capacitance vs Drain to Source Voltage

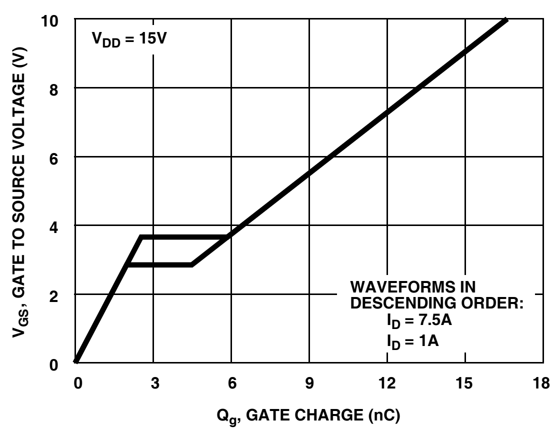


Figure 13. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

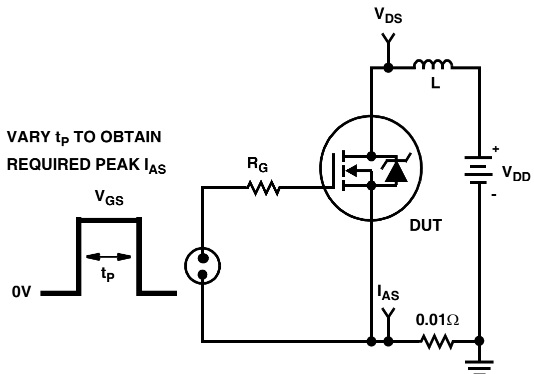


Figure 14. Unclamped Energy Test Circuit

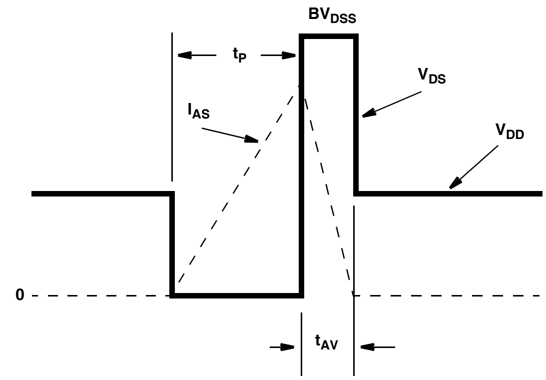


Figure 15. Unclamped Energy Waveforms

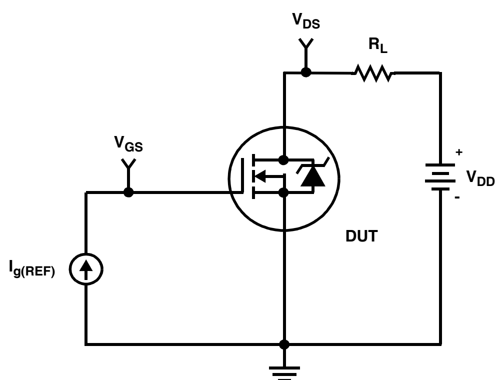


Figure 16. Gate Charge Test Circuit

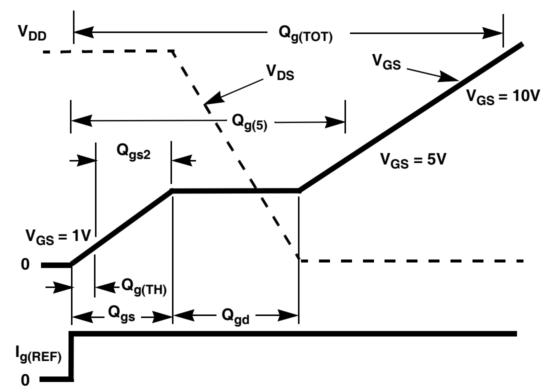


Figure 17. Gate Charge Waveforms

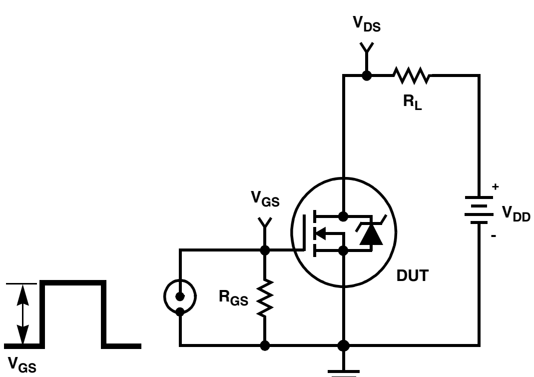


Figure 18. Switching Time Test Circuit

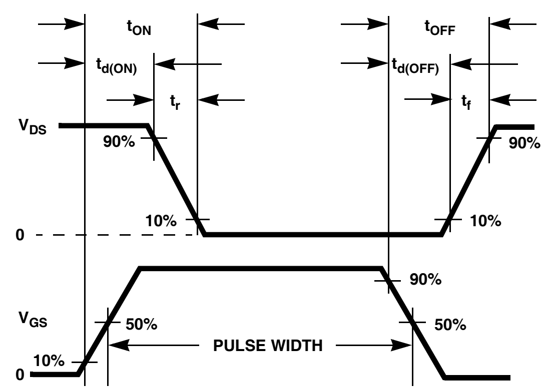


Figure 19. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SO8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 64 + \frac{26}{0.23 + Area} \qquad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 22 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

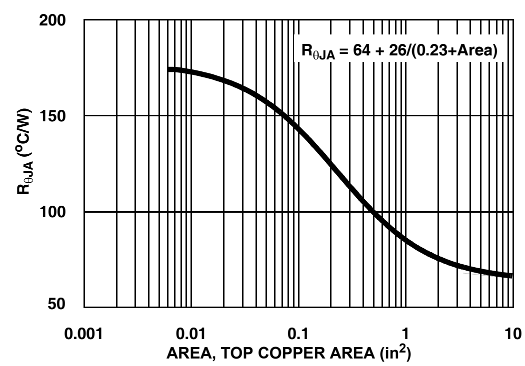


Figure 21. Thermal Resistance vs Mounting Pad Area

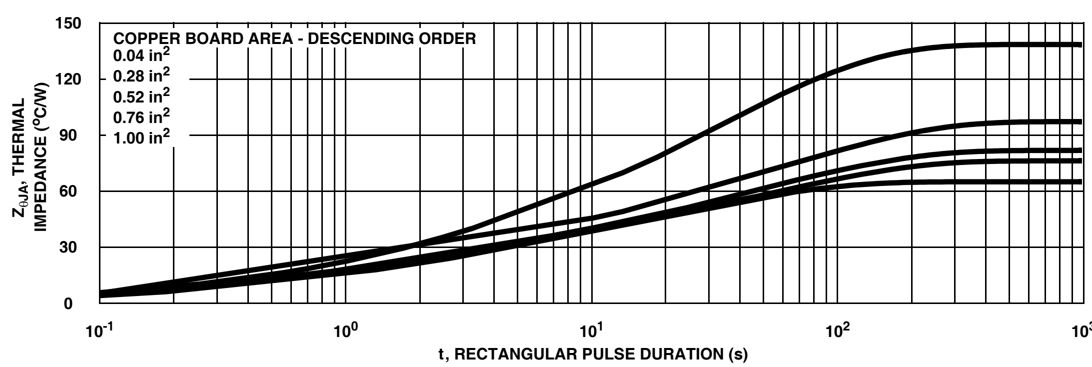
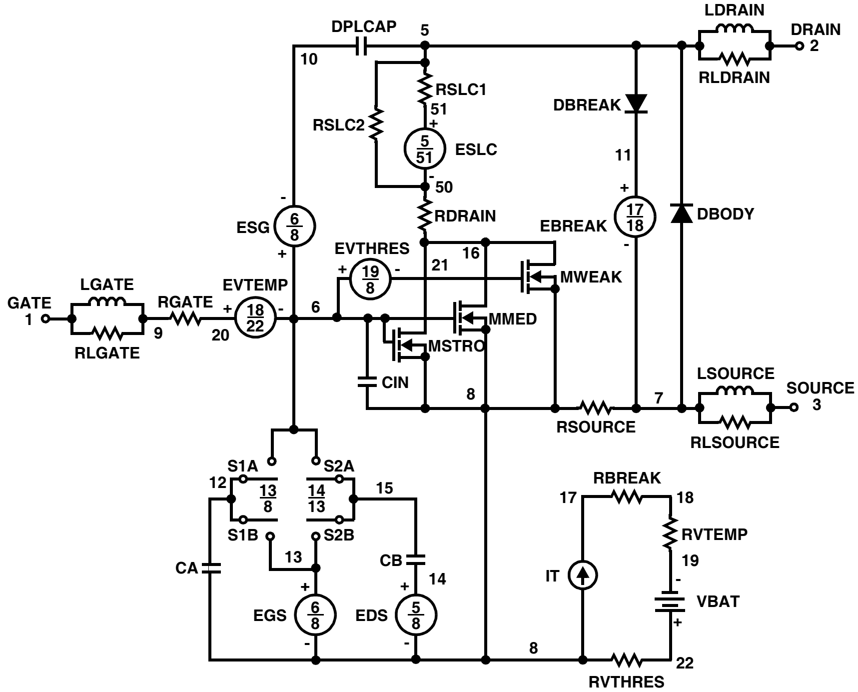


Figure 22. Thermal Impedance vs Mounting Pad Area

PSPICE Electrical Model

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.SUBCKT FDS8878  2 1 3
*February 2005

Ca 12 8 7.8e-10
Cb 15 14 7.8e-10
Cin 6 8 .78e-9
Dbody 7 5 DbodyMOD
Dbreak 5 11 DbreakMOD
Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 32.9
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 5.29e-9
Ldrain 2 5 1.0e-9
Lsource 3 7 0.18e-9

RLgate 1 9 52.9
RLdrain 2 5 10
RLsource 3 7 1.8

Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 1.6e-3
Rgate 9 20 2.3
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
Rsource 8 7 RsourceMOD 8.9e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*170),5))}

.MODEL DbodyMOD D (IS=2.0E-12 IKF=10 N=1.01 RS=7.0e-3 TRS1=8e-4 TRS2=2e-7
+ CJO=3.5e-10 M=0.55 TT=7e-11 XTI=2)
.MODEL DbreakMOD D (RS=0.2 TRS1=1e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=3.8e-10 IS=1e-30 N=10 M=0.45)

.MODEL MstroMOD NMOS (VTO=2.36 KP=150 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MmedMOD NMOS (VTO=1.95 KP=5.0 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=2.3)
.MODEL MweakMOD NMOS (VTO=1.57 KP=0.02 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=23  RS=0.1)

.MODEL RbreakMOD RES (TC1=8.3e-4 TC2=-8e-7)
.MODEL RdrainMOD RES (TC1=15e-3 TC2=0.1e-5)
.MODEL RSLCMOD RES (TC1=1e-4 TC2=1e-6)
.MODEL RsourceMOD RES (TC1=1e-3 TC2=3e-6)
.MODEL RvtempMOD RES (TC1=-1.8e-3 TC2=2e-7)
.MODEL RvthresMOD RES (TC1=-2.0e-3 TC2=-6e-6)
 MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-3.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.5 VOFF=-4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-1.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.0 VOFF=-1.5).ENDS
```

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

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SuperSOT™-6
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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