# TLV906x 10-MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems

## 1 Features

- Rail-to-Rail Input and Output
- Low Input Offset Voltage: ±0.3 mV
- Unity-Gain Bandwidth: 10 MHz
- Low Broadband Noise: 10 nV/$\sqrt{\text{Hz}}$
- Low Input Bias Current: 0.5 pA
- Low Quiescent Current: 538 µA
- Unity-Gain Stable
- Internal RFI and EMI Filter
- Operational at Supply Voltages as Low as 1.8 V
- Easier to Stabilize with Higher Capacitative Load Due to Resistive Open-Loop Output Impedance
- Extended Temperature Range: –40°C to +125°C

## 2 Applications

- E-Bikes
- Smoke Detectors
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Refrigerators
- Wearable Devices
- Laptop Computers
- Washing Machines
- Sensor Signal Conditioning
- Power Modules
- Barcode Scanners
- Active Filters
- Low-Side Current Sensing

## 3 Description

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) are single-, dual-, and quad- low-voltage (1.8 V to 5.5 V) operational amplifiers (op amps) with rail-to-rail input- and output-swing capabilities. These devices are highly cost-effective solutions for applications where low-voltage operation, a small footprint, and high capacitative load drive are needed. Although the capacitative load drive of the TLV906x is 100 pF, the resistive open-loop output impedance makes it easy to stabilize with much higher capacitive loads. These op amps are designed specifically for low-voltage operation (1.8 V to 5.5 V) with performance specifications similar to the OPAx316 and TLVx316 devices.

The TLV906x family helps simplify system design, because it is unity-gain stable, integrates the RFI and EMI rejection filter and provides no phase reversal in overdrive condition.

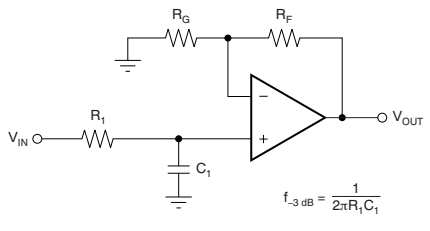
Micro-size packages, such as SOT553 and WSON, are offered for all the channel variants (single, dual and quad), along with industry-standard packages, such as SOIC, MSOP, SOT-23 and TSSOP.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV9061 | SOT-23 (5) | 1.60 mm × 2.90 mm |
| | SC70 (5) | 1.25 mm × 2.00 mm |
| | SOT553 (5) | 1.65 mm x 1.20 mm |
| | SOIC (8) | 3.91 mm × 4.90 mm |
| TLV9062 | SOIC (8) | 3.91 mm × 4.90 mm |
| | WSON (8) | 2.00 mm x 2.00 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| | VSSOP (10) | 3.00 mm × 3.00 mm |
| TLV9064 | SOIC(14) | 8.65 mm × 3.91 mm |
| | TSSOP (14) | 4.40 mm × 5.00 mm |

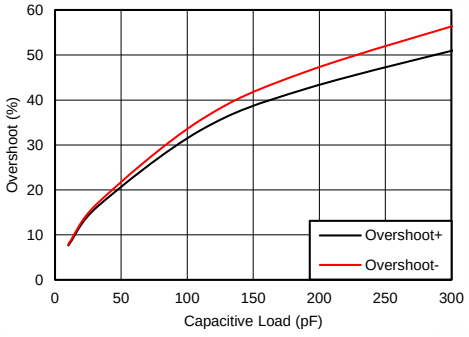
(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Single-Pole, Low-Pass Filter**




$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

**Small-Signal Overshoot vs Load Capacitance**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

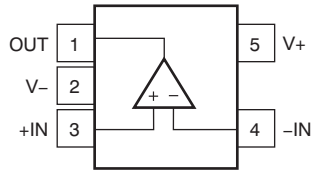
| Changes from Original (March 2017) to Revision A | Page |
|---|---|
| • Changed device status from Advance Information to Production Data | 1 |

# 5 Device Comparison Table

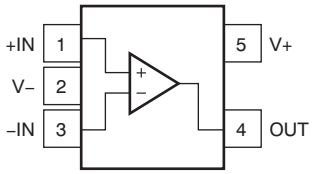
| DEVICE | NO. OF CHANNELS | PACKAGE-LEADS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | DBV | DCK | DRL | D | DSG | DGK | PW | RTE |
| TLV9061 | 1 | 5 | 5 | 5 | 8 | — | — | — | — |
| TLV9062 | 2 | — | — | — | 8 | 8 | 8 | — | — |
| TLV9064 | 4 | — | — | — | 14 | — | — | 14 | 16 |

# 6 Pin Configuration and Functions

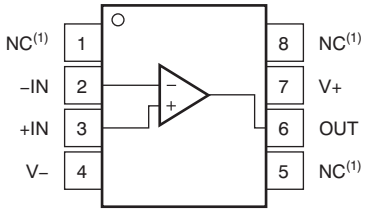
**TLV9061 DBV and DRL Package**
**5-Pin SOT-23 and SOT553**
**Top View**




**TLV9061 DCK Package**
**5-Pin SC70**
**Top View**




**TLV9061 D Package**
**8-Pin SOIC**
**Top View**

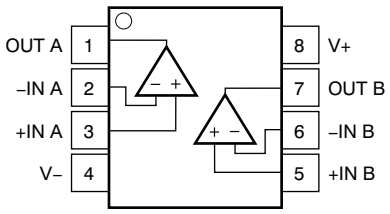



NC - No internal connection

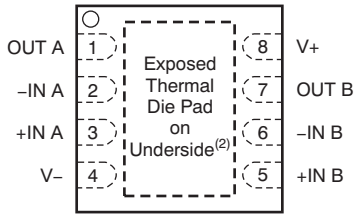
**Pin Functions: TLV9061**

| PIN | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DBV, DRL | DCK | D | | |
| –IN | 4 | 3 | 2 | I | Inverting input |
| +IN | 3 | 1 | 3 | I | Noninverting input |
| OUT | 1 | 4 | 6 | O | Output |
| NC | — | — | 1, 5, 8 | — | No internal connection |
| V– | 2 | 2 | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 5 | 5 | 7 | — | Positive (highest) supply |

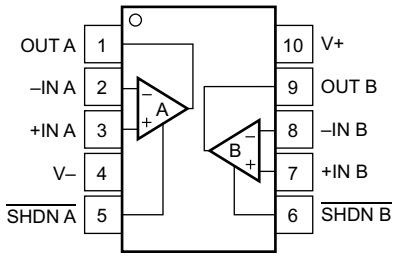
**TLV9062 D, DGK Packages**
**8-Pin SOIC, VSSOP**
**Top View**




**TLV9062 DSG Package**
**8-Pin WSON**
**Top View**



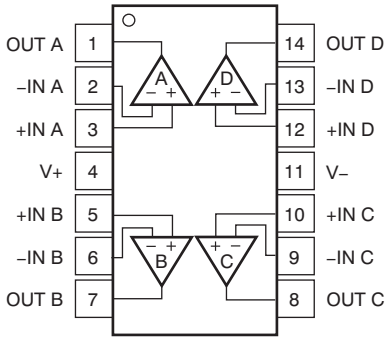

**TLV9062S DGS Package**
**10-Pin VSSOP**
**Top View**




## Pin Functions: TLV9062

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | D, DGK, DSG | DGS | | |
| –IN A | 2 | 2 | I | Inverting input, channel A |
| +IN A | 3 | 3 | I | Noninverting input, channel A |
| –IN B | 6 | 8 | I | Inverting input, channel B |
| +IN B | 5 | 7 | I | Noninverting input, channel B |
| OUT A | 1 | 1 | O | Output, channel A |
| OUT B | 7 | 9 | O | Output, channel B |
| $\overline{\text{SHDN A}}$ | — | 5 | — | Shutdown (logic low), enable (logic high), channel A |
| $\overline{\text{SHDN B}}$ | — | 6 | — | Shutdown (logic low), enable (logic high), channel B |
| V– | 4 | 4 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 8 | 10 | — | Positive (highest) supply |

**TLV9064 D, PW Packages**
**14-Pin SOIC, TSSOP**
**Top View**




## Pin Functions: TLV9064 D and PW

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | D, PW | | |
| –IN A | 2 | I | Inverting input, channel A |
| +IN A | 3 | I | Noninverting input, channel A |
| –IN B | 6 | I | Inverting input, channel B |
| +IN B | 5 | I | Noninverting input, channel B |
| –IN C | 9 | I | Inverting input, channel C |
| +IN C | 10 | I | Noninverting input, channel C |
| –IN D | 13 | I | Inverting input, channel D |
| +IN D | 12 | I | Noninverting input, channel D |
| OUT A | 1 | O | Output, channel A |
| OUT B | 7 | O | Output, channel B |
| OUT C | 8 | O | Output, channel C |
| OUT D | 14 | O | Output, channel D |
| V– | 11 | — | Negative (lowest) supply or ground (for single-supply operation) |
| V+ | 4 | — | Positive (highest) supply |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | | | | 6 | V |
| Signal input pins | Voltage(2) | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential | | (V+) – (V–) + 0.2 | |
| | Current(2) | | –10 | 10 | mA |
| Output short-circuit(3) | | | Continuous | | mA |
| Temperature | Specified, $T_A$ | | –40 | 125 | °C |
| | Junction, $T_J$ | | | 150 | |
| | Storage, $T_{stg}$ | | –65 | 150 | |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

## 7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage | 1.8 | 5.5 | V |
| | Specified temperature | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TLV9062 D (SOIC) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 157.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 104.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 99.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 55.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 99.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics: $V_S$ (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V

at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted);

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_S$ = 5 V | | ±0.3 | ±1.5 | mV |
| | | $V_S$ = 5 V, $T_A$ = –40°C to +125°C | | | ±1.6 | |
| $dV_{OS}/dT$ | Drift | $V_S$ = 5 V, $T_A$ = –40°C to +125°C | | ±0.53 | | µV/°C |
| PSRR | Power-supply rejection ratio | $V_S$ = 1.8 V – 5.5 V, $V_{CM}$ = (V–) | | ±7 | ±80 | µV/V |
| | Channel separation, dc | At dc | | 100 | | dB |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range | $V_S$ = 1.8 V to 5.5 V | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 5.5 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 1.4 V, $T_A$ = –40°C to +125°C | 86 | 103 | | dB |
| | | $V_S$ = 5.5 V, $V_{CM}$ = –0.1 V to 5.6 V, $T_A$ = –40°C to +125°C | 57 | 87 | | |
| | | $V_S$ = 1.8 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 1.4 V, $T_A$ = –40°C to +125°C | | 88 | | |
| | | $V_S$ = 1.8 V, $V_{CM}$ = –0.1 V to 1.9 V, $T_A$ = –40°C to +125°C | | 81 | | |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | | | ±0.5 | | pA |
| $I_{OS}$ | Input offset current | | | ±0.05 | | pA |
| **NOISE** | | | | | | |
| $E_n$ | Input voltage noise (peak-to-peak) | $V_S$ = 5 V, f = 0.1 Hz to 10 Hz | | 4.77 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density | $V_S$ = 5 V, f = 10 kHz | | 10 | | $nV/\sqrt{Hz}$ |
| | | $V_S$ = 5 V, f = 1 kHz | | 16 | | $nV/\sqrt{Hz}$ |
| $i_n$ | Input current noise density | f = 1 kHz | | 10 | | $fA/\sqrt{Hz}$ |
| **INPUT CAPACITANCE** | | | | | | |
| $C_{ID}$ | Differential | | | 2 | | pF |
| $C_{IC}$ | Common-mode | | | 4 | | pF |
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 1.8 V, (V–) + 0.04 V < $V_O$ < (V+) – 0.04 V, $R_L$ = 10 kΩ | | 100 | | dB |
| | | $V_S$ = 5.5 V, (V–) + 0.05 V < $V_O$ < (V+) – 0.05 V, $R_L$ = 10 kΩ | 104 | 130 | | |
| | | $V_S$ = 1.8 V, (V–) + 0.06 V < $V_O$ < (V+) – 0.06 V, $R_L$ = 2 kΩ | | 100 | | |
| | | $V_S$ = 5.5 V, (V–) + 0.15 V < $V_O$ < (V+) – 0.15 V, $R_L$ = 2 kΩ | | 130 | | |
| **FREQUENCY RESPONSE** | | | | | | |
| GBP | Gain bandwidth product | $V_S$ = 5 V, G = +1 | | 10 | | MHz |
| $\varphi_m$ | Phase margin | $V_S$ = 5 V, G = +1 | | 55 | | Degrees |
| SR | Slew rate | $V_S$ = 5 V, G = +1 | | 6.5 | | V/µs |
| $t_S$ | Settling time | To 0.1%, $V_S$ = 5 V, 2-V step , G = +1, $C_L$ = 100 pF | | 0.5 | | µs |
| | | To 0.01%, $V_S$ = 5 V, 2-V step , G = +1, $C_L$ = 100 pF | | 1 | | |
| $t_{OR}$ | Overload recovery time | $V_S$ = 5 V, $V_{IN}$ × gain > $V_S$ | | 0.2 | | µs |
| THD + N | Total harmonic distortion + noise(1) | $V_S$ = 5 V, $V_O$ = 1 $V_{RMS}$, G = +1, f = 1 kHz | | 0.0008% | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from supply rails | $V_S$ = 5.5 V, $R_L$ = 10 kΩ, | | | 15 | mV |
| | | $V_S$ = 5.5 V, $R_L$ = 2 kΩ, | | | 25 | |
| $I_{SC}$ | Short-circuit current | $V_S$ = 5 V | | ±50 | | mA |
| $Z_O$ | Open-loop output impedance | $V_S$ = 5 V, f = 10 MHz | | 100 | | Ω |
| **POWER SUPPLY** | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $V_S$ = 5.5 V, $I_O$ = 0 mA, | | 538 | 750 | µA |
| | | $V_S$ = 5.5 V, $I_O$ = 0 mA, $T_A$ = –40°C to +125°C | | | 800 | |

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

## 7.6 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

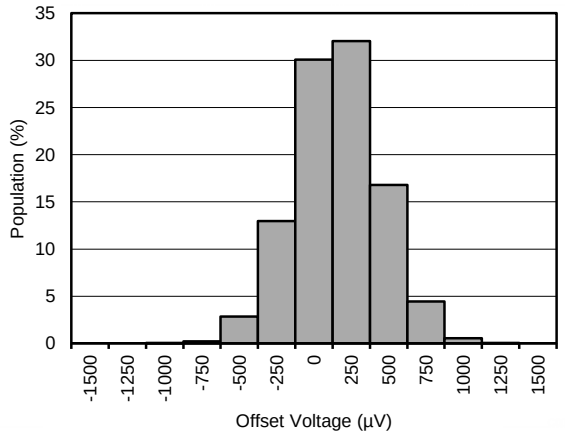
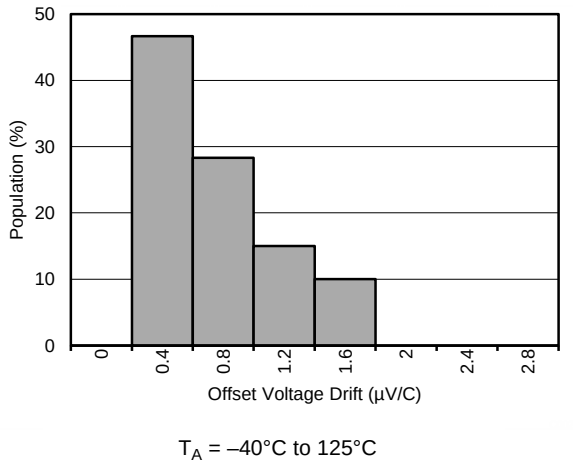



**Figure 1. Offset Voltage Production Distribution**




$T_A$ = –40°C to 125°C

**Figure 2. Offset Voltage Drift Distribution**

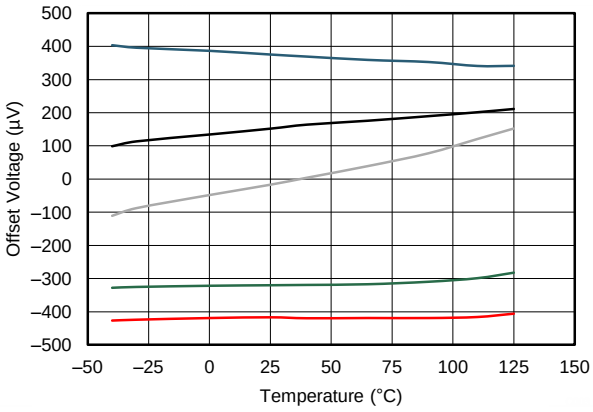
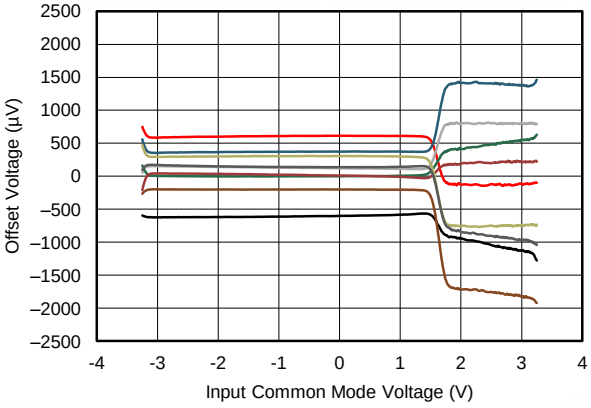
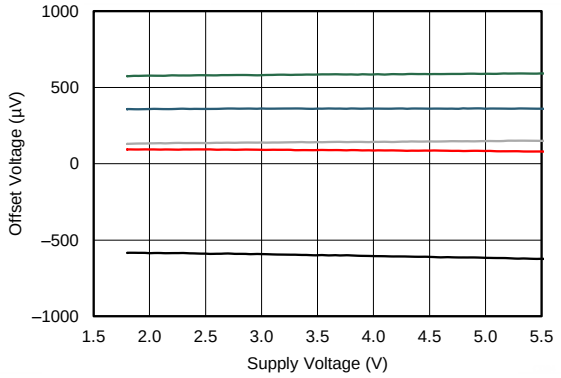



**Figure 3. Offset Voltage vs Temperature**



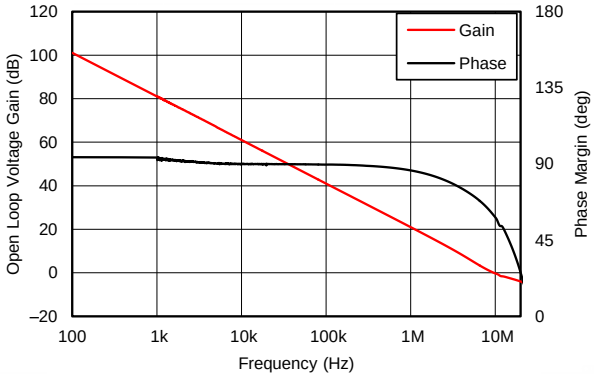

V+ = 2.75 V, V– = –2.75 V

**Figure 4. Offset Voltage vs Common-Mode Voltage**




$V_S$ = 1.8 V to 5.5 V

**Figure 5. Offset Voltage vs Power Supply**




$C_L$ = 10 pF

**Figure 6. Open-Loop Gain and Phase vs Frequency**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

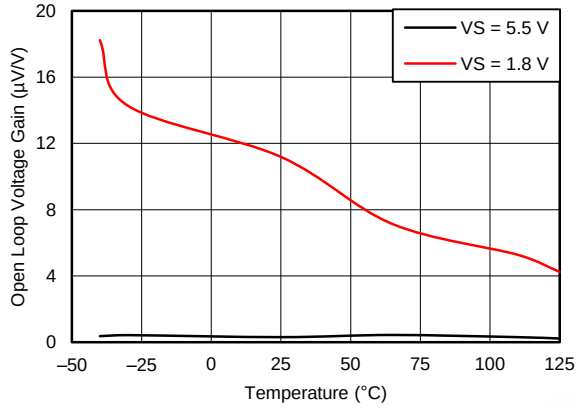



**Figure 7. Open-Loop Gain vs Temperature**

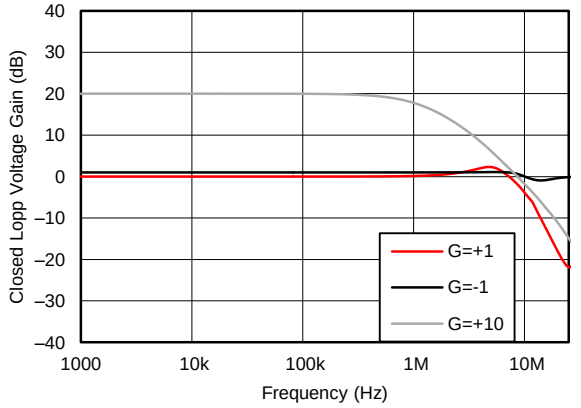



**Figure 8. Closed-Loop Gain vs Frequency**

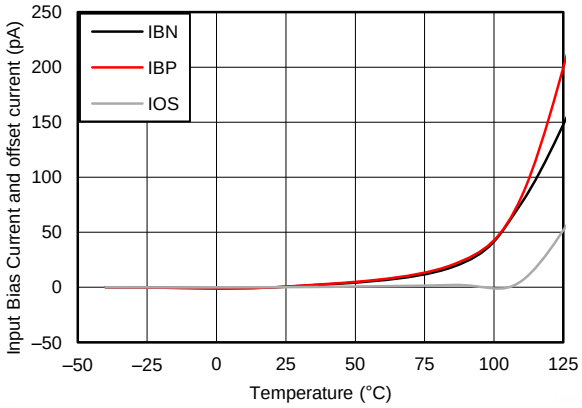



**Figure 9. Input Bias Current vs Temperature**

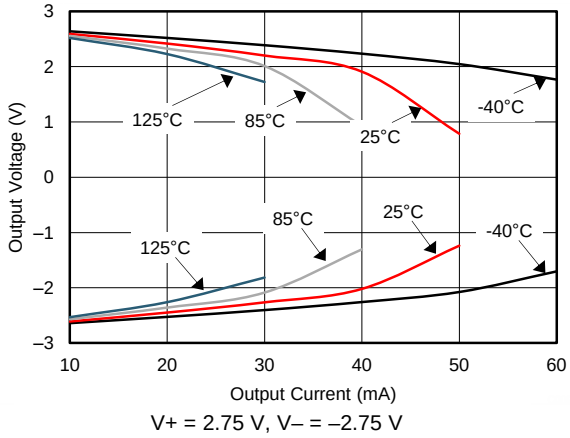



**Figure 10. Output Voltage Swing vs Output Current**

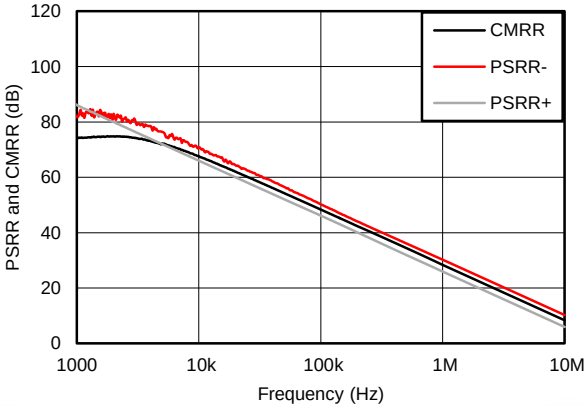



**Figure 11. CMRR and PSRR vs Frequency (Referred to Input)**

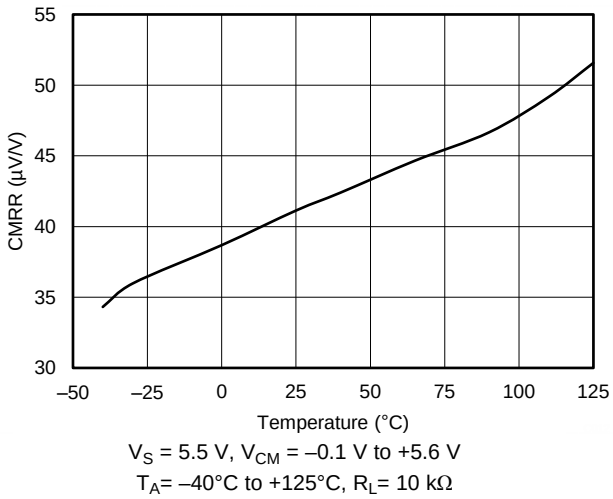
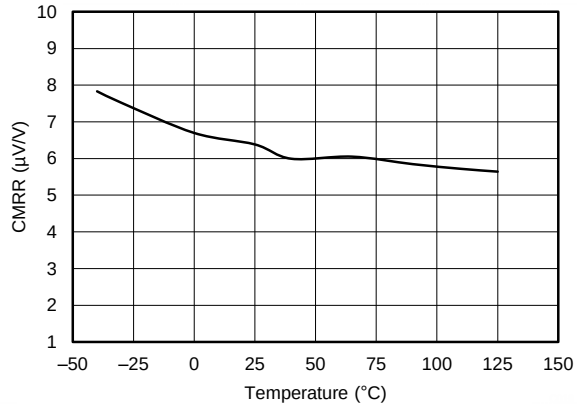



**Figure 12. CMRR vs Temperature**

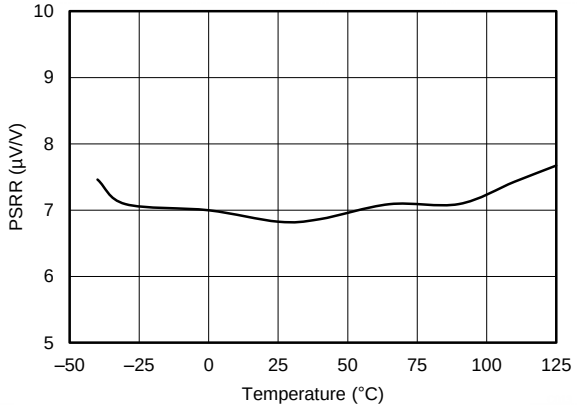
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)



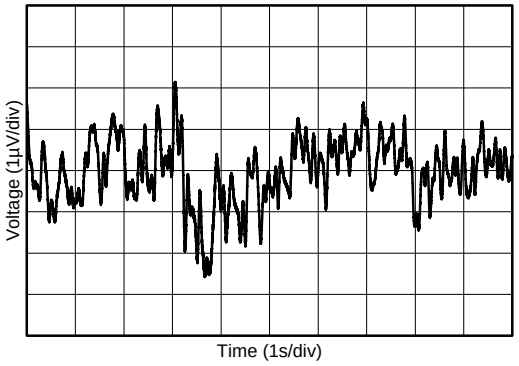

$V_S$ = 5.5 V, $V_{CM}$ = (V-) - 0.1 V to (V+) - 1.4 V
$T_A$= –40°C to +125°C, $R_L$= 10 kΩ

**Figure 13. CMRR vs Temperature**




$V_S$ = 1.8 V to 5.5 V

**Figure 14. PSRR vs Temperature**




$V_S$ = 1.8 V to 5.5 V

**Figure 15. 0.1-Hz to 10-Hz Input Voltage Noise**

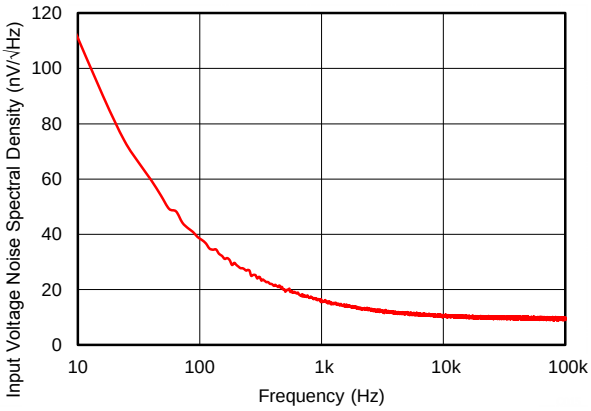
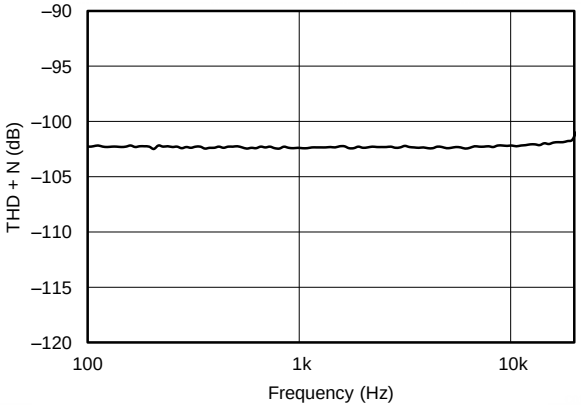
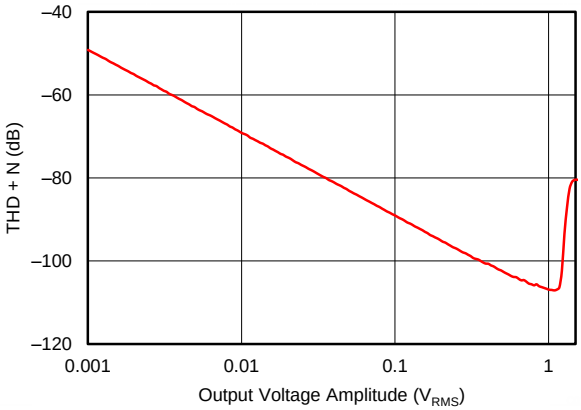



**Figure 16. Input Voltage Noise Spectral Density vs Frequency**




$V_S$ = 5.5 V, $V_{CM}$ = 2.5 V, $R_L$ = 2 kΩ, G = +1, BW = 80kHz
$V_{OUT}$ = 0.5 $V_{RMS}$

**Figure 17. THD + N vs Frequency**

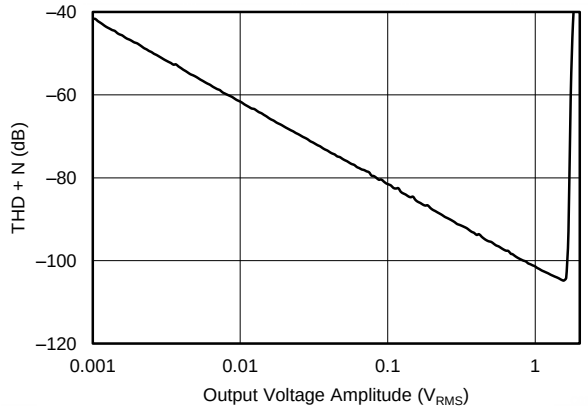



$V_S$ = 5.5 V, $V_{CM}$ = 2.5 V, $R_L$ = 2 kΩ, G = +1
BW = 80kHz, f = 1 kHz

**Figure 18. THD + N vs Amplitude**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)




$V_S$ = 5.5 V, $V_{CM}$ = 2.5 V, $R_L$ = 2 kΩ, G = –1
BW = 80 kHz, f = 1 kHz

**Figure 19. THD + N vs Amplitude**

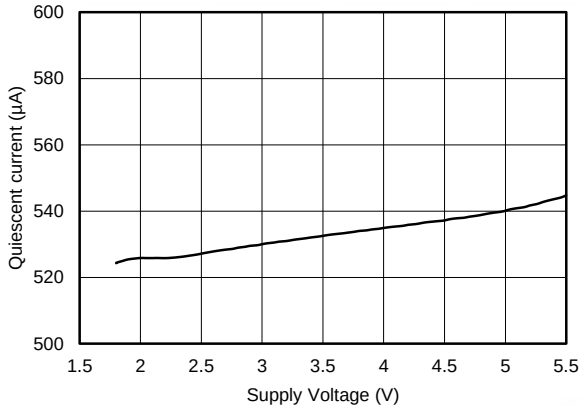



**Figure 20. Quiescent Current vs Supply Voltage**

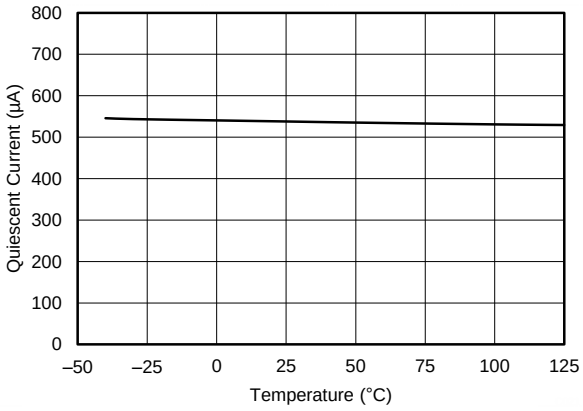



**Figure 21. Quiescent Current vs Temperature**

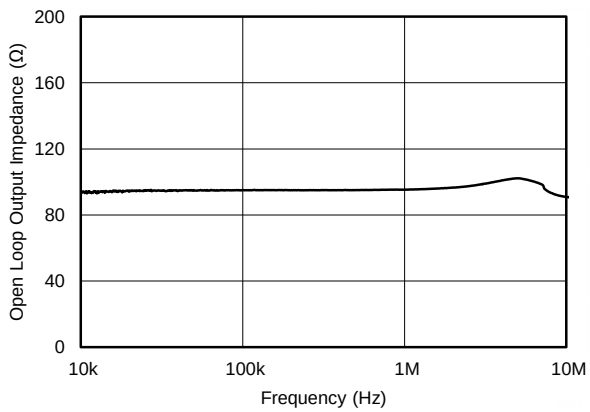
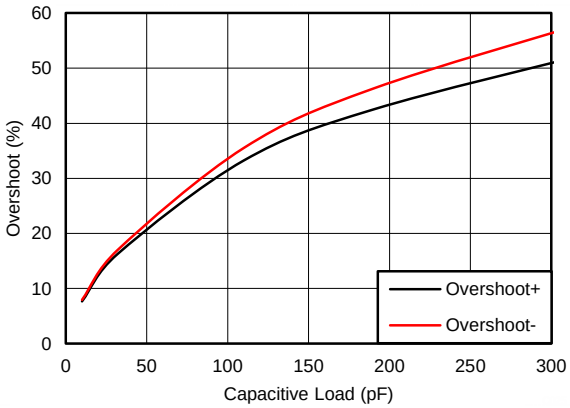
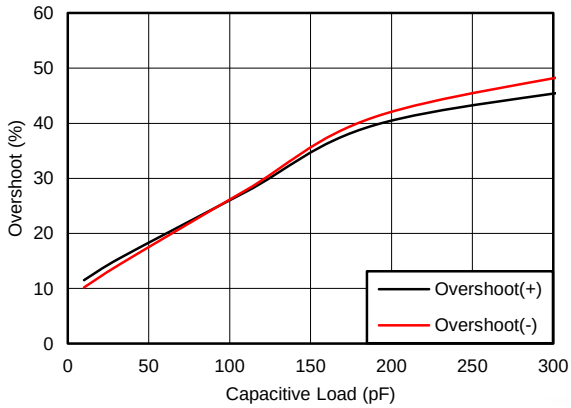



**Figure 22. Open-Loop Output Impedance vs Frequency**




V+ = 2.75 V, V– = –2.75 V , G = +1 V/V, $R_L$ = 10 kΩ
$V_{OUT}$ step = 100 $mV_{p-p}$

**Figure 23. Small-Signal Overshoot vs Load Capacitance**

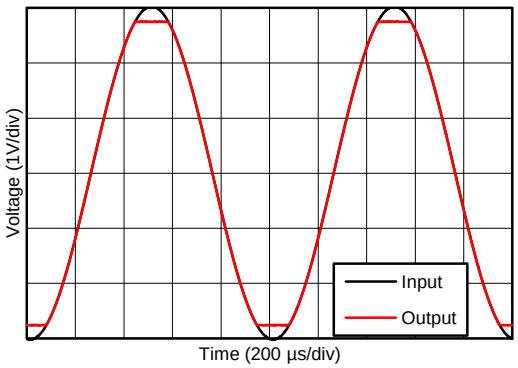



V+ = 2.75 V, V– = –2.75 V , G = -1 V/V, $R_L$ = 10 kΩ
$V_{OUT}$ step = 100 $mV_{p-p}$

**Figure 24. Small-Signal Overshoot vs Load Capacitance**

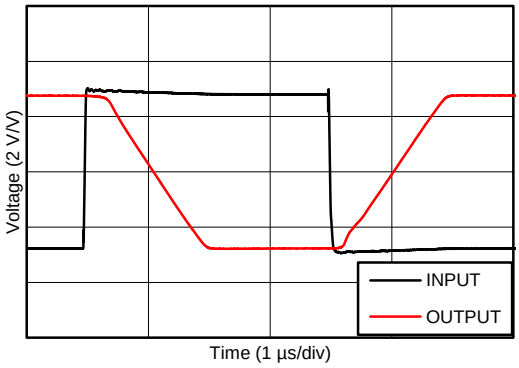
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)



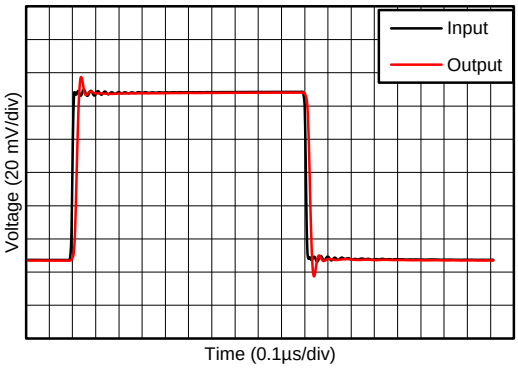

V+ = 2.75 V, V– = –2.75 V

**Figure 25. No Phase Reversal**



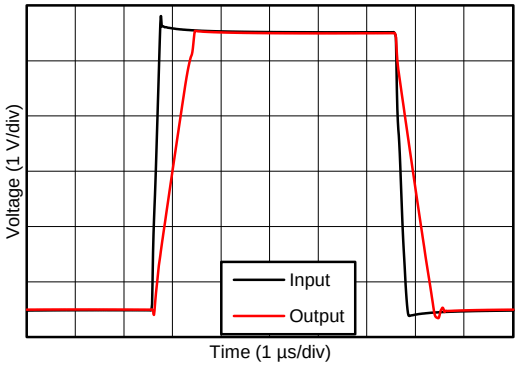

V+ = 2.75 V, V– = –2.75 V , G = –10 V/V

**Figure 26. Overload Recovery**




V+ = 2.75 V, V– = –2.75 V, G = 1 V/V

**Figure 27. Small-Signal Step Response**




V+ = 2.75 V, V– = –2.75 V, $C_L$ = 100 pF, G = 1 V/V

**Figure 28. Large-Signal Step Response**

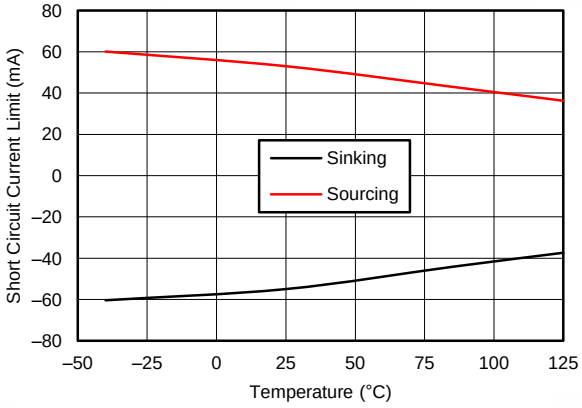
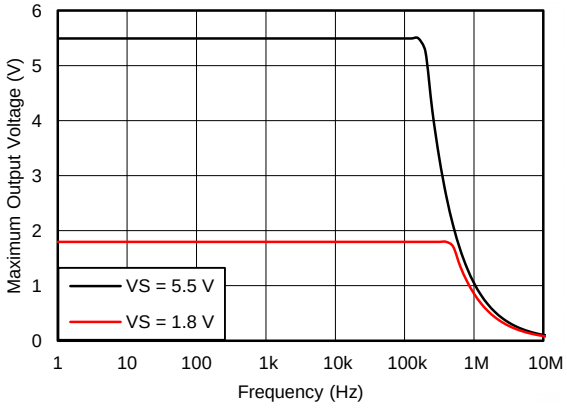



**Figure 29. Short-Circuit Current vs Temperature**




$R_L$ = 10 kΩ, $C_L$ = 10 pF

**Figure 30. Maximum Output Voltage vs Frequency and Supply Voltage**

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = 5.5 V, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{OUT}$ = $V_S$ / 2 (unless otherwise noted)

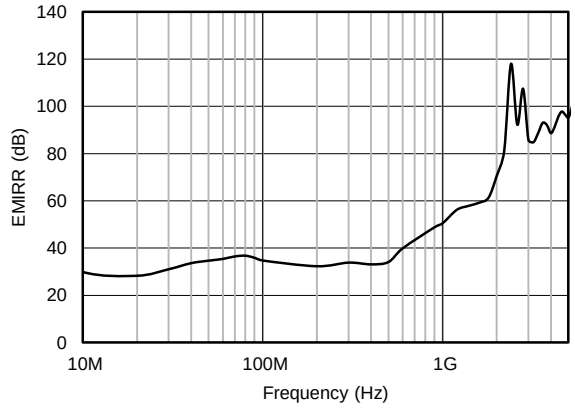



**Figure 31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency**

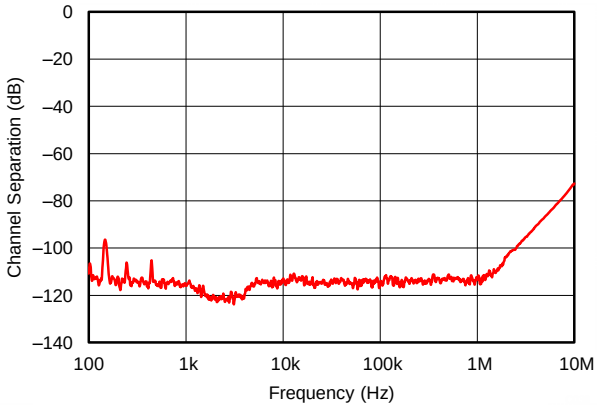



**Figure 32. Channel Separation vs Frequency**

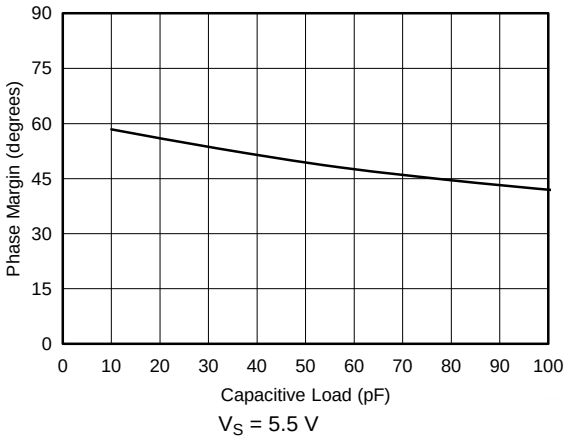



**Figure 33. Phase Margin vs Capacitive Load**

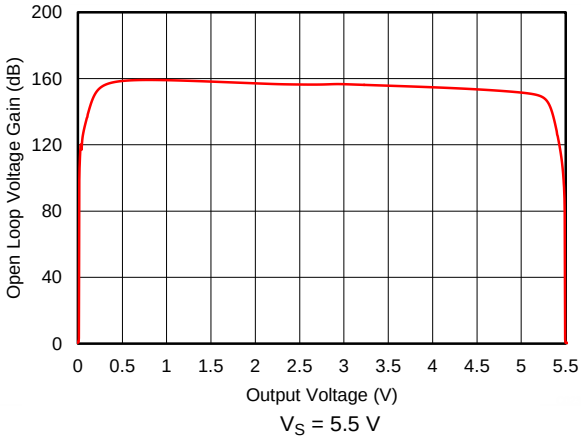



**Figure 34. Open Loop Voltage Gain vs Output Voltage**

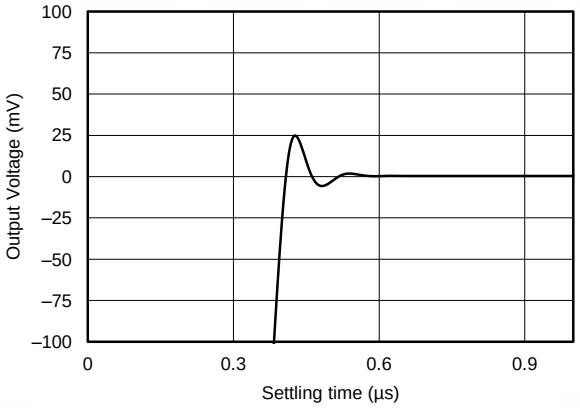



**Figure 35. Large Signal Settling Time (Positive)**

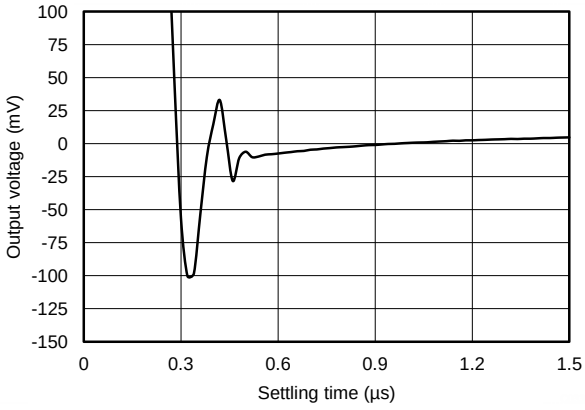


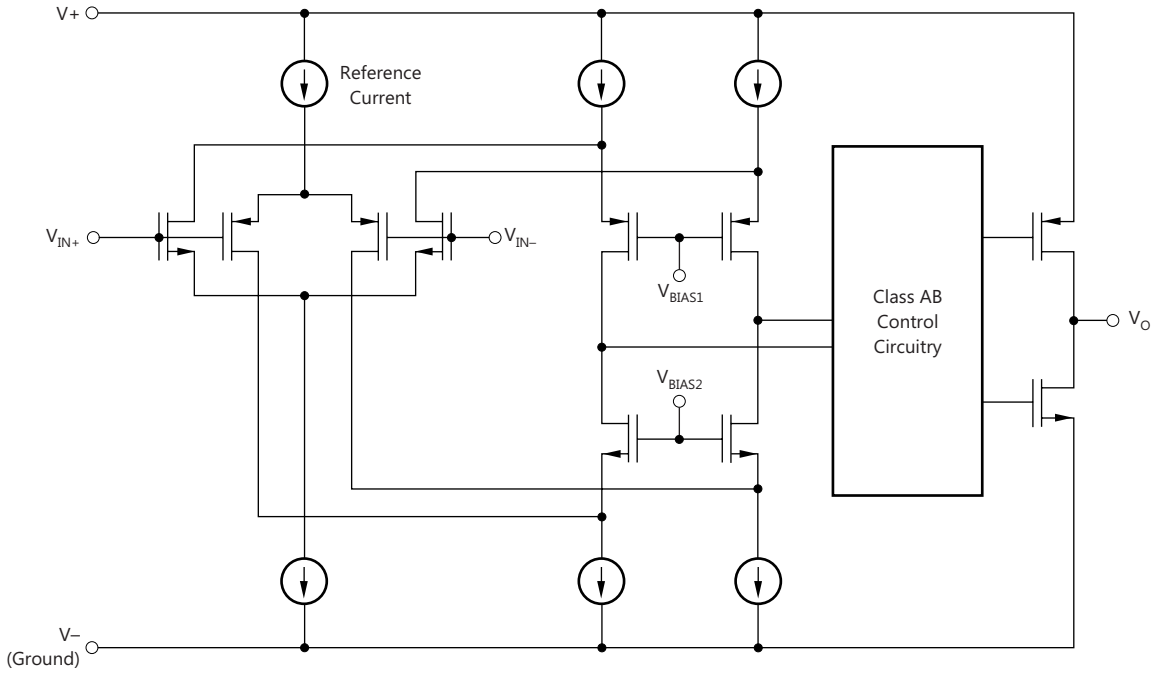

**Figure 36. Large Signal Settling Time (Negative)**

# 8 Detailed Description

## 8.1 Overview

The TLV906x series is a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling analog-to-digital converters (ADCs).

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

### 8.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

### 8.3.3 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x series is approximately 200 ns.

## 8.4 Device Functional Modes

The TLV906x family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TLV906x series features 10-MHz bandwidth and 6.5-V/µs slew rate with only 538-µA of supply current per channel, providing good ac performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 10 nV / $\sqrt{\text{Hz}}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

## 9.2 Typical Application

Figure 37 shows the TLV906x configured in a low-side current sensing application.

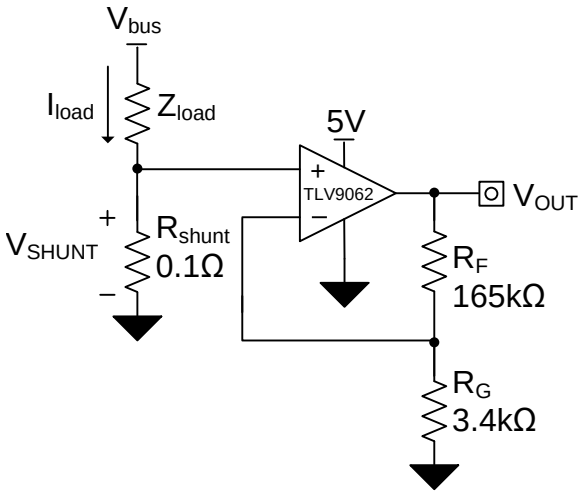



**Figure 37. TLV906x in a Low-Side, Current-Sensing Application**

### 9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 37 is given in Equation 1

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current ($I_{LOAD}$) produces a voltage drop across the shunt resistor ($R_{SHUNT}$). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using Equation 2, $R_{SHUNT}$ is calculated to be 100 mΩ. The voltage drop produced by $I_{LOAD}$ and $R_{SHUNT}$ is amplified by the TLV906x to produce an output voltage of roughly 0 V to 4.95 V. The gain needed by the TLV906x to produce the necessary output voltage is calculated using Equation 3:

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using Equation 3, the required gain is calculated to be 49.5 V/V, which is set with resistors $R_F$ and $R_G$. Equation 4 is used to size the resistors, $R_F$ and $R_G$, to set the gain of the TLV906x to 49.5 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \quad (4)$$

Choosing $R_F$ as 165 kΩ and $R_G$ as 3.4 kΩ provides a combination that equals roughly 49.5 V/V. Figure 38 shows the measured transfer function of the circuit shown in Figure 37.

### 9.2.3 Application Curve

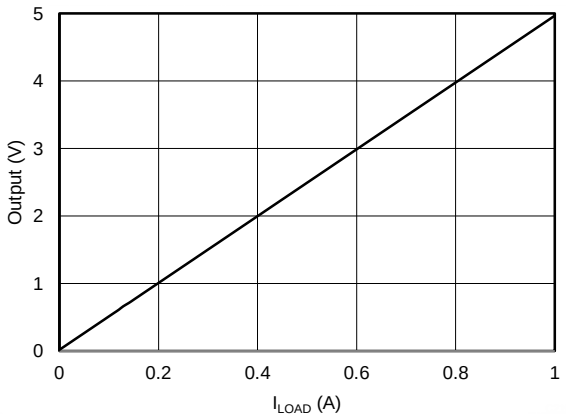



**Figure 38. Low-Side, Current-Sense, Transfer Function**

# 10 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

**CAUTION**

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the section.

## 10.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10-mA, as stated in the *Absolute Maximum Ratings* table. Figure 39 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

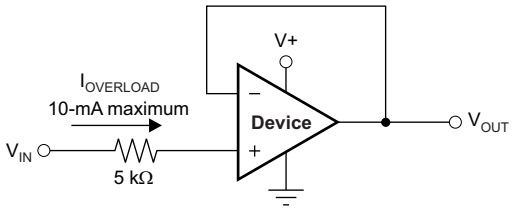



**Figure 39. Input Current Protection**

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information refer to, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 41, keeping RF and RG close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

## 11.2 Layout Example

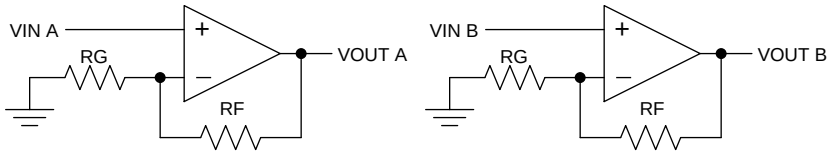



**Figure 40. Schematic Representation for Figure 41**

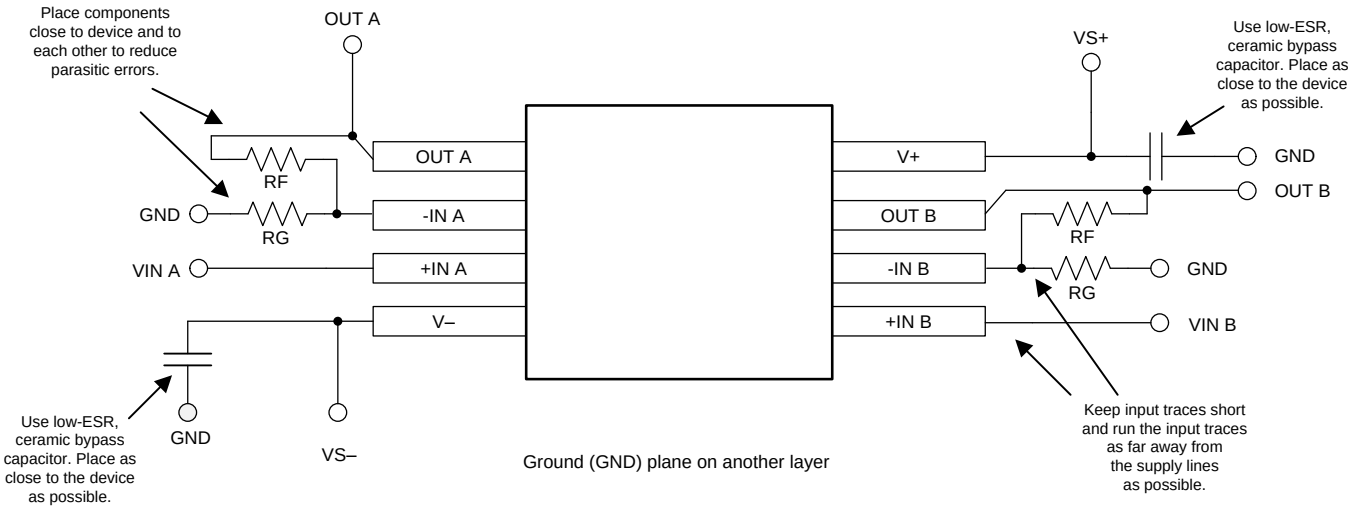



**Figure 41. Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

*TLVx313 Low-Power, Rail-to-Rail In/Out, 500-μV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems* (SBOS753).

*TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier* (SBOS754).

*EMI Rejection Ratio of Operational Amplifiers* (SBOA128).

*QFN/SON PCB Attachment* (SLUA271).

*Quad Flatpack No-Lead Logic Packages* (SCBA017).

*Circuit Board Layout Techniques* (SLOA089).

*Single-Ended Input to Differential Output Conversion Circuit Reference Design* (TIPD131).

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TLV9061 | Click here | Click here | Click here | Click here | Click here |
| TLV9062 | Click here | Click here | Click here | Click here | Click here |
| TLV9064 | Click here | Click here | Click here | Click here | Click here |

## 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTLV9062IDSGR | ACTIVE | WSON | DSG | 8 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |
| TLV9062IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-2-260C-1 YEAR | -40 to 125 | TL9062 | Samples |
| TLV9062IDSGR | PREVIEW | WSON | DSG | 8 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | |
| TLV9062IDSGT | PREVIEW | WSON | DSG | 8 | 250 | TBD | Call TI | Call TI | -40 to 125 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

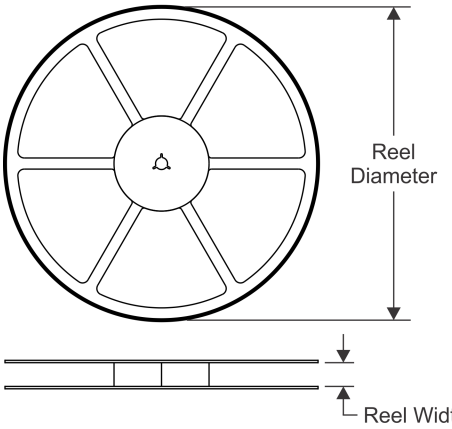
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

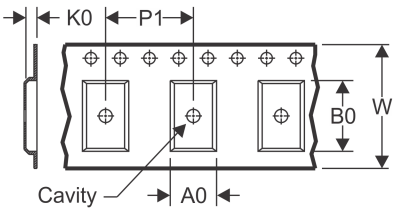
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

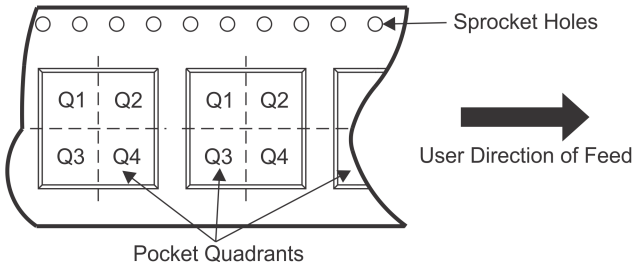



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

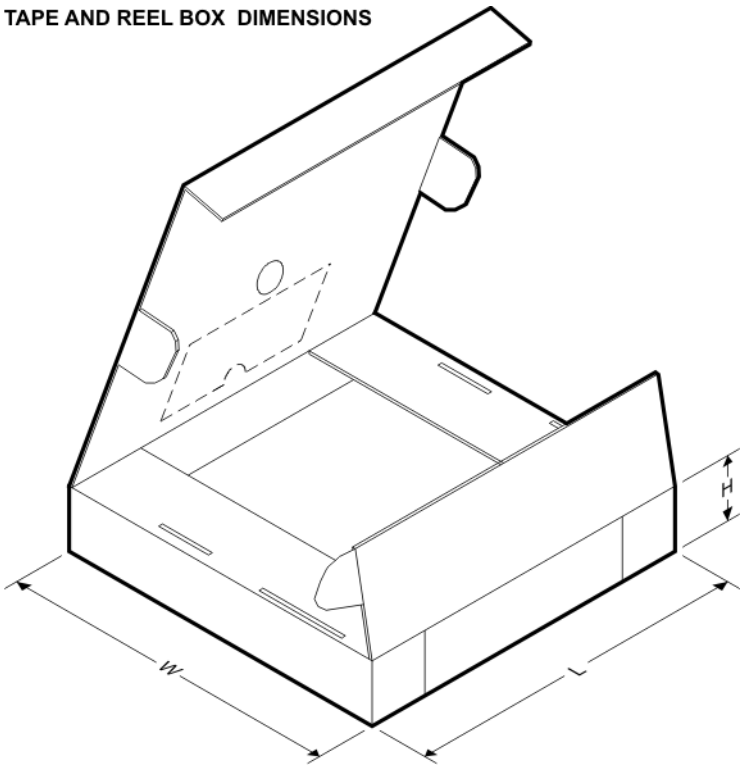
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV9062IDR | SOIC | D | 8 | 2500 | 330.0 | 15.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

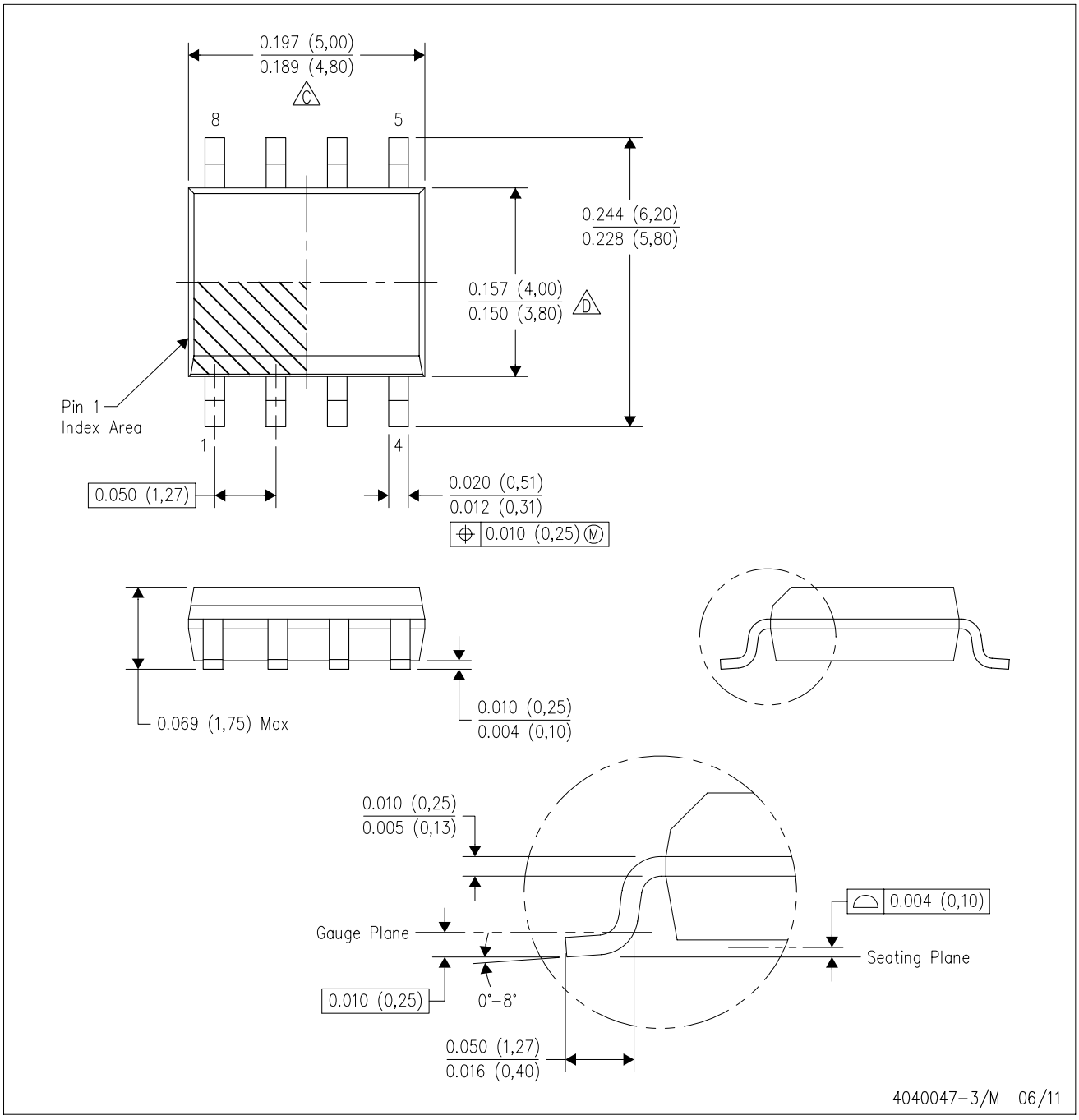
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

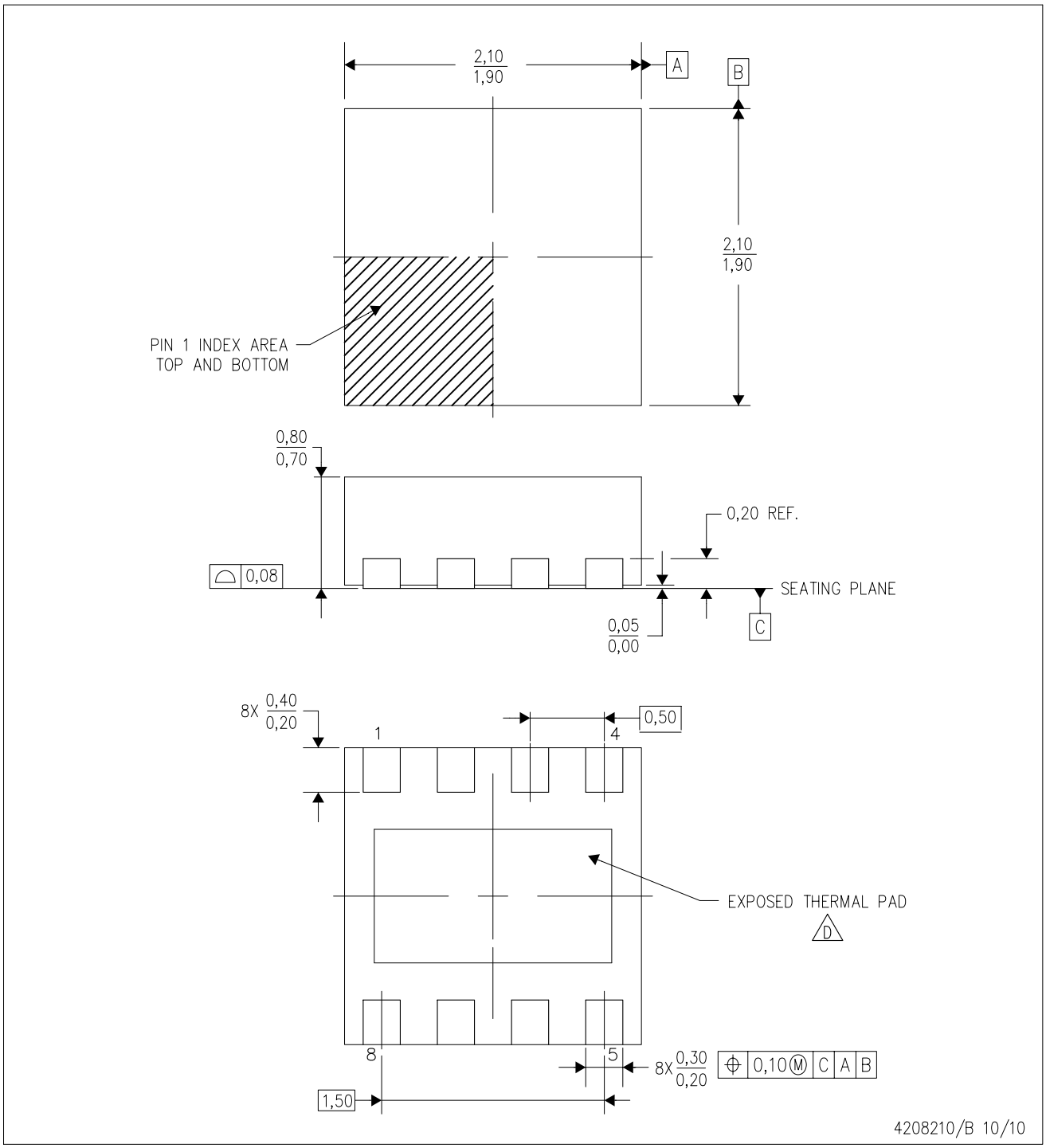
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV9062IDR | SOIC | D | 8 | 2500 | 333.2 | 345.9 | 28.6 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

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