3-V to 17-V 2-A Step-Down Converter in 3-mm × 3-mm QFN Package

Check for Samples: TPS62140, TPS62141, TPS62142, TPS62143

FEATURES

- **DCS-Control™ Topology**
- **Input Voltage Range: 3 V to 17 V**
- **Up to 2-A Output Current**
- **Adjustable Output Voltage from 0.9 V to 6 V**
- **Pin-Selectable Output Voltage (Nominal, +5%)**
- **Programmable Soft Start and Tracking**
- **Seamless Power-Save Mode Transition**
- **Quiescent Current of 17 μA (typ.)**
- **Selectable Operating Frequency**
- **Power-Good Output**
- **100% Duty-Cycle Mode**
- **Short-Circuit Protection**
- **Overtemperature Protection**
- **Available in a 3-mm × 3-mm, QFN-16 Package**

APPLICATIONS

- **Standard 12-V Rail Supplies**
- **POL Supply From Single or Multiple Li-Ion Battery**
- **Solid-State Disk Drives**
- **Embedded Systems**
- **LDO Replacement**
- **Mobile PCs, Tablet, Modems, Cameras**

DESCRIPTION

The TPS6214X family is an easy-to-use synchronous step-down dc-dc converter optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response by use of the DCS-Control™ topology.

With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other batteries, as well as from 12-V intermediate power rails. It supports up to 2 A of continuous output current at output voltages between 0.9 V and 6 V (with 100% duty-cycle mode).

The output voltage start-up ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable (EN) and open-drain power-good (PG) pins.

In power-save mode, the devices show quiescent current of about 17 μA from VIN. Power-save mode, entered automatically and seamlessly if load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 μA.

The device, available in adjustable and fixed output voltage versions, is packaged in a 16-pin QFN package measuring 3 mm × 3 mm (RGT).

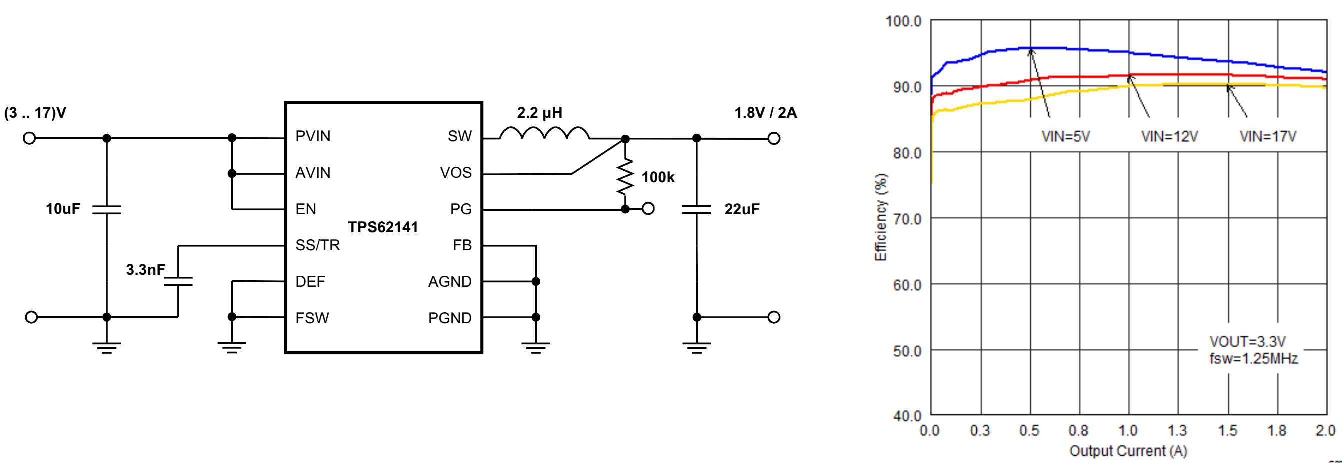


Figure 1. Typical Application and Efficiency

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	OUTPUT VOLTAGE	PART NUMBER(2)	PACKAGE	ORDERING	PACKAGE MARKING
–40°C to 85°C	Adjustable	TPS62140	16-Pin QFN	TPS62140RGT	QTZ
	1.8 V	TPS62141		TPS62141RGT	QWA
	3.3 V	TPS62142		TPS62142RGT	QWB
	5 V	TPS62143		TPS62143RGT	QWC

(1) For detailed ordering information, see the PACKAGE OPTION ADDENDUM section at the end of this data sheet.
(2) Contact the factory to check availability of other fixed output voltage versions.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Pin voltage range(2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR	–0.3	V_{IN}+0.3	
	SW	–0.3	V_{IN}+0.3	V
	DEF, FSW, FB, PG, VOS	–0.3	7	V
Power-good sink current	PG		10	mA
Temperature range	Operating junction temperature range, T_J	–40	125	°C
	Storage temperature range, T_{stg}	–65	150	
ESD rating(3)	HBM Human-body model		2	kV
	CDM Charged-device model		0.5	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS6214X	UNITS
		RGT (16) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	29.1	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance	15	
θ_{JB}	Junction-to-board thermal resistance	11	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	10	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance	3.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{IN} (at AVIN and P VIN)	3		17	V
Operating free-air temperature, T_A	–40		85	°C
Operating junction temperature, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

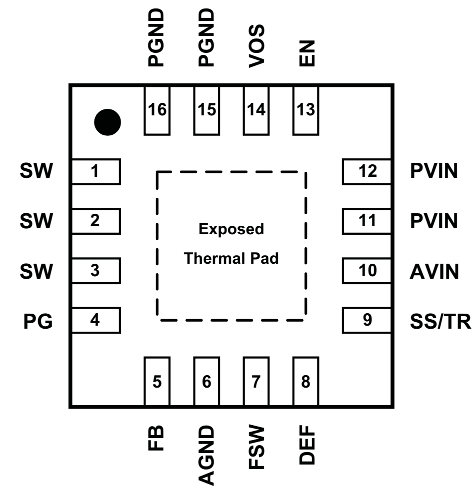
over free-air temperature range (T_A=-40°C to +85°C), typical values at VIN=AVIN=PVIN=12V and T_A=25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range(1)		3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching		17	25	µA
I_{SD}	Shutdown current(2)	EN = Low		1.5	4	µA
V_{UVLO}	Undervoltage lockout threshold	Falling input voltage	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, DEF, FSW, SS/TR, PG)						
V_H	High-level input threshold voltage (EN, DEF, FSW)		0.9			V
V_L	Low-level input threshold voltage (EN, DEF, FSW)				0.3	V
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN, DEF, FSW = V_{IN} or GND		0.01	1	µA
V_{TH_PG}	Power-good threshold voltage	Rising (%V_{OUT})	92	95	98	%
		Falling (%V_{OUT})	87	90	93	
V_{OL_PG}	Power-good output low	I_{PG}= –2 mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V		1	400	nA
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	µA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V		90	170	mΩ
		V_{IN} = 3 V		120		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V		40	70	mΩ
		V_{IN} = 3 V		50		
I_{LIMF}	High-side MOSFET forward current limit(3)	V_{IN} = 12 V, T_A = 25°C	2.45	3	3.5	A
OUTPUT						
VREF	Internal reference voltage(4)			0.8		V
I_{LKG_FB}	Input leakage current (FB)	TPS62140, V_{FB} = 0.8 V		1	100	nA
V_{OUT}	Output voltage range (TPS62140)	V_{IN} ≥ V_{OUT}	0.9		6.0	V
	DEF (output voltage programming)	DEF = 0 (GND)		VOUT		
		DEF = 1 (V_{OUT})		VOUT + 5%		
	Initial output voltage accuracy(5)	PWM mode operation, V_{IN} ≥ V_{OUT} + 1 V	–1.8		1.8	%
		Power-save mode operation, C_{OUT}=22µF	–2.3		2.8	
	Load regulation(6)	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation		0.05		%/A
	Line regulation(6)	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, PWM mode operation		0.02		%/V

(1) The device is still functional down to undervoltage lockout (see parameter V_{UVLO}).
(2) Current into AVIN + PVIN pins
(3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit and Short Circuit Protection section).
(4) This is the voltage regulated at the FB pin.
(5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For the fixed-voltage versions the (internal) resistive divider is included.
(6) Line and load regulation depend on external component selection and layout (see Figure 17 and Figure 18).

DEVICE INFORMATION

RGT PACKAGE
(TOP VIEW)

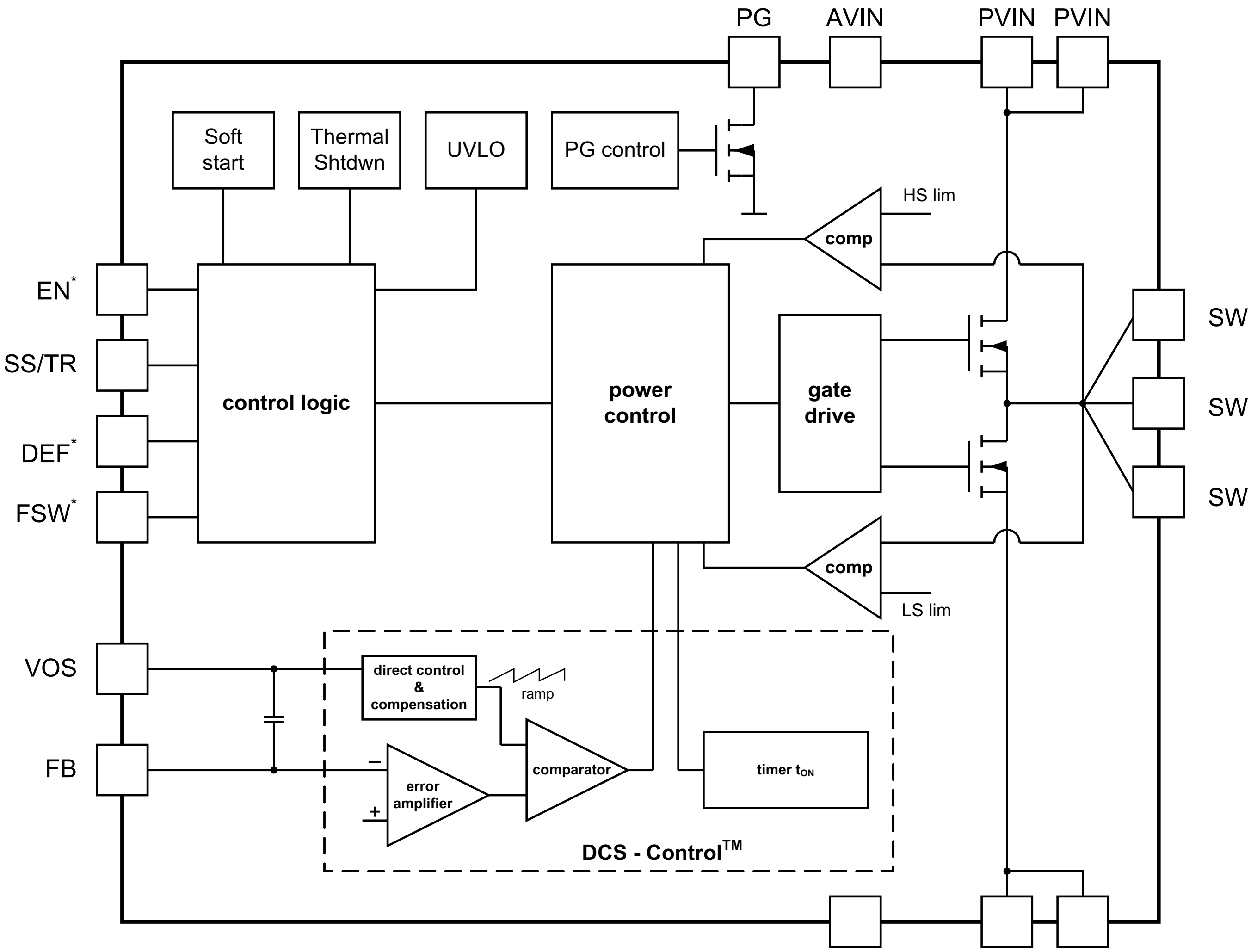


Terminal Functions

PIN (1)		I/O	DESCRIPTION
NAME	NO.		
SW	1, 2 ,3	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	4	O	Output power-good (High = VOUT ready, Low = VOUT below nominal regulation); open-drain (requires pullup resistor; goes high-impedance when device is switched off)
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. Its recommended to connect FB to AGND on fixed output-voltage versions for improved thermal performance.
AGND	6	–	Analog ground
FSW	7	I	Switching frequency select (Low ≈ 2.5 MHz, High ≈ 1.25 MHz for typical operation) (2)
DEF	8	I	Output voltage scaling (Low = nominal, High = nominal + 5%) (2)
SS/TR	9	I	Soft-start / tracking pin. An external capacitor connected to this pin sets the internal voltage-reference rise time. It can be used for tracking and sequencing.
AVIN	10	I	Supply voltage for control circuitry. Connect to same source as PVIN.
PVIN	11, 12	I	Supply voltage for power stage. Connect to same source as AVIN.
EN	13	I	Enable input (High = enabled, Low = disabled) (2)
VOS	14	I	Output-voltage sense pin and connection for the control loop circuitry.
PGND	15, 16	–	Power ground
Exposed thermal pad		–	Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see the DETAILED DESCRIPTION and APPLICATION INFORMATION sections.
(2) An internal pulldown resistor keeps the logic level low, if pin is floating.

FUNCTIONAL BLOCK DIAGRAM



* This pin is connected to a pull down resistor internally (see Detailed Description section).

Figure 2. TPS62140 (Adjustable Output Voltage)

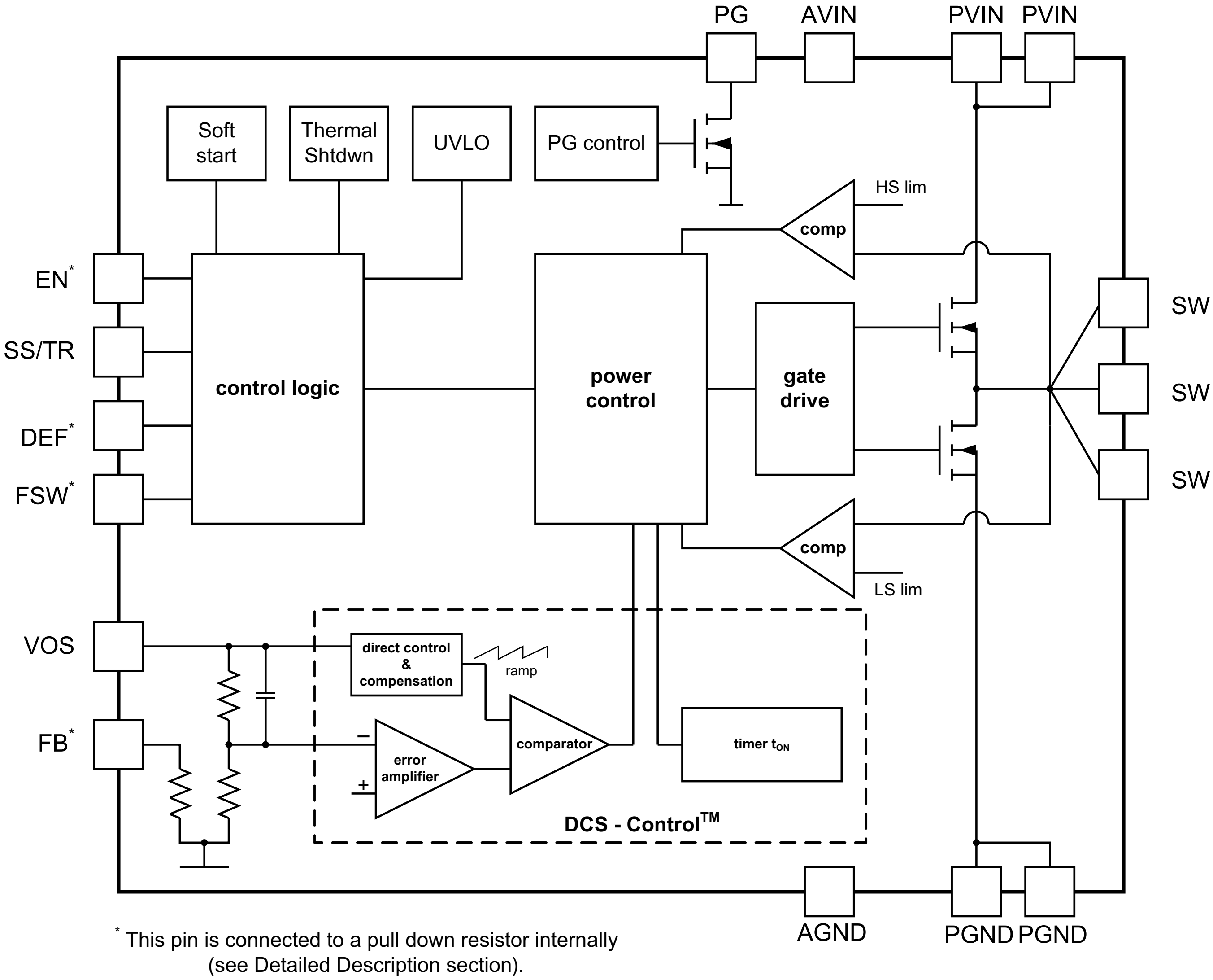


Figure 3. TPS62141/2/3 (Fixed Output Voltage)

PARAMETER MEASUREMENT INFORMATION

List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 2-A step-down converter, QFN	TPS62140RGT, Texas Instruments
L1	2.2-μH, 3.1-A, 0.165 in × 0.165 in	XFL4020-222MEB, Coilcraft
Cin	10-μF, 25-V, ceramic	Standard
Cout	22-μF, 6.3-V, ceramic	Standard
Cs	3300-pF, 25-V, ceramic	
R1	Dependent on Vout	
R2	Dependent on Vout	
R3	100-kΩ, chip, 0603, 1/16W, 1%	Standard

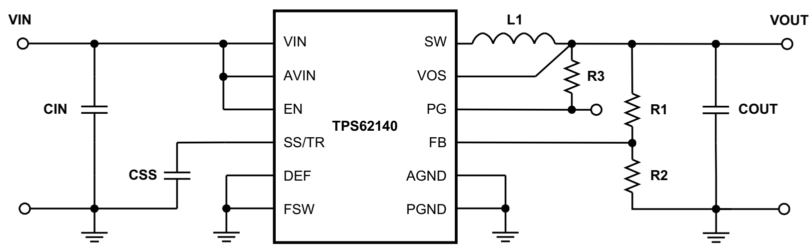


Figure 4. Measurement Setup

TYPICAL CHARACTERISTICS

Table of Graphs

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Efficiency	vs Output Current, vs Input Voltage	5–16
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	Typical PWM Mode Operation	35
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EFFICIENCY vs OUTPUT CURRENT

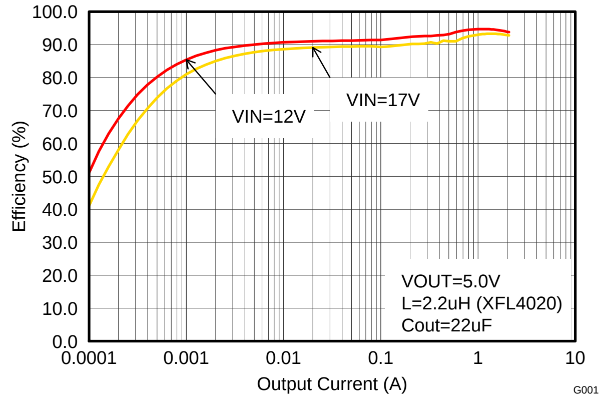

Figure 5. Efficiency With 1.25 MHz, Vout = 5 V

EFFICIENCY vs INPUT VOLTAGE

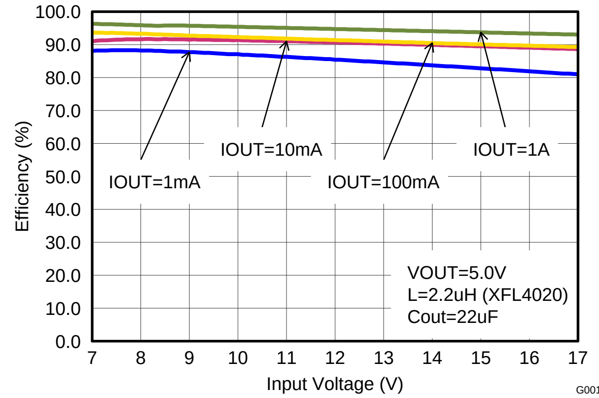

Figure 6. Efficiency With 1.25 MHz, Vout = 5 V

EFFICIENCY vs OUTPUT CURRENT

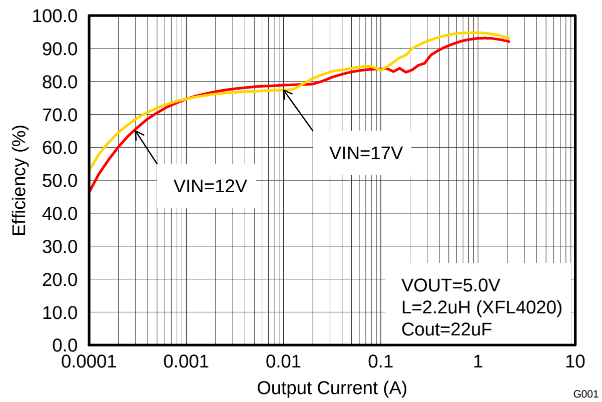

Figure 7. Efficiency With 2.5 MHz, Vout = 5 V

EFFICIENCY vs INPUT VOLTAGE

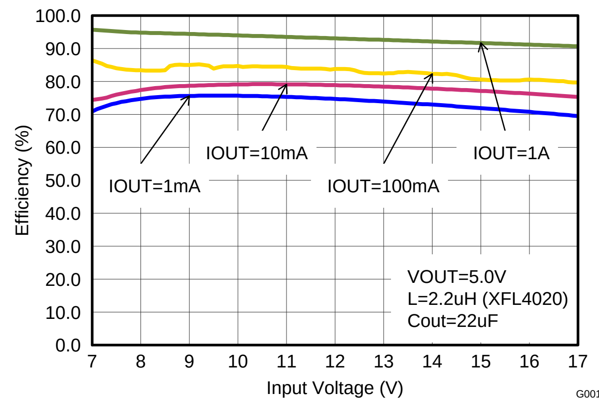

Figure 8. Efficiency With 2.5 MHz, Vout = 5 V

EFFICIENCY vs OUTPUT CURRENT

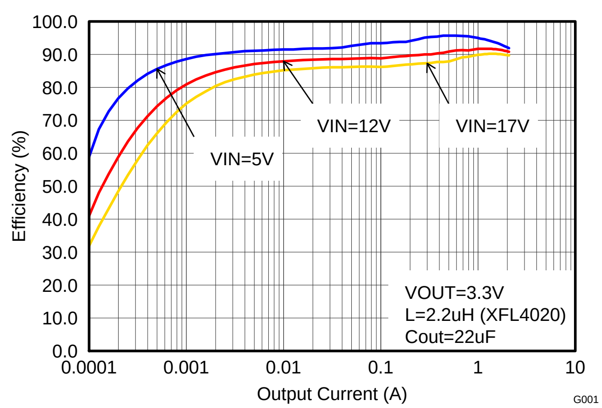

Figure 9. Efficiency With 1.25 MHz, Vout = 3.3 V

EFFICIENCY vs INPUT VOLTAGE

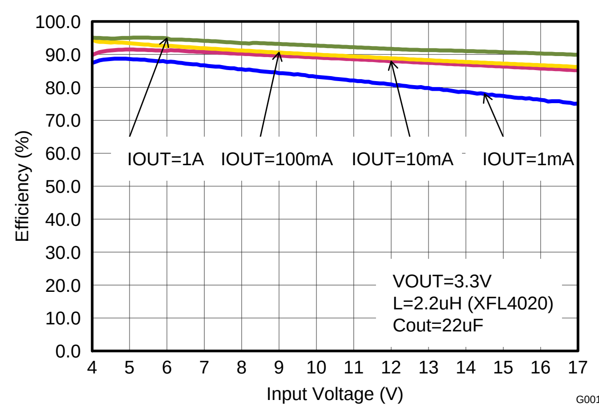

Figure 10. Efficiency With 1.25 MHz, Vout = 3.3 V

EFFICIENCY
vs
OUTPUT CURRENT

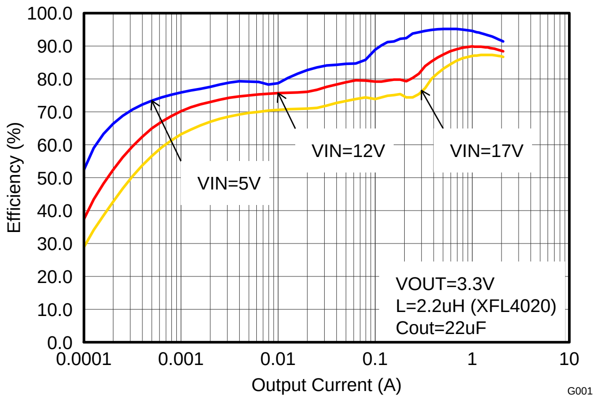

Figure 11. Efficiency With 2.5 MHz, Vout = 3.3 V

EFFICIENCY
vs
INPUT VOLTAGE

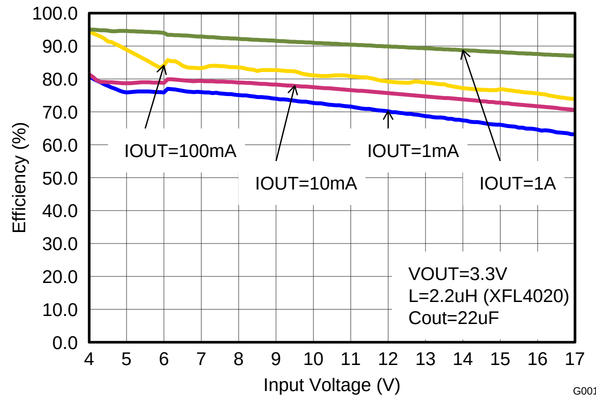

Figure 12. Efficiency With 2.5 MHz, Vout = 3.3 V

EFFICIENCY
vs
OUTPUT CURRENT

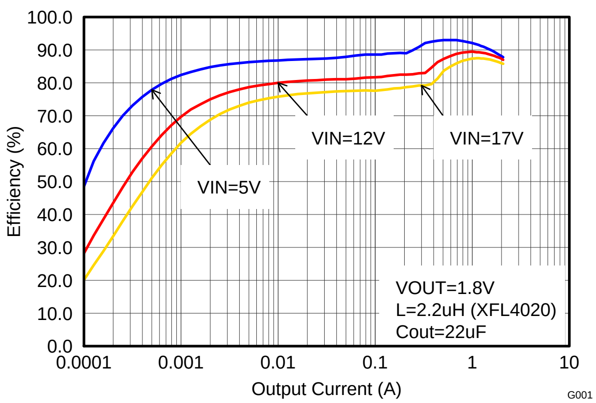

Figure 13. Efficiency With 1.25 MHz, Vout = 1.8 V

EFFICIENCY
vs
INPUT VOLTAGE

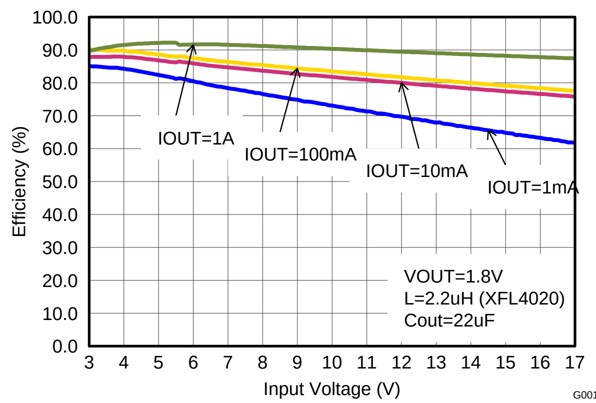

Figure 14. Efficiency With 1.25 MHz, Vout = 1.8 V

EFFICIENCY
vs
OUTPUT CURRENT

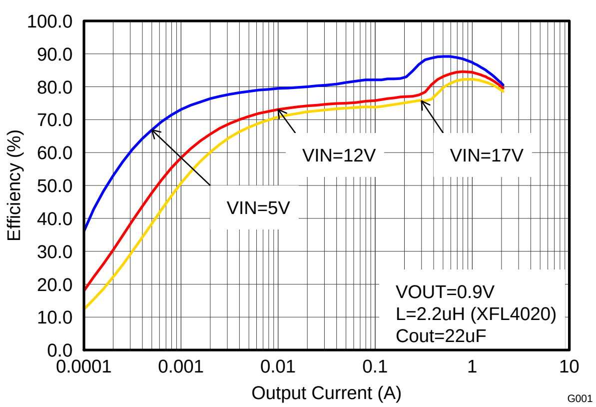

Figure 15. Efficiency With 1.25 MHz, Vout = 0.9 V

EFFICIENCY
vs
INPUT VOLTAGE

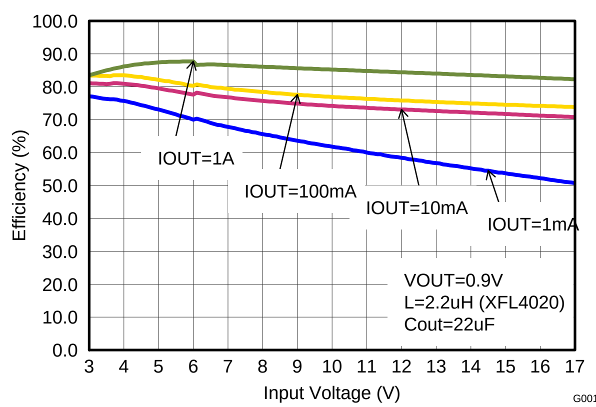

Figure 16. Efficiency With 1.25 MHz, Vout = 0.9 V

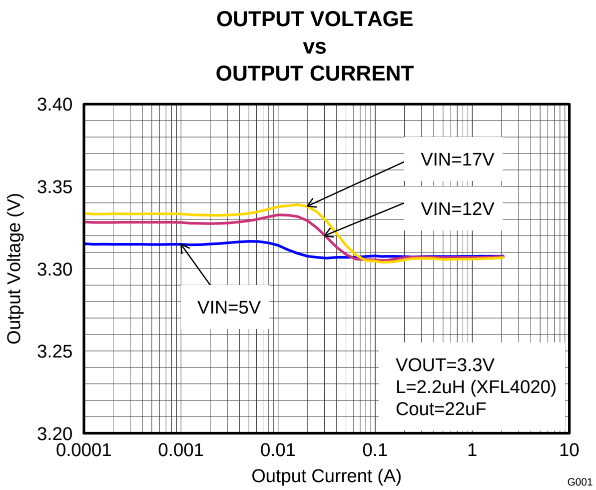

Figure 17. Output Voltage Accuracy (Load Regulation)

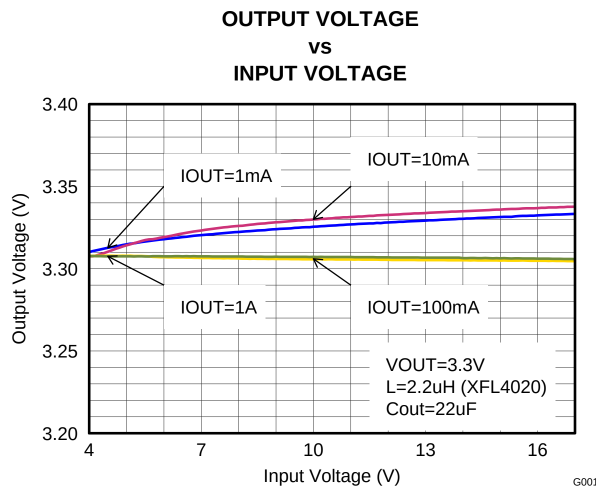

Figure 18. Output Voltage Accuracy (Line Regulation)

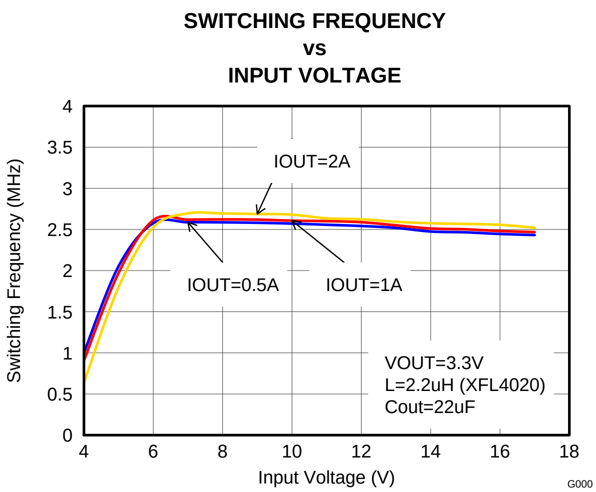

Figure 19. Switching Frequency

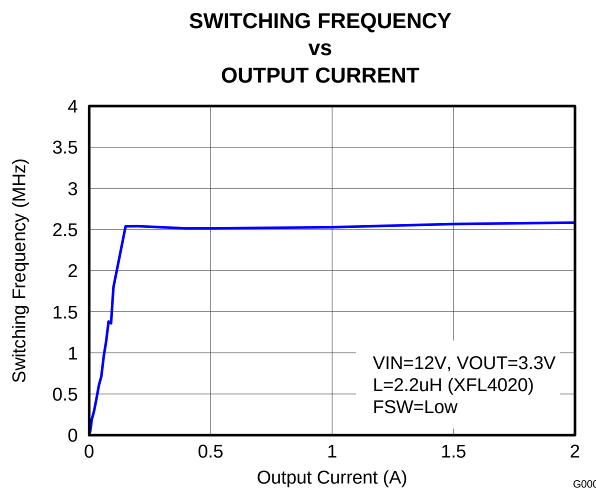

Figure 20. Switching Frequency

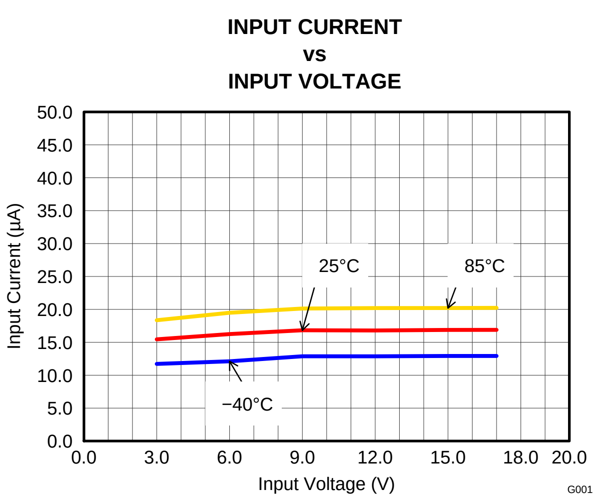

Figure 21. Quiescent Current

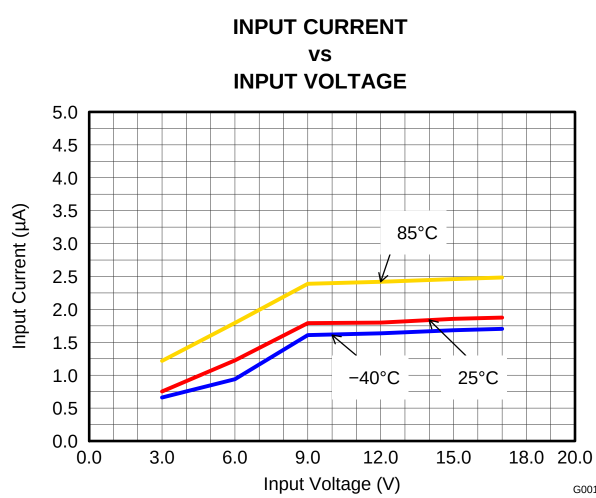

Figure 22. Shutdown Current

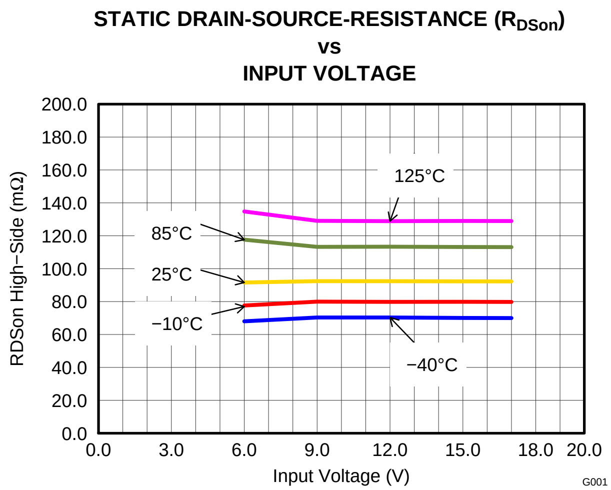

Figure 23. High-Side Switch Resistance

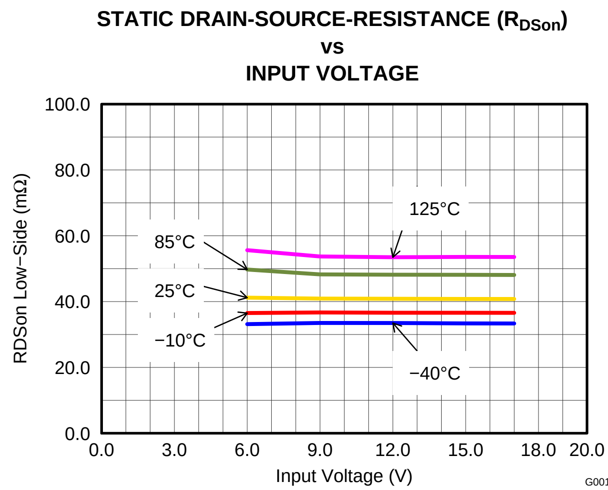

Figure 24. Low-Side Switch Resistance

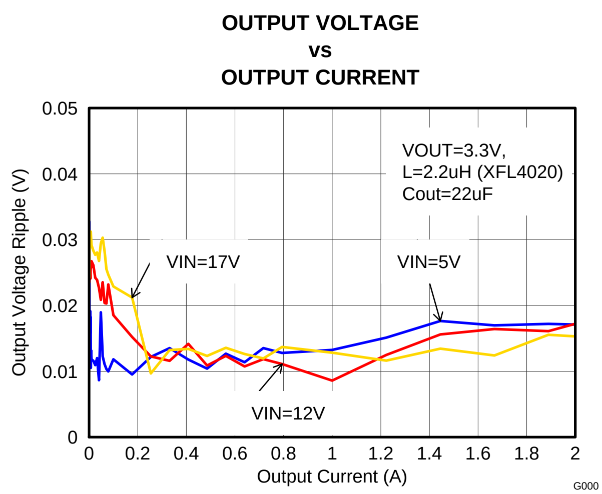

Figure 25. Output Voltage Ripple

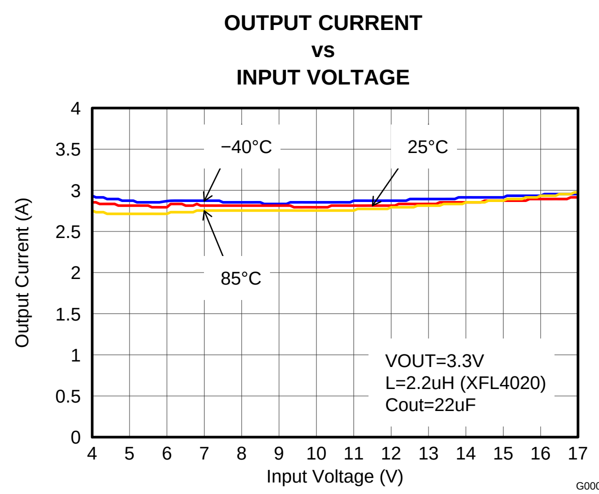

Figure 26. Maximum Output Current

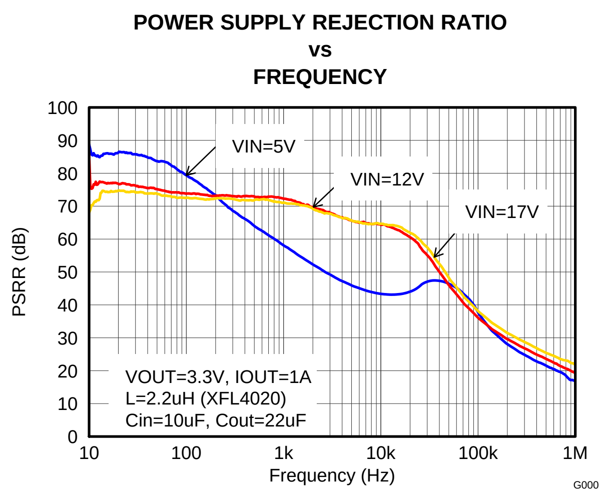

Figure 27. Power-Supply Rejection Ratio, f_{SW} = 2.5 MHz

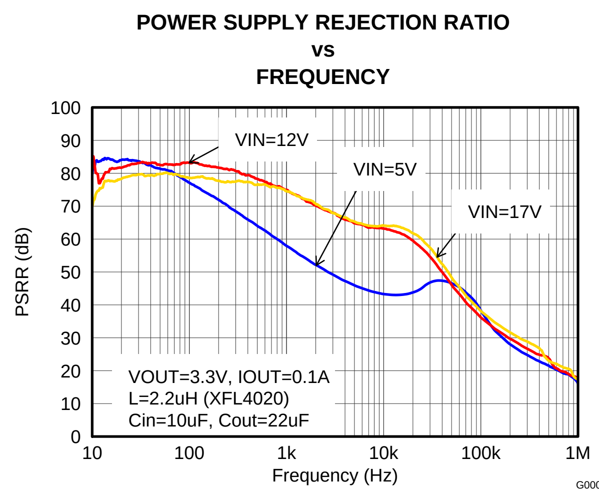

Figure 28. Power-Supply Rejection Ratio, f_{SW} = 2.5 MHz

OUTPUT VOLTAGE
vs
TIME

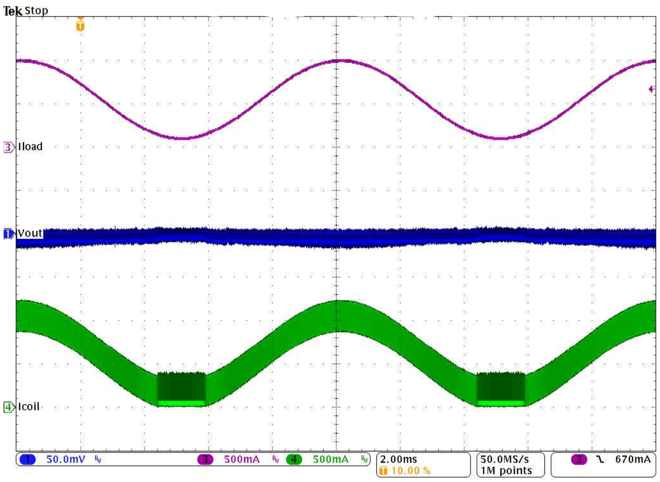

Figure 29. PWM-PSM-Transition (V_{IN}=12 V, V_{OUT} = 3.3 V With 50 mV/div)

OUTPUT VOLTAGE
vs
TIME

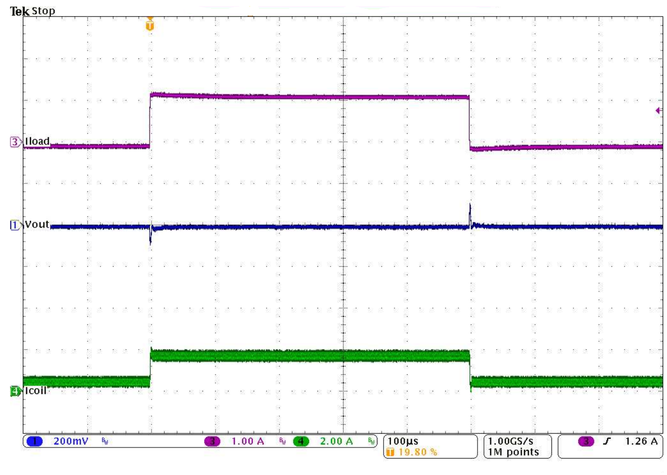

Figure 30. Load Transient Response (I_{OUT}= 0.5 to 2 to 0.5 A, V_{IN} = 12 V, V_{OUT} = 3.3 V)

OUTPUT VOLTAGE
vs
TIME

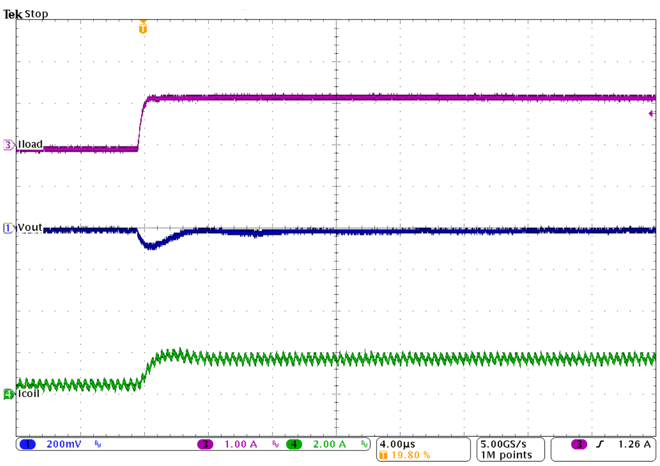

Figure 31. Line Transient Response of Figure 30, Rising Edge

OUTPUT VOLTAGE
vs
TIME

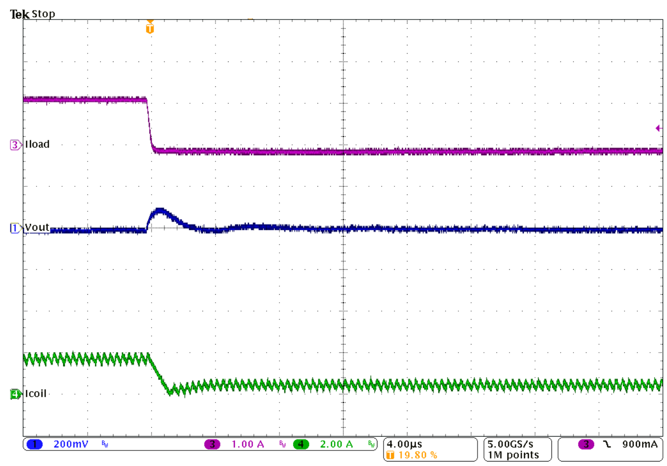

Figure 32. Line Transient Response of Figure 30, Falling Edge

OUTPUT VOLTAGE
vs
TIME

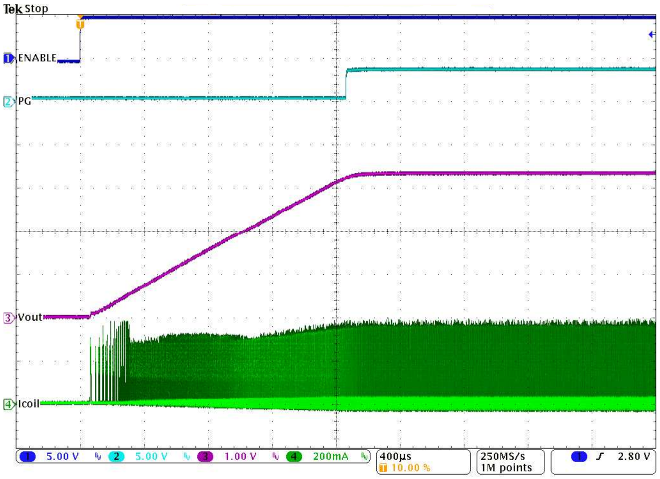

Figure 33. Start-Up Into 100 mA (VIN = 12 V, VOUT = 3.3 V)

OUTPUT VOLTAGE
vs
TIME

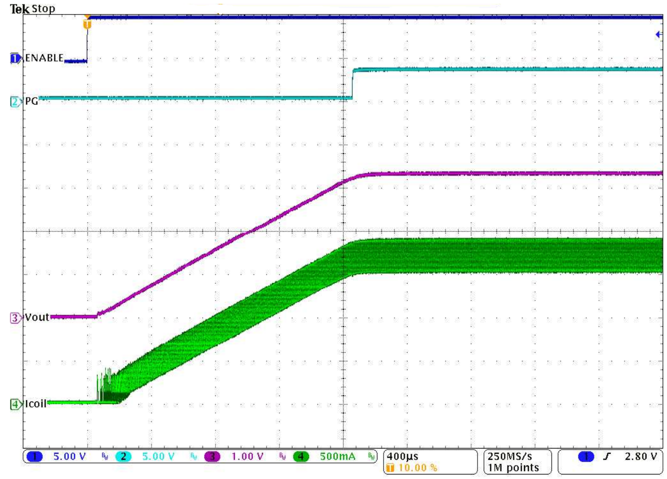

Figure 34. Start-Up into 2 A (VIN = 12 V, VOUT = 3.3 V)

PWM SIGNALS
vs
TIME

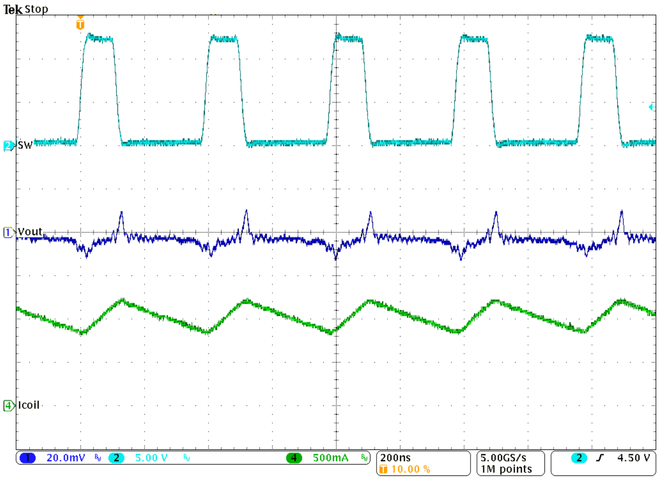

Figure 35. Typical Operation in PWM Mode (I_{OUT} = 1 A)

POWER SAVE MODE SIGNALS
vs
TIME

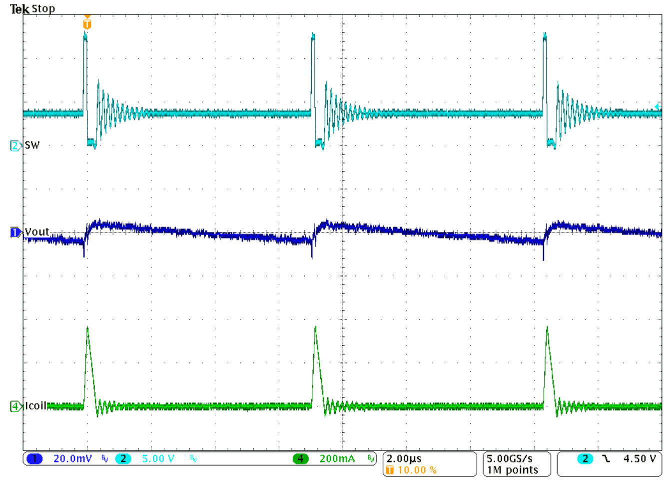

Figure 36. Typical Operation in Power-Save Mode (I_{OUT} = 10 mA)

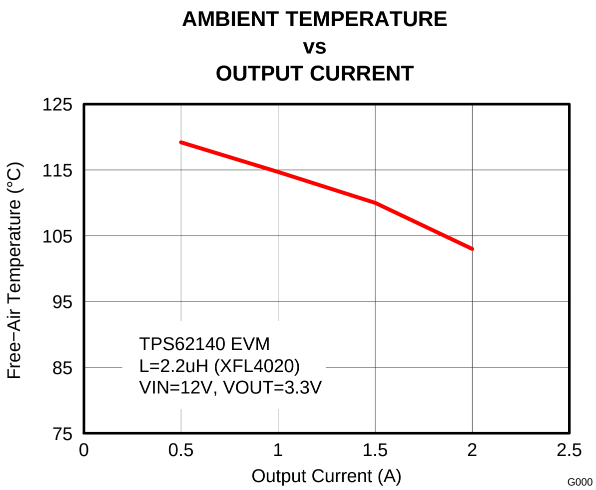

Figure 37. Maximum Ambient Temperature (f_{SW} = 2.5 MHz)

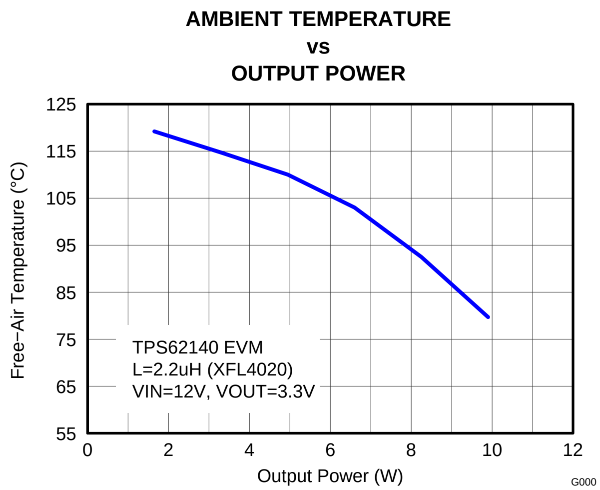

Figure 38. Maximum Ambient Temperature (f_{SW} = 2.5 MHz)

DETAILED DESCRIPTION

Device Operation

The TPS6214X synchronous switched-mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power-Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage-mode and current-mode control including an ac loop directly associated with the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate dc load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

The DCS-Control topology supports pulse-width modulation (PWM) mode for medium and heavy load conditions and a power-save mode at light loads. During PWM, it operates at its nominal switching frequency in continuous-conduction mode. This frequency is typically about 2.5 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power-save mode to sustain high efficiency down to very light loads. In power-save mode, the switching frequency decreases linearly with the load current. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to power-save mode is seamless without effects on the output voltage.

Fixed output-voltage versions provide the smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 2A.

The TPS6214X family offers both excellent dc voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

Pulse-Width Modulation (PWM) Operation

The TPS6214X operates with pulse-width modulation in continuous-conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT} and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor ripple current. To maintain high efficiency at light loads, the device enters power-save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor ripple current.

Power-Save Mode Operation

The TPS6214X enters its built-in power-save mode seamlessly if the load current decreases. This secures a high efficiency in light-load operation. The device remains in power-save mode as long as the inductor current is discontinuous.

In power-save mode, the switching frequency decreases linearly with the load current, maintaining high efficiency. The transition into and out of power-save mode happens within the entire regulation scheme and is seamless in both directions.

TPS6214X includes a fixed-on-time circuit. The on-time, in steady-state operation, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \tag{1}$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. Using t_{ON}, the typical peak inductor current in power-save mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above VOUT, the TPS6214X does not enter power-save mode, regardless of the load current. The device maintains output regulation in PWM mode.

100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = Vout/Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty-cycle operation, turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input-to-output voltage differences, e.g., for longest operation time of battery-powered applications. In 100% duty-cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right) \tag{3}$$

where

I_{OUT} is the output current.
$R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET.
R_L is the dc resistance of the inductor used.

Enable / Shutdown (EN)

When the enable pin (EN) is set High, the device starts operation.

Shutdown is forced if EN is pulled Low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. An internal pulldown resistor of about 400 kΩ is connected and keeps EN logic Low if the pin is floating. It is disconnected if the pin is High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

Soft-Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and ensures a controlled output-voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs, and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 33 and Figure 34 for typical start-up operation.

The slope can be controlled by an external capacitor connected to the SS/TR pin. Connecting SS/TR directly to AVIN provides fastest start-up behavior. The TPS6214X can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device internal ramp sets an output voltage above the pre-bias voltage. As long as the output is below about 0.5 V, a reduced current limit of typically 1.6 A is set internally. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage follows this voltage in both directions, up and down (see APPLICATION INFORMATION).

Current Limit and Short Circuit Protection

The TPS6214X devices are protected against heavy load and short-circuit events. If a short circuit is detected (VOUT drops below 0.5 V), the current limit is reduced to 1.6 A, typically. If the output voltage rises above 0.5 V, the device runs in normal operation again. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot-through current, the low-side FET is switched on to sink the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side current-limit threshold.

The output current of the device is limited by the current limit (see ELECTRICAL CHARACTERISTICS). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \tag{4}$$

where

I_{LIMF} is the static current limit, specified in the ELECTRICAL CHARACTERISTICS
L is the inductor value
V_L is the voltage across the inductor (V_{IN} – V_{OUT})
t_{PD} is the internal propagation delay

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \tag{5}$$

Power Good (PG)

The TPS6214X has a built-in power-good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic-low level. It is high-impedance when the device is turned off due to EN, UVLO, or thermal shutdown.

Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6214X devices can be increased by 5% above the nominal voltage by setting the DEF pin to High[(1)]. When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6214X can be found in SLVA489. A pulldown resistor of about 400 kΩ is internally connected to the pin, to ensure a proper logic level if the pin is high-impedance or floating. The resistor is disconnected if the pin is High.

Frequency Selection (FSW)

To get high power density with a very small solution size, a high switching frequency allows the use of small external components for the output filter. However, switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High[(1)] . Pull FSW to Low for high-frequency operation (2.5 MHz typ.). Running with lower frequency, a higher efficiency, but also a higher output-voltage ripple, is achieved. To get low ripple and full output current at the lower switching frequency, it is recommended to use an inductor of 3.3 µH. The switching frequency can be changed during operation, if needed. A pulldown resistor of about 400 kΩ is internally connected to the pin to ensure a proper logic level if the pin is high-impedance or floating. The resistor is disconnected if the pin is High.

Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents incorrect operation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes high-impedance. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

(1) Maximum allowed voltage is 7 V. Therefore it is recommended to connect it to VOUT, not VIN.

APPLICATION INFORMATION

The following information is intended to be a guideline through the individual power-supply design process.

Programming the Output Voltage

While the output voltage of the TPS62140 is adjustable, the TPS62141/2/3 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 (see Figure 4). It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most-robust design. For applications requiring lowest current consumption, the use of fixed output-voltage versions is recommended.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{6}$$

In case the FB pin is opened, the device clamps the output voltage at the VOS pin internally to about 7.4 V.

External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6214X is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered in conjunction, creating a double pole, responsible for the corner frequency of the converter (see Output Filter and Loop Stabilitysection). Table 1 can be used to simplify the output filter component selection.

Table 1. Recommended LC Output Filter Combinations(1)

	4.7 µF	**10 µF**	**22 µF**	**47 µF**	**100 µF**	**200 µF**	**400 µF**
0.47 µH							
1 µH			√	√	√	√	
2.2 µH		√	√(2)	√	√	√	
3.3 µH		√	√	√	√		
4.7 µH							

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

TPS6214X can be run with an inductor as low as 1 µH or 2.2 µH. FSW should be set Low in this case. However, for applications running with the low-frequency setting (FSW = High) or with low input voltages, 3.3 µH is recommended. More detailed information on further LC combinations can be found in SLVA463.

Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the inductor selected must be rated for appropriate saturation current and dc resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right) \quad (8)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- L(min) is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency

Calculating the maximum inductor current using the actual operating conditions gives the minimum required inductor saturation current. It is recommended to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6214X and are recommended for use:

Table 2. List of Inductors

Type	Inductance [µH]	Current [A][1]	Dimensions [L x B x H] mm	MANUFACTURER
XFL4020-222ME_	2.2 µH, ±20%	3.5	4 x 4 x 2.1	Coilcraft
XFL4020-332ME_	3.3 µH, ±20%	2.9	4 x 4 x 2.1	Coilcraft
IHPL1212BZ-11	2.2 µH, ±20%	3.0	3 x 3.6 x 2	Vishay
IHLP1616AB-11	2.2 µH, ±20%	2.75	4.05 x 4.45 x 1.2	Vishay
DEM4518C 1235AS-H-3R3M	3.3 µH, ±20%	2.5	4.5 x 4.7 x 1.9	Toko

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

The inductor value also determines the load current at which the power-save mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L \quad (9)$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

Capacitor Selection

Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6214X allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output-voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value can have some advantages, like smaller voltage ripple and a tighter dc output accuracy in power-save mode (see SLVA463).

Note: In power-save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

Input Capacitor

For most applications, 10 μF is sufficient and is recommended, though a larger value reduces input-current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low-ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between PVIN and PGND as close as possible to those pins. Even though AVIN and PVIN must be supplied from the same input source, it is recommended to place a capacitance of 0.1 uF from AVIN to AGND, to avoid potential noise coupling.

Soft-Start Capacitor

A capacitance connected between the SS/TR pin and AGND allows a user-programmable start-up slope of the output voltage. A constant-current source provides 2.5 μA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu A}{1.25V} \quad [F] \tag{10}$$

where

C_{SS} is the capacitance (F) required at the SS/TR pin and
t_{SS} is the desired soft-start ramp time (s).

NOTE

DC bias effect: High-capacitance ceramic capacitors have a dc bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in Equation 11 and shown in Figure 39.

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{11}$$

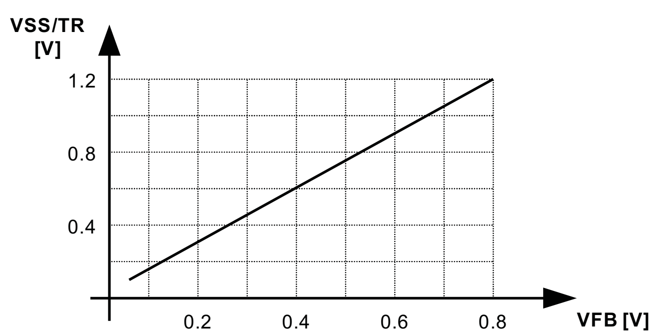

Figure 39. Voltage Tracking Relationship

This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. Figure 40 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

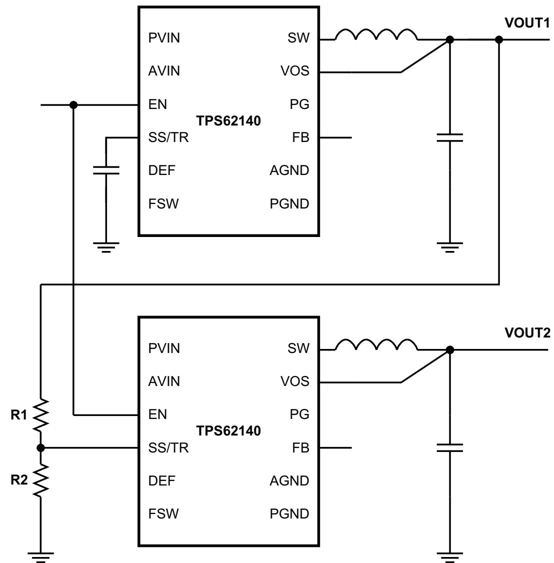

Figure 40. Sequence for Ratiometric and Simultaneous Startup

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. A ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 10 calculates the soft-start time, though the SS/TR current must be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy may have a wider tolerance than specified.

Output Filter and Loop Stability

The devices of the TPS6214X family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 1 and are recommended for use. Different values may work, but care must be taken on the loop stability, which is affected. More information including a detailed L-C stability matrix can be found in SLVA463.

The TPS6214X devices, both fixed and adjustable versions, include an internal 25 pF feed-forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equations Equation 13 and Equation 14:

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25\,pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25\,pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

Though the TPS6214X devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power-save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability vs transient response can be found in SLVA289 and SLVA466.

Layout Considerations

A proper layout is critical for the operation of a switched-mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6214X demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

Provide low-inductance and -resistance paths for loops with high di/dt. Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low-capacitance paths (with respect to all other nodes) for wires with high dv/dt. Therefore, the input and output capacitance should be placed as close as possible to the IC pins, and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Also, sensitive nodes like FB and VOS should be connected with short wires, not near high-dv/dt signals (e.g., SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission (e.g., feedback divider, SS/TR capacitor) should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the PVIN and PGND pins of the IC. The connections should be made with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC PGND pins, avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor, minimizing the loop area between the SW pin, inductor, output capacitor, and PGND pin. The feedback resistors, R_1 and R_2, should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and even more to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load. The capacitor on the SS/TR pin should be kept close to the IC, and its return should be connected to AGND.

See Figure 41 for the recommended layout of the TPS6214X. AGND is connected to the exposed thermal pad, which is also connected to PGND and internal metal layers to get best thermal performance. The regulation loop is closed from COUT directly to AGND with vias down to the AGND bottom layer. More detailed information can be found in the EVM user's guide, SLVU437.

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the exposed thermal pad can be connected to a floating circuit board trace, the device has better thermal performance if it is connected to a larger ground plane. The exposed thermal pad is electrically connected to AGND.

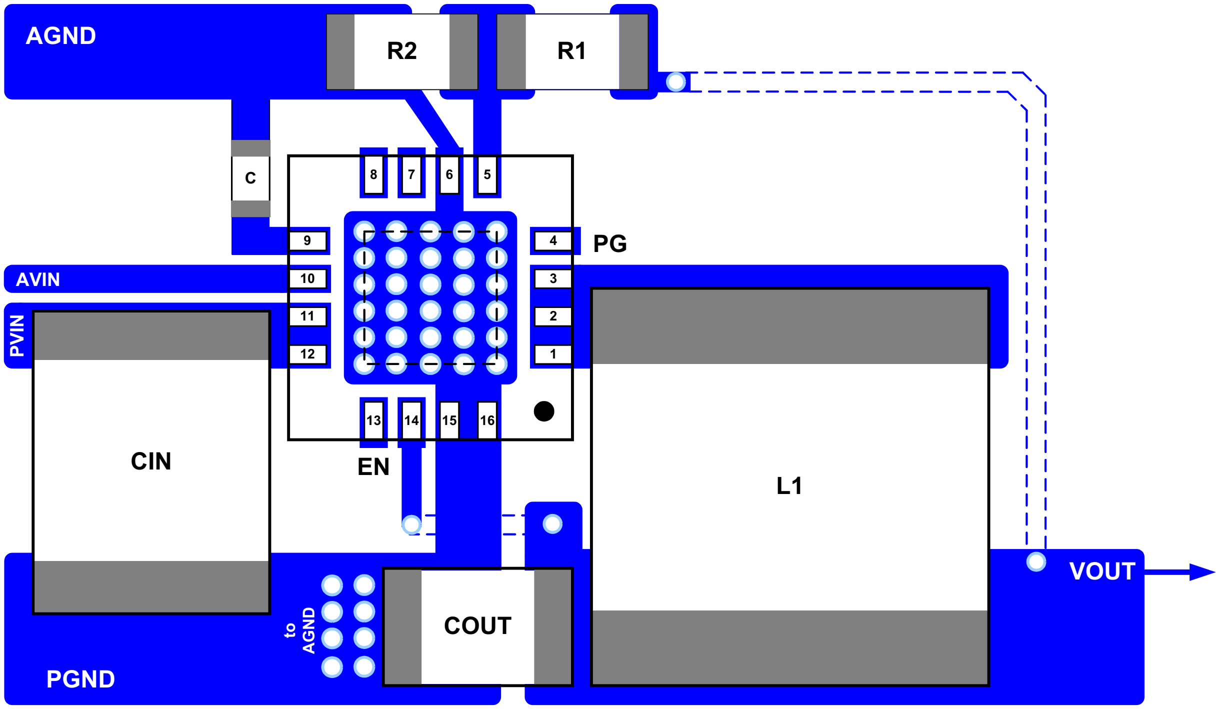

Figure 41. Layout Example

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS6214X is designed for a maximum operating junction temperature (T_J) of 125°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get improved thermal behavior, it is recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short-circuit or overload conditions are present, the device is protected by limiting internal power dissipation. Experimental data, taken from the TPS62140 EVM, shows the maximum ambient temperature (without additional cooling like airflow or heat sink), that can be allowed to limit the junction temperature to at most 125°C (see Figure 37).

Application Example As Power LED Supply

The TPS62140 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Because this pin provides 2.5 μA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62140. Figure 42 shows an application circuit, tested with analog dimming:

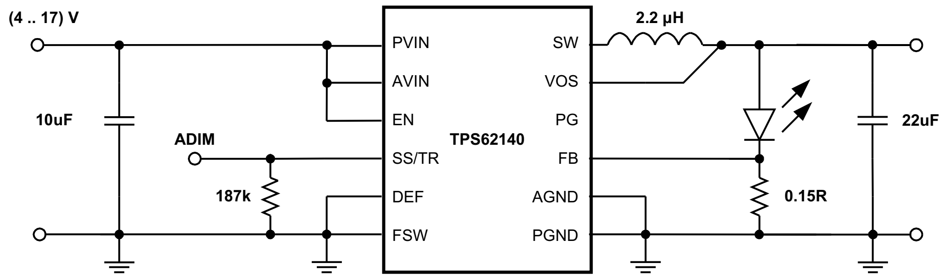

Figure 42. Single Power LED Supply

The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu A \cdot R_{SS/TR} \tag{15}$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage must be rated according to the forward voltage needed by the LED used. More information is available in the application note SLVA451.

Typical Applications

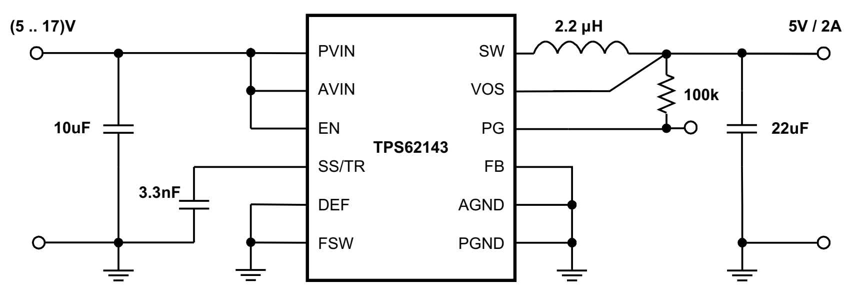

Figure 43. 5-V/2-A Power Supply

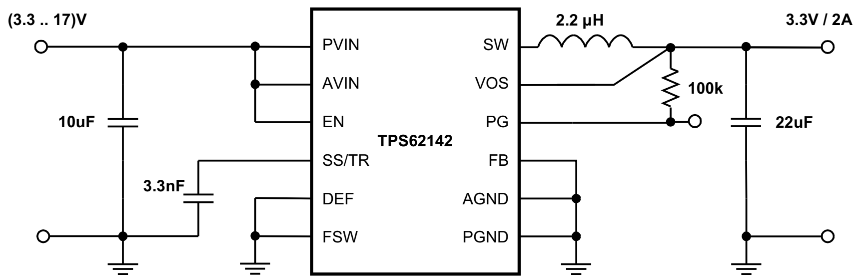

Figure 44. 3.3-V/2-A Power Supply

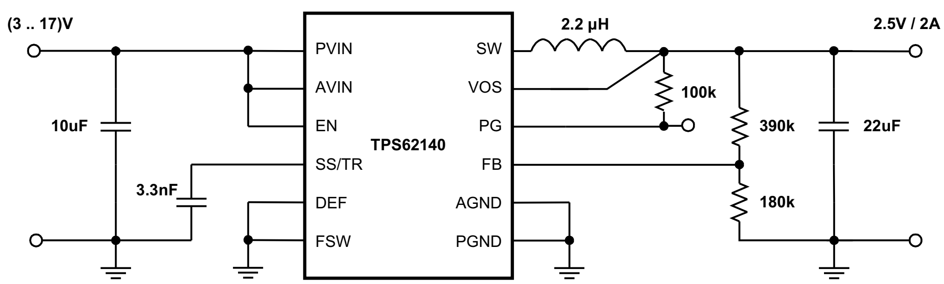

Figure 45. 2.5-V/2-A Power Supply

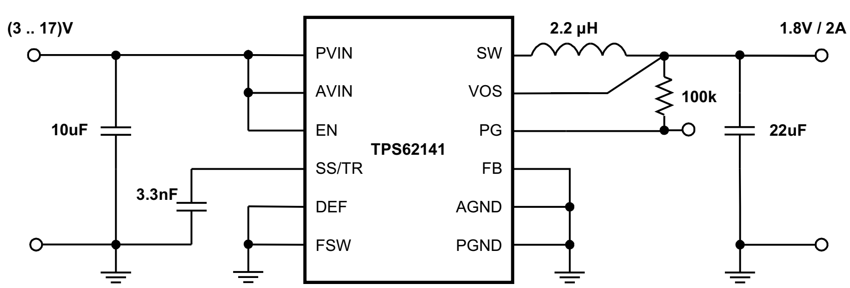

Figure 46. 1.8-V/2-A Power Supply

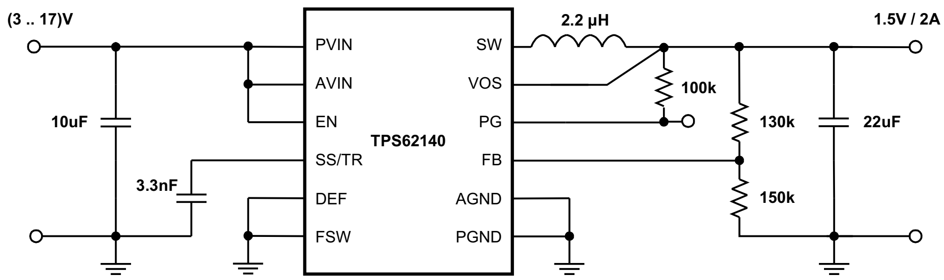

Figure 47. 1.5-V/2-A Power Supply

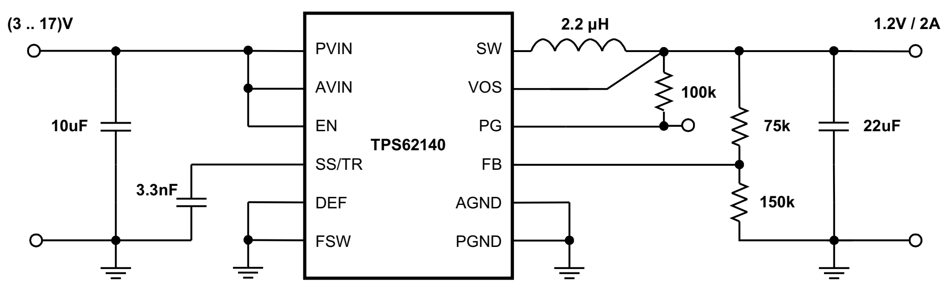

Figure 48. 1.2-V/2-A Power Supply

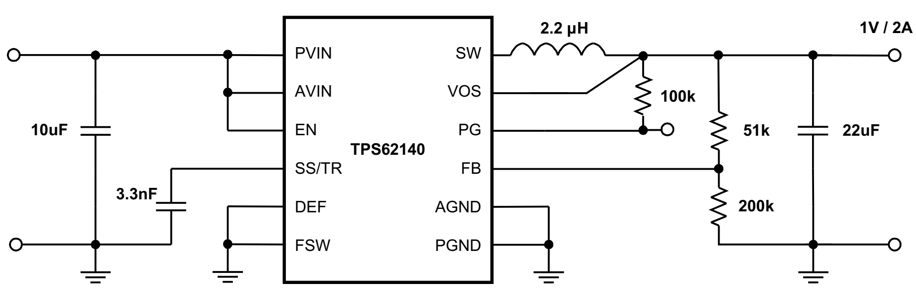

Figure 49. 1-V/2-A Power Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS62140RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62140RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62141RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62141RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62142RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62142RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62143RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS62143RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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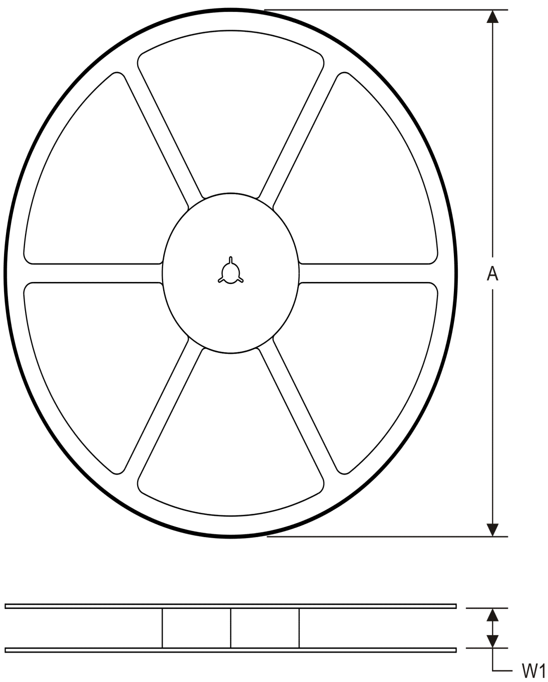
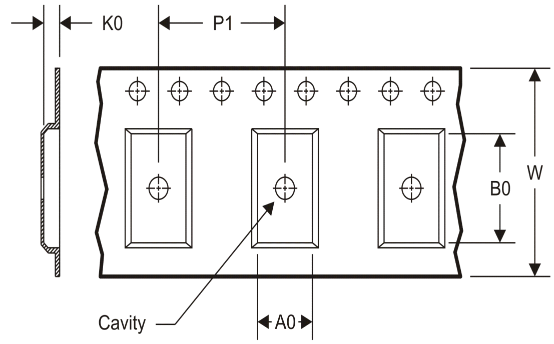
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



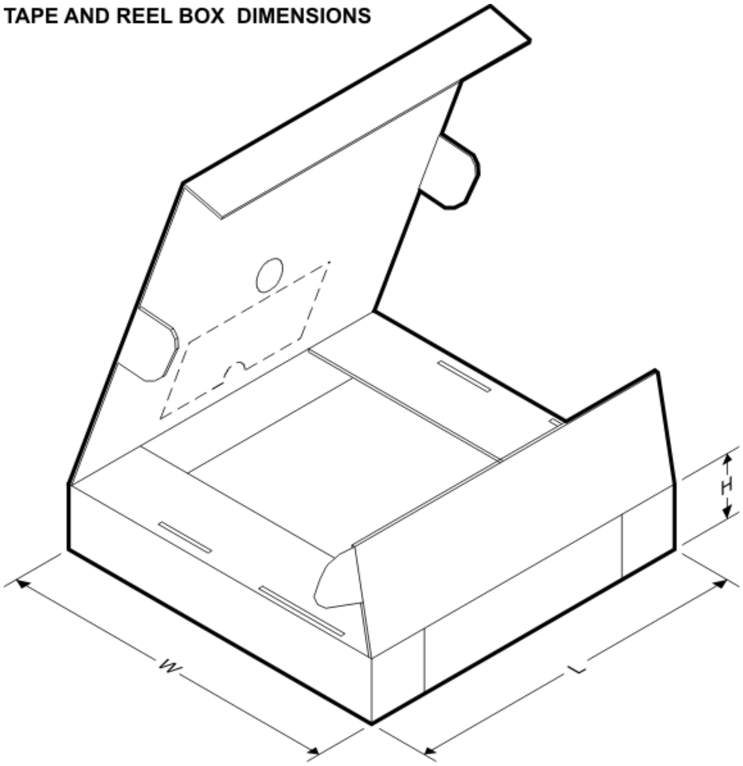
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62140RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62140RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62141RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62142RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62143RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

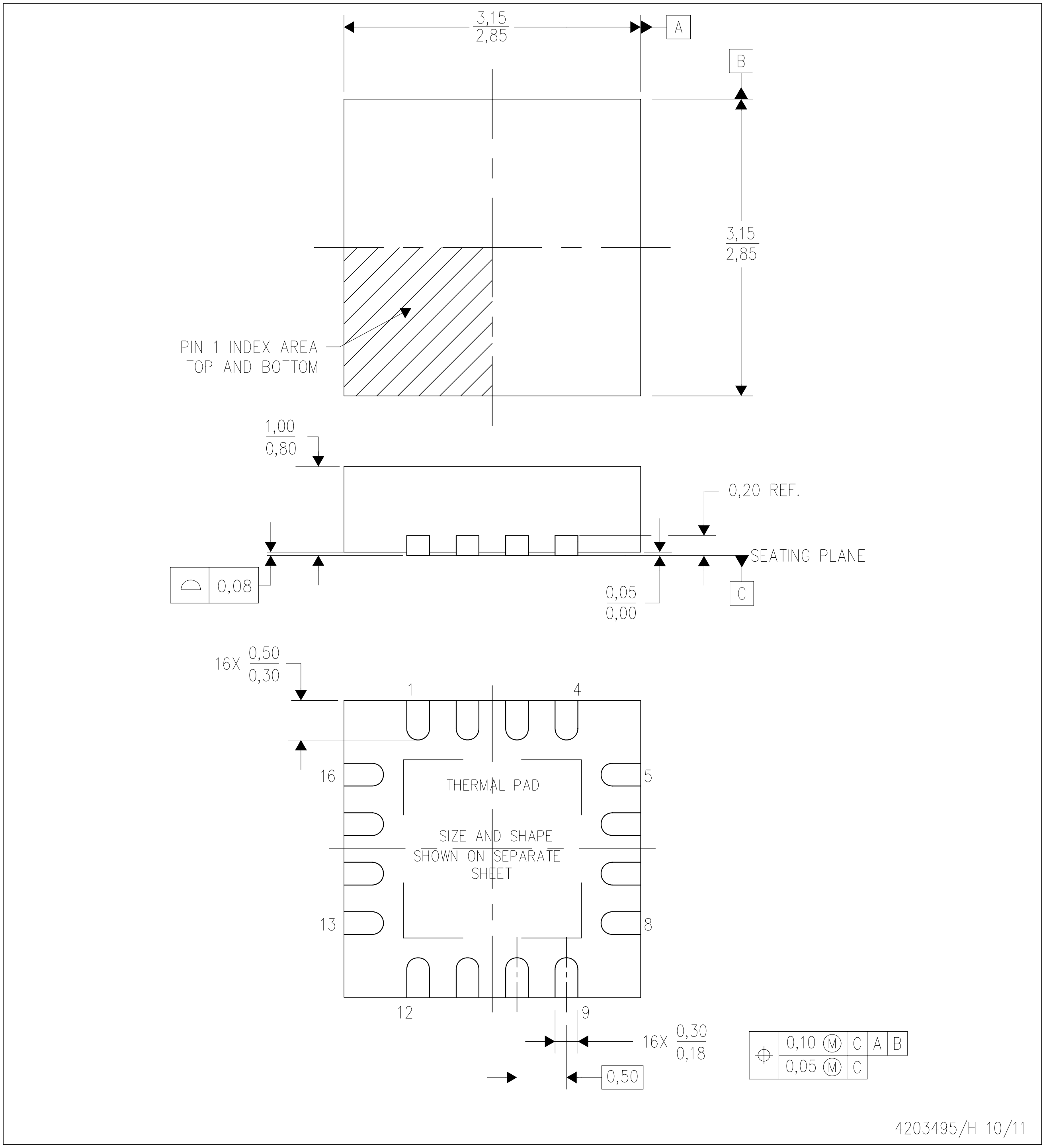
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62140RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62140RGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62141RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62141RGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62142RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62142RGTT	QFN	RGT	16	250	552.0	185.0	36.0
TPS62143RGTR	QFN	RGT	16	3000	552.0	367.0	36.0
TPS62143RGTT	QFN	RGT	16	250	552.0	185.0	36.0

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No–leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–220.

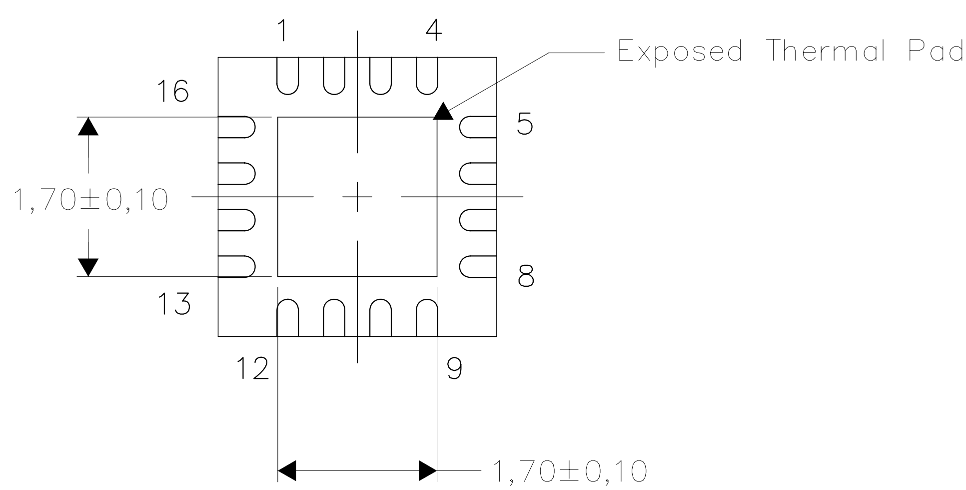
RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



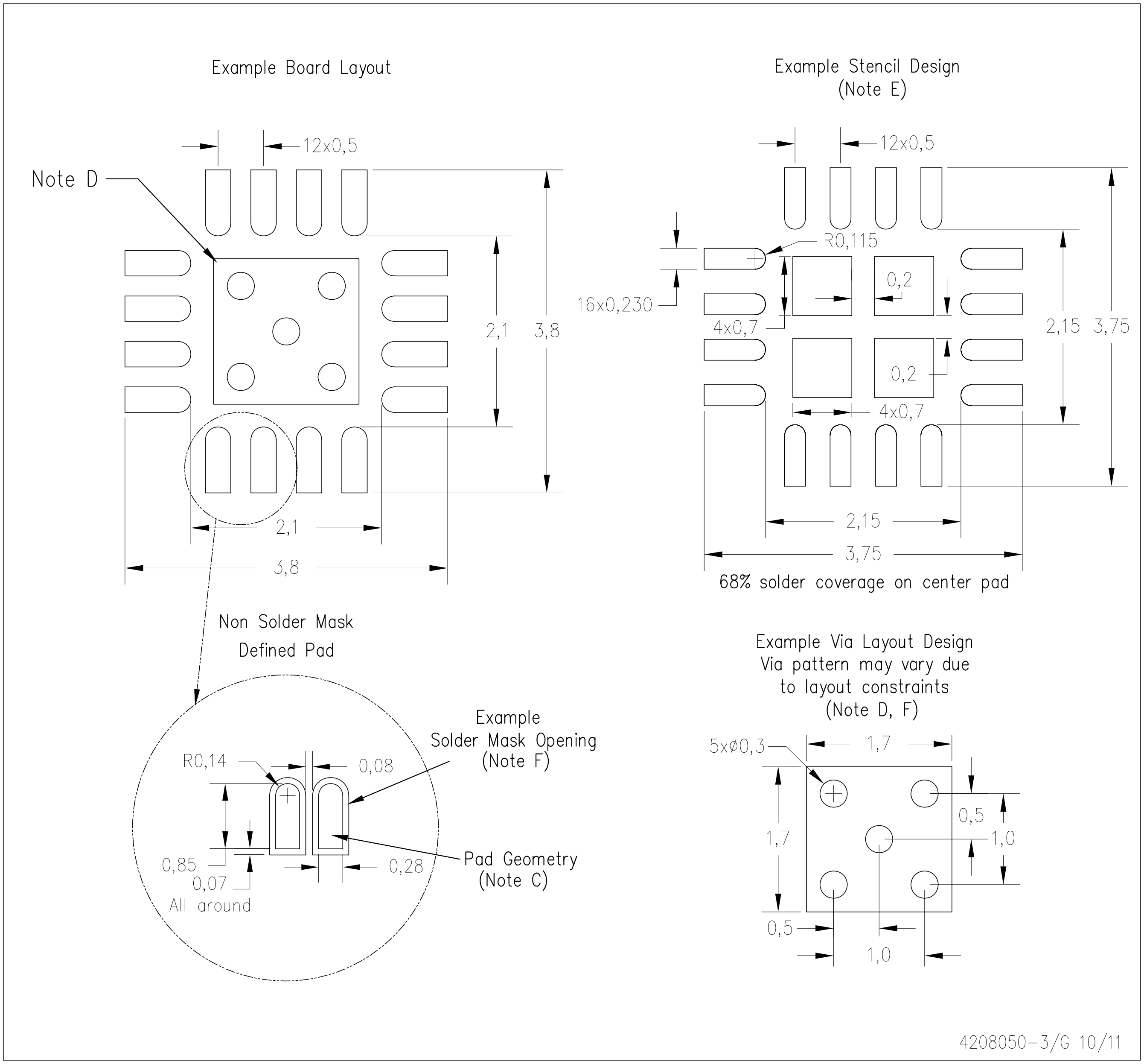
Bottom View

Exposed Thermal Pad Dimensions

4206349-4/Q 10/11

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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