Dual, Interleaved, Step-Down DC-to-DC Controller with Tracking

ADP1823

FEATURES

- Fixed-frequency operation: 300 kHz, 600 kHz, or synchronized operation up to 1 MHz
- Supply input range: 2.9 V to 20 V
- Interleaved operation results in smaller, low cost input capacitor
- All-N-channel MOSFET design for low cost
- ±0.85% accuracy at 0°C to 70°C
- Soft start, thermal overload, current-limit protection
- 10 µA shutdown supply current
- Internal linear regulator
- Lossless R_{DSON} current-limit sensing
- Reverse current protection during soft start for handling precharged outputs
- Independent Power OK outputs
- Voltage tracking for sequencing or DDR termination
- Available in 5 mm × 5 mm, 32-lead LFCSP

APPLICATIONS

- Telecommunications and networking systems
- Medical imaging systems
- Base station power
- Set-top boxes
- Printers
- DDR termination

TYPICAL APPLICATION CIRCUIT

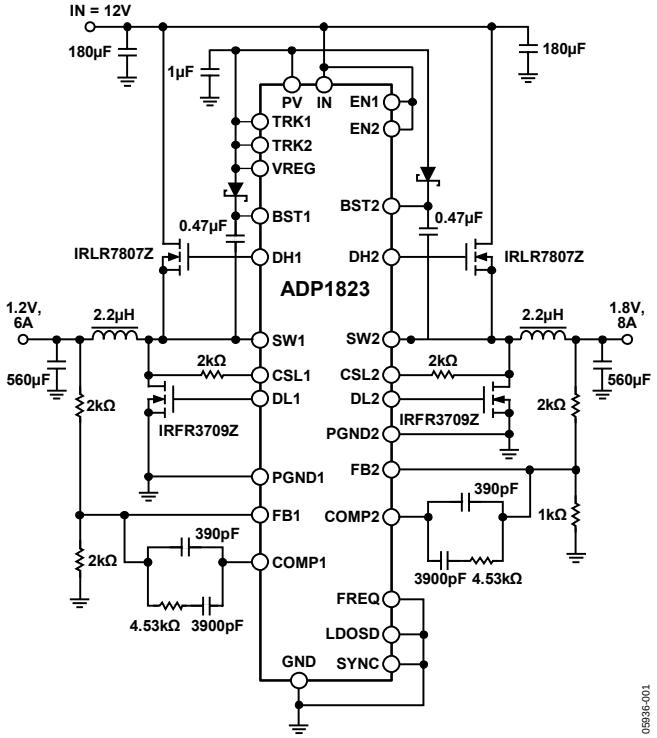

Figure 1. Typical Application Circuit

GENERAL DESCRIPTION

The ADP1823 is a versatile, dual, interleaved, synchronous PWM buck controller that generates two independent output rails from an input of 2.9 V to 20 V. Each controller can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators. The two channels operate 180° out of phase, reducing stress on the input capacitor and allowing smaller, low cost components. The ADP1823 is ideal for a wide range of high power applications, such as DSP and processor core I/O power, and general-purpose power in telecommunications, medical imaging, PC, gaming, and industrial applications.

The ADP1823 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise-sensitive applications, it can also be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1 MHz. The ADP1823 includes soft start protection to prevent inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

For applications requiring power supply sequencing, the ADP1823 also provides tracking inputs that allow the output voltages to track during startup, shutdown, and faults. This feature can also be used to implement DDR memory bus termination.

The ADP1823 is specified over the −40°C to +85°C ambient temperature range, and is available in a 32-lead LFCSP package.

Rev. A

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4/06—Revision 0: Initial Version

SPECIFICATIONS

VIN = 12 V, EN = FREQ = PV = VREG = 5 V, SYNC = GND, T_J = −40°C to +125°C, unless otherwise specified. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC). Typical values are at T_A = 25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
IN Input Voltage	PV = VREG (using internal regulator)	5.5		20	V
	IN = PV = VREG (not using internal regulator)	2.9		5.5	V
IN Quiescent Current	Not switching, I_{VREG} = 0 mA		1.5	3	mA
IN Shutdown Current	EN1 = EN2 = GND		10	20	µA
VREG Undervoltage Lockout Threshold	VREG rising	2.4	2.7	2.9	V
VREG Undervoltage Lockout Hysteresis			0.125		V
ERROR AMPLIFER					
FB1, FB2 Regulation Voltage	T_A = 25°C, TRK1, TRK2 > 700 mV	597	600	603	mV
	T_J = 0°C to 85°C, TRK1, TRK2 > 700 mV	591		609	mV
	T_J = −40°C to +125°C, TRK1, TRK2 > 700 mV	588		612	mV
	T_J = 0°C to 70°C, TRK1, TRK2 > 700 mV	595		605	mV
FB1, FB2 Input Bias Current				100	nA
Open-Loop Voltage Gain			70		dB
Gain-Bandwidth Product			20		MHz
COMP1, COMP2 Sink Current			600		µA
COMP1, COMP2 Source Current			120		µA
COMP1, COMP2 Clamp High Voltage			2.4		V
COMP1, COMP2 Clamp Low Voltage			0.75		V
LINEAR REGULATOR					
VREG Output Voltage	T_A = 25°C, I_{VREG} = 20 mA	4.85	5.0	5.15	V
	VIN = 7 V to 20 V, I_{VREG} = 0 mA to 100 mA, T_A = −40°C to +85°C	4.75	5.0	5.25	V
VREG Load Regulation	I_{VREG} = 0 mA to 100 mA, VIN = 12 V		−40		mV
VREG Line Regulation	VIN = 7 V to 20 V, I_{VREG} = 20 mA		1		mV
VREG Current Limit	VREG = 4 V		220		mA
VREG Short-Circuit Current	VREG < 0.5 V	100	140	200	mA
IN to VREG Dropout Voltage	I_{VREG} = 100 mA		0.7	1.4	V
VREG Minimum Output Capacitance		1			µF
PWM CONTROLLER					
PWM Ramp Voltage Peak	SYNC = GND		1.3		V
DH1, DH2 Maximum Duty Cycle	FREQ = GND (300 kHz)	85	90		%
DH1, DH2 Minimum Duty Cycle	FREQ = GND (300 kHz)		1	3	%
SOFT START					
SS1, SS2 Pull-Up Resistance	SS1, SS2 = GND		90		kΩ
SS1, SS2 Pull-Down Resistance	SS1, SS2 = 0.6 V		6		kΩ
SS1, SS2 to FB1, FB2 Offset Voltage	SS1, SS2 = 0 mV to 500 mV		−45		mV
SS1, SS2 Pull-Up Voltage			0.8		V
TRACKING					
TRK1, TRK2 Common-Mode Input Voltage Range		0		600	mV
TRK1, TRK2 to FB1, FB2 Offset Voltage	TRK1, TRK2 = 0 mV to 500 mV	−5		+5	mV
TRK1, TRK2 Input Bias Current				100	nA

Parameter	Conditions	Min	Typ	Max	Unit
OSCILLATOR					
Oscillator Frequency	SYNC = FREQ = GND ($f_{SW} = f_{OSC}$)	240	300	370	kHz
	SYNC = GND, FREQ = VREG ($f_{SW} = f_{OSC}$)	480	600	720	kHz
SYNC Synchronization Range	FREQ = GND, SYNC = 600 kHz to 1.2 MHz[1] ($f_{SW} = f_{SYNC}/2$)	300		600	kHz
	FREQ = VREG, SYNC = 1.2 MHz to 2 MHz[1] ($f_{SW} = f_{SYNC}/2$)	600		1000	kHz
SYNC Minimum Input Pulse Width				200	ns
CURRENT SENSE					
CSL1, CSL2 Threshold Voltage	Relative to PGND	−30	0	+30	mV
CSL1, CSL2 Output Current	CSL1, CSL2 = PGND	44	50	56	µA
Current Sense Blanking Period			100		ns
GATE DRIVERS					
DH1, DH2 Rise Time	C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		15		ns
DH1, DH2 Fall Time	C_{DH} = 3 nF, $V_{BST} - V_{SW}$ = 5 V		10		ns
DL1, DL2 Rise Time	C_{DL} = 3 nF		15		ns
DL1, DL2 Fall Time	C_{DL} = 3 nF		10		ns
DH to DL, DL to DH Dead Time			40		ns
LOGIC THRESHOLDS					
SYNC, FREQ, LDOSD Input High Voltage		2.2			V
SYNC, FREQ, LDOSD Input Low Voltage				0.4	V
SYNC, FREQ Input Leakage Current	SYNC, FREQ = 0 V to 5.5 V			1	µA
LDOSD Pull-Down Resistance			100		kΩ
EN1, EN2 Input High Voltage	IN = 2.9 V to 20 V	2.0			V
EN1, EN2 Input Low Voltage	IN = 2.9 V to 20 V			0.8	V
EN1, EN2 Current Source	EN1, EN2 = 0 V to 3.0 V	−0.3	−0.6	−1.5	µA
EN1, EN2 Input Impedance to 5 V Zener	EN1, EN2 = 5.5 V to 20 V		100		kΩ
THERMAL SHUTDOWN					
Thermal Shutdown Threshold[2]			145		°C
Thermal Shutdown Hysteresis[2]			15		°C
POWER GOOD					
FB1, UV2 Overvoltage Threshold	V_{FB1}, V_{UV2} rising		750		mV
FB1, UV2 Overvoltage Hysteresis			50		mV
FB1, UV2 Undervoltage Threshold	V_{FB1}, V_{UV2} rising		550		mV
FB1, UV2 Undervoltage Hysteresis			50		mV
POK1, POK2 Propagation Delay			8		µs
POK1, POK2 Off Leakage Current	V_{POK1}, V_{POK2} = 5.5 V			1	µA
POK1, POK2 Output Low Voltage	I_{POK1}, I_{POK2} = 10 mA		150	500	mV
UV2 Input Bias Current			10	100	nA

[1] SYNC input frequency is 2× single channel switching frequency. The SYNC frequency is divided by 2 and the separate phases were used to clock the controllers.
[2] Guaranteed by design and not subject to production test.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN, EN1, EN2	−0.3 V to +20 V
BST1, BST2	−0.3 V to +30 V
BST1, BST2 to SW1, SW2	−0.3 V to +6 V
CSL1, CSL2	−1 V to +30 V
SW1, SW2	−2 V to +30 V
DH1	SW1 − 0.3 V to BST1 + 0.3 V
DH2	SW2 − 0.3 V to BST2 + 0.3 V
DL1, DL2 to PGND	−0.3 V to PV + 0.3 V
PGND to GND	±2 V
LDOSD, SYNC, FREQ, COMP1, COMP2, SS1, SS2, FB1, FB2, VREG, PV, POK1, POK2, TRK1, TRK2	−0.3 V to +6 V
θ_{JA} 4-Layer (JEDEC Standard Board)[1, 2]	45°C/W
Operating Ambient Temperature[3]	−40°C < T_A < +85°C
Operating Junction Temperature[3]	−40°C < T_J < +125°C
Storage Temperature	−65°C to +150°C

[1] Measured with exposed pad attached to PCB.

[2] Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is application and board-layout dependent. In applications where high maximum power dissipation exists, attention to thermal dissipation issues in board design is required. For more information, please refer to Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

[3] In applications where high power dissipation and poor package thermal resistance are present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A_MAX}) is dependent on the maximum operating junction temperature ($T_{J\_MAX\_OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D_MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), is given by the following equation: $T_{A\_MAX} = T_{J\_MAX\_OP} - (\theta_{JA} \times P_{D\_MAX})$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FUNCTIONAL BLOCK DIAGRAM

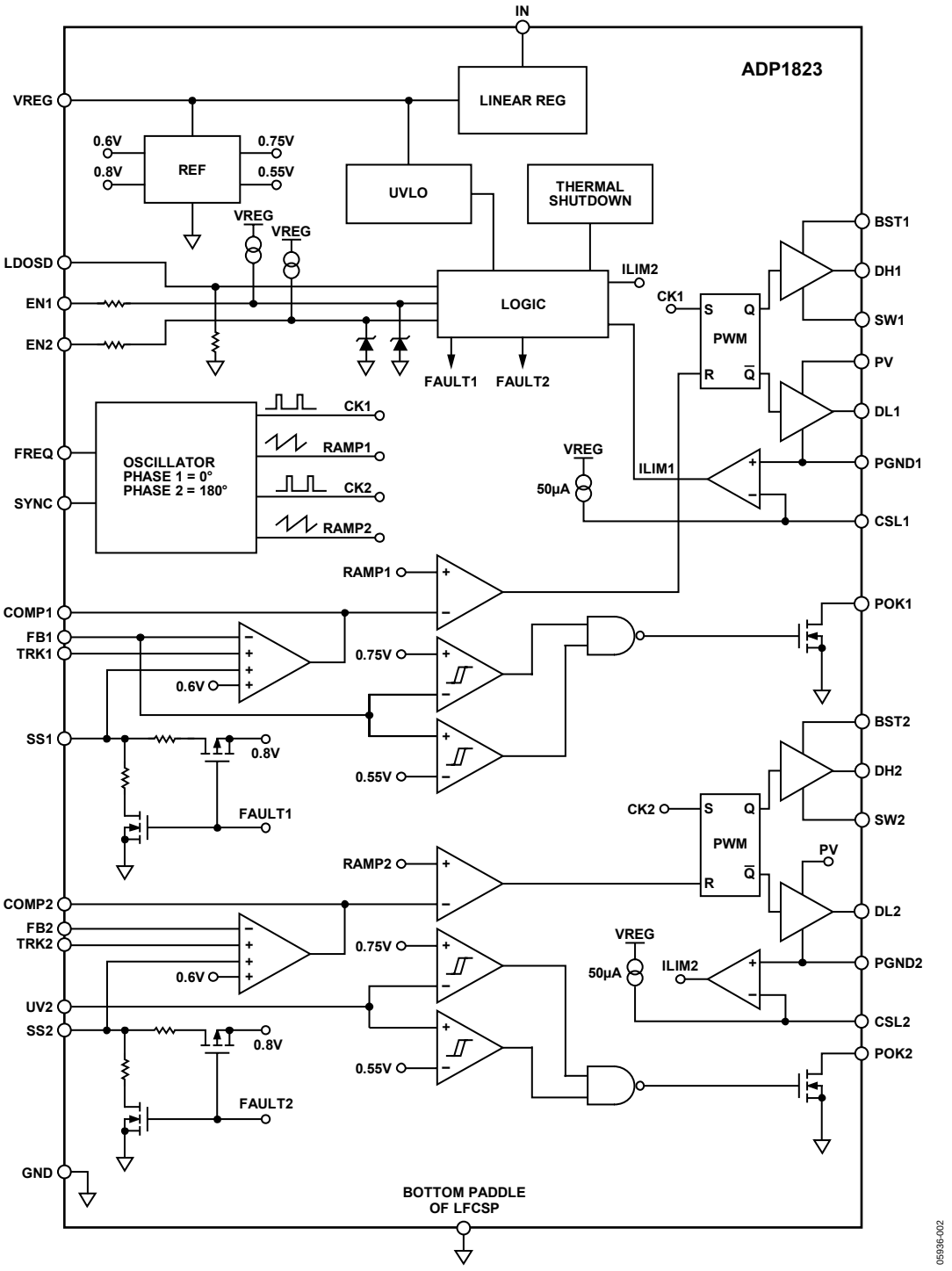


Figure 2. Functional Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

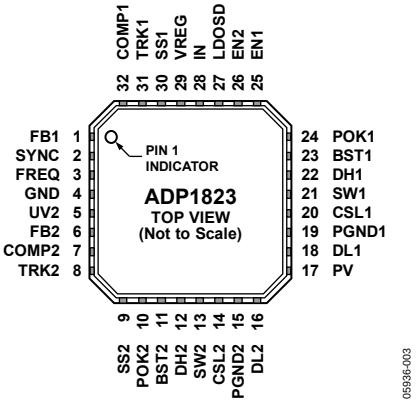


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB1	Feedback Voltage Input for Channel 1. Connect a resistor divider from the buck regulator output to GND and tie the tap to FB1 to set the output voltage.
2	SYNC	Frequency Synchronization Input. Accepts external signal between 600 kHz and 1.2 MHz or between 1.2 MHz and 2 MHz depending on whether FREQ is low or high, respectively. Connect SYNC to ground if not used.
3	FREQ	Frequency Select Input. Low for 300 kHz or high for 600 kHz.
4	GND	Ground. Connect to a ground plane directly beneath the ADP1823. Tie the bottom of the feedback dividers to this GND.
5	UV2	Input to the POK2 Undervoltage and Overvoltage Comparators. For the default thresholds, connect UV2 directly to FB2. For some tracking applications, connect UV2 to an extra tap on the FB2 voltage divider string.
6	FB2	Voltage Feedback Input for Channel 2. Connect a resistor divider from the buck regulator output to GND and tie the tap to FB2 to set the output voltage.
7	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from COMP2 to FB2 to compensate Channel 2.
8	TRK2	Tracking Input for Channel 2. To track a master voltage, drive TRK2 from a voltage divider from the master voltage. If the tracking function is not used, connect TRK2 to VREG.
9	SS2	Soft Start Control Input. Connect a capacitor from SS2 to GND to set the soft start period.
10	POK2	Open-Drain Power OK Output for Channel 2. Sinks current when UV2 is out of regulation. Connect a pull-up resistor from POK2 to VREG.
11	BST2	Boost Capacitor Input for Channel 2. Powers the high-side gate driver DH2. Connect a 0.22 µF to 0.47 µF ceramic capacitor from BST2 to SW2 and a Schottky diode from PV to BST2.
12	DH2	High-Side (Switch) Gate Driver Output for Channel 2.
13	SW2	Switch Node Connection for Channel 2.
14	CSL2	Current Sense Comparator Inverting Input for Channel 2. Connect a resistor between CSL2 and SW2 to set the current-limit offset.
15	PGND2	Ground for Channel 2 Gate Driver. Connect to a ground plane directly beneath the ADP1823.
16	DL2	Low-Side (Synchronous Rectifier) Gate Driver Output for Channel 2.
17	PV	Positive Input Voltage for Gate Drivers DL1 and DL2. Connect PV to VREG and bypass to ground with a 1 µF capacitor.
18	DL1	Low-Side (Synchronous Rectifier) Gate Driver Output for Channel 1.
19	PGND1	Ground for Channel 1 Gate Driver. Connect to a ground plane directly beneath the ADP1823.
20	CSL1	Current Sense Comparator Inverting Input for Channel 1. Connect a resistor between CSL1 and SW1 to set the current-limit offset.
21	SW1	Switch Node Connection for Channel 1.
22	DH1	High-Side (Switch) Gate Driver Output for Channel 1.
23	BST1	Boost Capacitor Input for Channel 1. Powers the high-side gate driver DH1. Connect a 0.22 µF to 0.47 µF ceramic capacitor from BST1 to SW1 and a Schottky diode from PV to BST1.
24	POK1	Open-Drain Power OK Output for Channel 1. Sinks current when FB1 is out of regulation. Connect a pull-up resistor from POK1 to VREG.
25	EN1	Enable Input for Channel 1. Drive EN1 high to turn on the Channel 1 controller, and drive it low to turn off. Enabling starts the internal LDO. Tie to IN for automatic startup.

Pin No.	Mnemonic	Description
26	EN2	Enable Input for Channel 2. Drive EN2 high to turn on the Channel 2 controller, and drive it low to turn off. Enabling starts the internal LDO. Tie to IN for automatic startup.
27	LDOSD	LDO Shut-Down Input. Only used to shut down the LDO in those applications where IN is tied directly to VREG. Otherwise connect LDOSD to GND or leave it open, as it has an internal 100 kΩ pull-down resistor.
28	IN	Input Supply to the Internal Linear Regulator. Drive IN with 5.5 V to 20 V to power the ADP1823 from the LDO. For input voltages between 2.9 V and 5.5 V, tie IN to VREG and PV.
29	VREG	Output of the Internal Linear Regulator (LDO). The internal circuitry and gate drivers are powered from VREG. Bypass VREG to ground plane with 1 µF ceramic capacitor.
30	SS1	Soft Start Control Input. Connect a capacitor from SS1 to GND to set the soft start period.
31	TRK1	Tracking Input for Channel 1. To track a master voltage, drive TRK1 from a voltage divider to the master voltage. If the tracking function is not used, connect TRK1 to VREG.
32	COMP1	Error Amplifier Output for Channel 1. Connect an RC network from COMP1 to FB1 to compensate Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

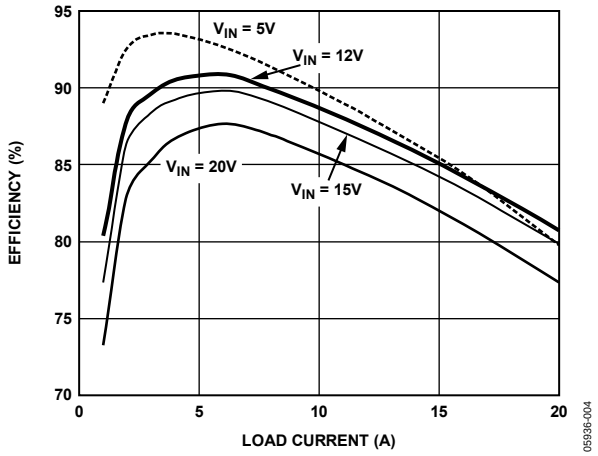


Figure 4. Efficiency vs. Load Current, V_{OUT} = 1.8 V, 300 kHz Switching

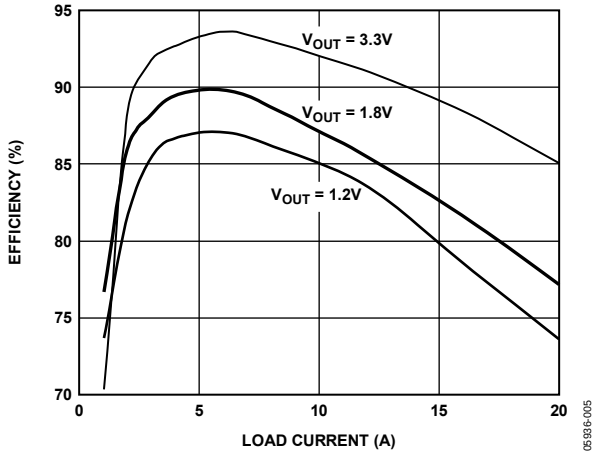


Figure 5. Efficiency vs. Load Current, V_{IN} = 12 V, 300 kHz Switching

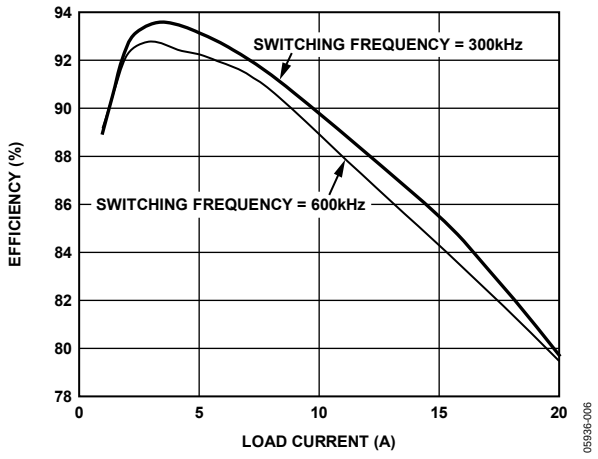


Figure 6. Efficiency vs. Load Current, V_{IN} = 5 V, V_{OUT} = 1.8 V

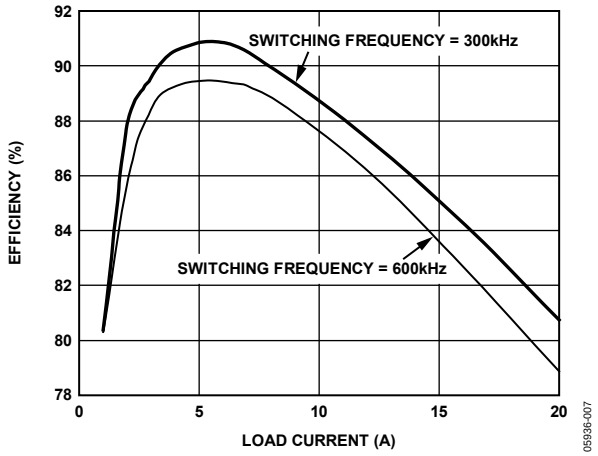


Figure 7. Efficiency vs. Load Current, V_{IN} = 12 V, V_{OUT} = 1.8 V

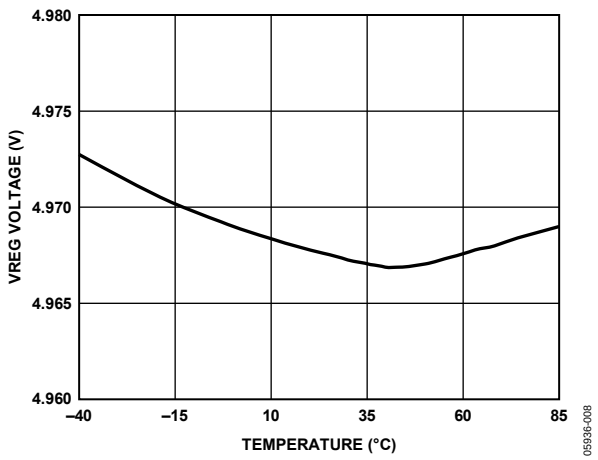


Figure 8. VREG Voltage vs. Temperature

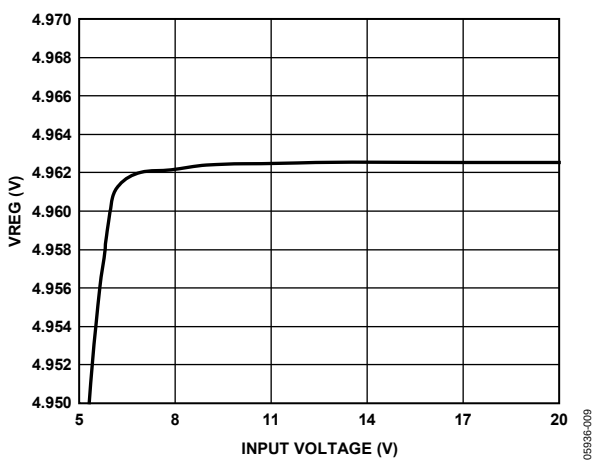


Figure 9. VREG vs. Input Voltage, 10 mA Load

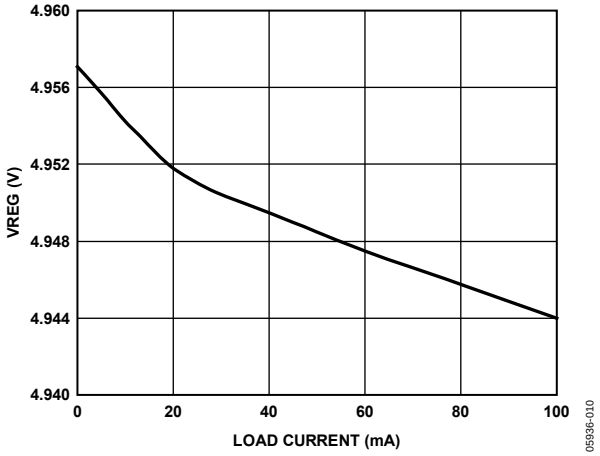


Figure 10. VREG vs. Load Current, V_{IN} = 12 V

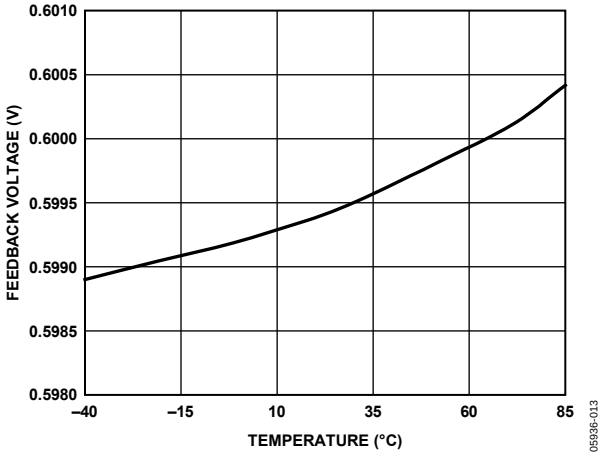


Figure 13. Feedback Voltage vs. Temperature, V_{IN} = 12 V

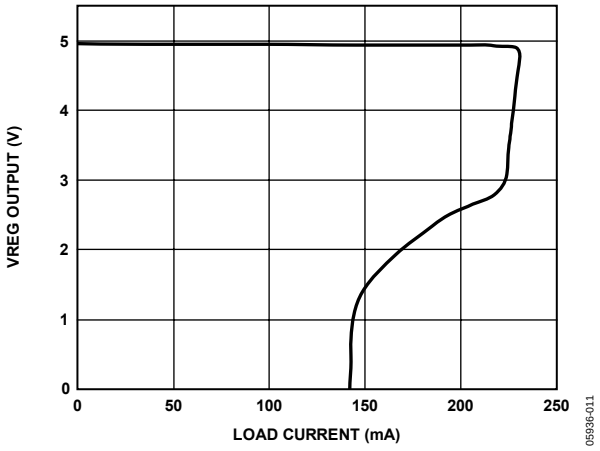


Figure 11. VREG Current-Limit Foldback

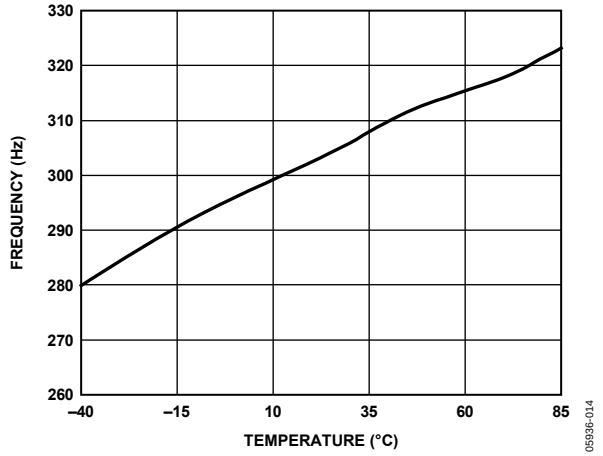


Figure 14. Switching Frequency vs. Temperature, V_{IN} = 12 V

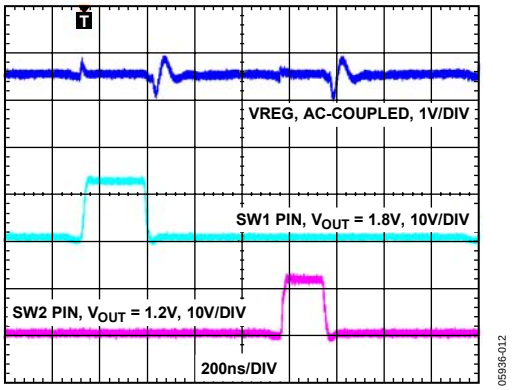


Figure 12. VREG Output During Normal Operation

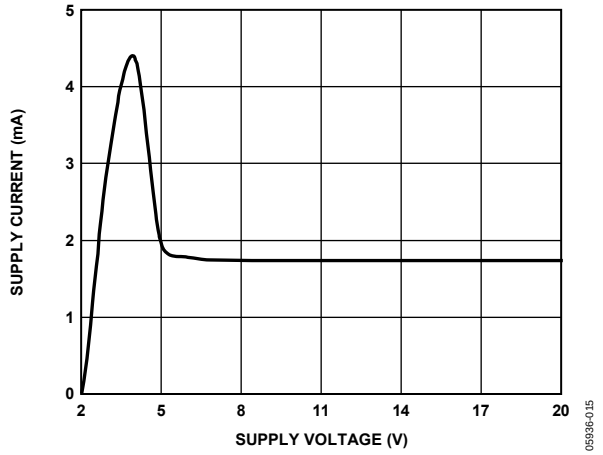


Figure 15. Supply Current vs. Input Voltage

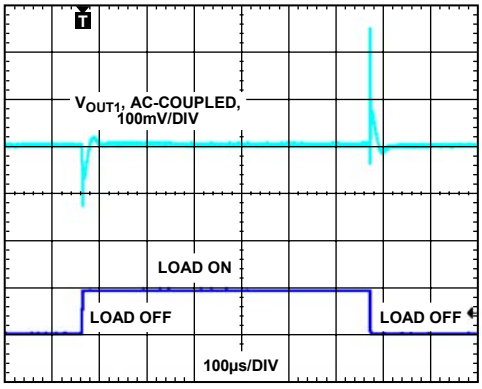


Figure 16. 1.5 A to 15 A Load Transient Response, V_{IN} = 12 V

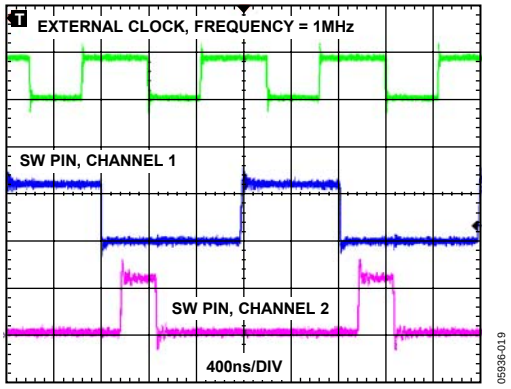


Figure 19. Out-of-Phase Switching, External 1 MHz Clock

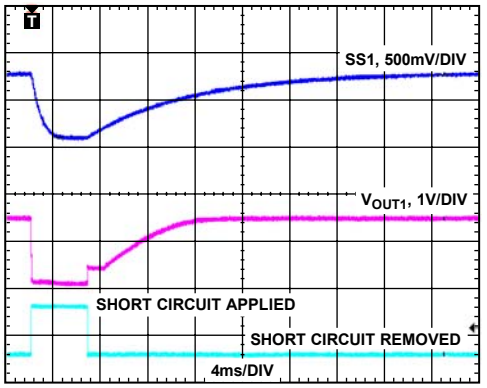


Figure 17. Output Short-Circuit Response

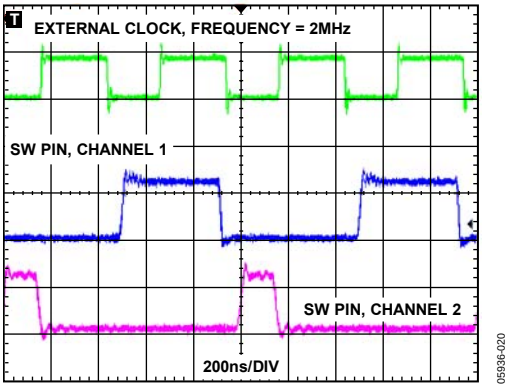


Figure 20. Out-of-Phase Switching, External 2 MHz Clock

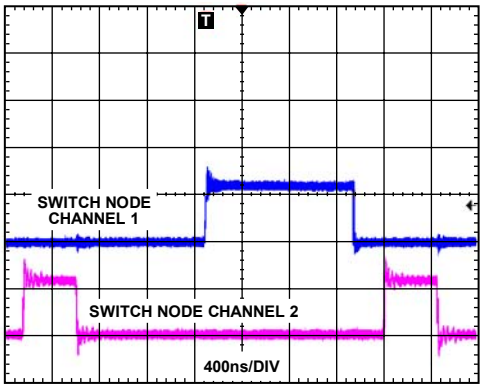


Figure 18. Out-of-Phase Switching, Internal Oscillator

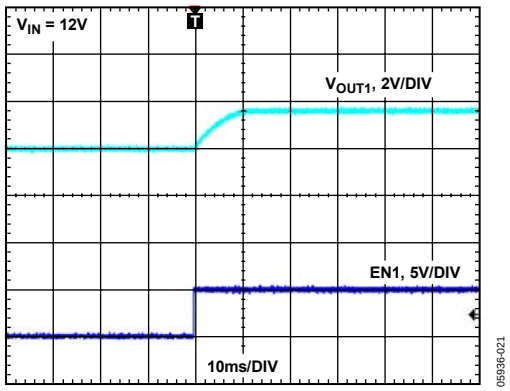


Figure 21. Enable Pin Response, V_{IN} = 12 V

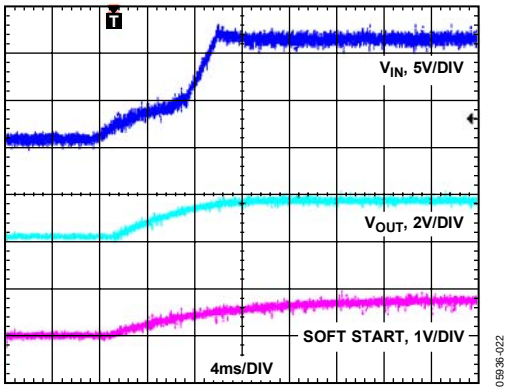


Figure 22. Power-On Response, EN Tied to V_{IN}

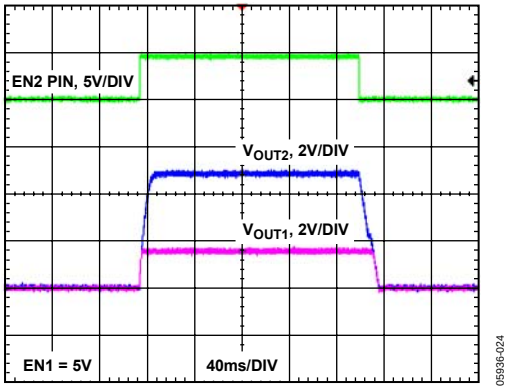


Figure 24. Coincident Voltage Tracking Response

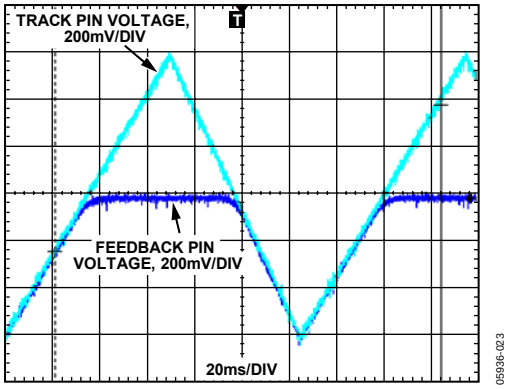


Figure 23. Output Voltage Tracking Response

THEORY OF OPERATION

The ADP1823 is a dual, synchronous, PWM buck controller capable of generating output voltages down to 0.6 V and output currents in the tens of amps. The switching of the regulators is interleaved for reduced current ripple. It is ideal for a wide range of applications, such as DSP and processor core I/O supplies, general-purpose power in telecommunications, medical imaging, gaming, PCs, set-top boxes, and industrial controls. The ADP1823 controller operates directly from 2.9 V to 20 V. It includes fully integrated MOSFET gate drivers and a linear regulator for internal and gate drive bias.

The ADP1823 operates at a fixed 300 kHz or 600 kHz switching frequency. The ADP1823 can also be synchronized to an external clock to switch at up to 1 MHz per channel. The ADP1823 includes soft start to prevent inrush current during startup, as well as a unique adjustable lossless current limit.

The ADP1823 offers flexible tracking for startup and shutdown sequencing. It is specified over the −40°C to +85°C temperature range and is available in a space-saving, 5 mm × 5 mm, 32-lead LFCSP.

INPUT POWER

The ADP1823 is powered from the IN pin up to 20 V. The internal low dropout linear regulator, VREG, regulates the IN voltage down to 5 V. The control circuits, gate drivers, and external boost capacitors operate from the LDO output. Tie the PV pin to VREG and bypass VREG with a 1 µF or greater capacitor.

The ADP1823 phase shifts the switching of the two step-down converters by 180°, thereby reducing the input ripple current. This reduces the size and cost of the input capacitors. The input voltage should be bypassed with a capacitor close to the high-side switch MOSFETs (see the Selecting the Input Capacitor section). In addition, a minimum 0.1 µF ceramic capacitor should be placed as close as possible to the IN pin.

The VREG output is sensed by the undervoltage lockout (UVLO) circuit to be certain that enough voltage headroom is available to run the controllers and gate drivers. As VREG rises above about 2.7 V, the controllers are enabled. The IN voltage is not directly monitored by UVLO. If the IN voltage is insufficient to allow VREG to be above the UVLO threshold, the controllers are disabled but the LDO continues to operate. The LDO is enabled whenever either EN1 or EN2 is high, even if VREG is below the UVLO threshold.

If the desired input voltage is between 2.9 V and 5.5 V, connect the IN directly to the VREG and PV pins, and drive LDOSD high to disable the internal regulator. The ADP1823 requires that the voltage at VREG and PV be limited to no more than 5.5 V. This is the only application where the LDOSD pin is used, and it should otherwise be grounded or left open. LDOSD has an internal 100 kΩ pull-down resistor.

While IN is limited to 20 V, the switching stage can run from up to 24 V and the BST pins can go to 30 V to support the gate drive. This can provide an advantage, for example, in the case of high frequency operation from a high input voltage. Dissipation on the ADP1823 can be limited by running IN from a low voltage rail while operating the switches from the high voltage rail.

START-UP LOGIC

The ADP1823 features independent enable inputs for each channel. Drive EN1 or EN2 high to enable their respective controllers. The LDO starts when either channel is enabled. When both controllers are disabled, the LDO is disabled and the IN quiescent current drops to about 10 µA. For automatic startup, connect EN1 and/or EN2 to IN. The enable pins are 20 V compliant, but they sink current through an internal 100 kΩ resistor once the EN pin voltage exceeds about 5 V.

INTERNAL LINEAR REGULATOR

The internal linear regulator, VREG, is low dropout, meaning it can regulate its output voltage close to the input voltage. It powers up the internal control and provides bias for the gate drivers. It is guaranteed to have more than 100 mA of output current capability, which is sufficient to handle the gate drive requirements of typical logic threshold MOSFETs driven at up to 1 MHz. Bypass VREG with a 1 µF or greater capacitor.

Because the LDO supplies the gate drive current, the output of VREG is subjected to sharp transient currents as the drivers switch and the boost capacitors recharge during each switching cycle. The LDO has been optimized to handle these transients without overload faults. Due to the gate drive loading, using the VREG output for other auxiliary system loads is not recommended.

The LDO includes a current limit well above the expected maximum gate drive load. This current limit also includes a short-circuit foldback to further limit the VREG current in the event of a fault.

OSCILLATOR AND SYNCHRONIZATION

The ADP1823 internal oscillator can be set to either 300 kHz or 600 kHz. Drive the FREQ pin low for 300 kHz; drive it high for 600 kHz. The oscillator generates a start clock for each switching phase and also generates the internal ramp voltages for the PWM modulation.

The SYNC input is used to synchronize the converter switching frequency to an external signal. The SYNC input should be driven with twice the desired switching frequency, as the SYNC input is divided by 2 and the resulting phases were used to clock the two channels alternately.

If FREQ is driven low, the recommended SYNC input frequency is between 600 kHz and 1.2 MHz. If FREQ is driven high, the recommended SYNC frequency is between 1.2 MHz and 2 MHz. The FREQ setting should be carefully observed for these SYNC frequency ranges, as the PWM voltage ramp scales down from about 1.3 V based on the percentage of frequency overdrive. Driving SYNC faster than recommended for the FREQ setting results in a small ramp signal, which could affect the signal-to-noise ratio and the modulator gain and stability.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset and clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH rising edges appear about 400 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. Depending on the startup conditions of Channel 1 and Channel 2, either Channel 1 or Channel 2 can be the first channel synchronized to the rising edge of the SYNC clock. If the external SYNC signal disappears during operation, the ADP1823 reverts back to its internal oscillator and experiences a delay of no more than a single cycle of the internal oscillator.

ERROR AMPLIFIER

The ADP1823 error amplifiers are operational amplifiers. The ADP1823 senses the output voltages through external resistor dividers at the FB1 and FB2 pins. The FB pins are the inverting inputs to the error amplifiers. The error amplifiers compare these feedback voltages to the internal 0.6 V reference, and the outputs of the error amplifiers appear at the COMP1 and COMP2 pins. The COMP pin voltages then directly control the duty cycle of each respective switching converter.

A series/parallel RC network is tied between the FB pins and their respective COMP pins to provide the compensation for the buck converter control loops. A detailed design procedure for compensating the system is provided in the Compensating the Voltage Mode Buck Regulator section.

The error amplifier outputs are clamped between a lower limit of about 0.7 V and a higher limit of about 2.4 V. When the COMP pins are low, the switching duty cycle goes to 0%, and when the COMP pins are high, the switching duty cycle goes to the maximum.

The SS and TRK pins are auxiliary positive inputs to the error amplifiers. Whichever has the lowest voltage, SS, TRK, or the internal 0.6 V reference, controls the FB pin voltage and thus the output. Therefore, if two or more of these inputs are close to each other, a small offset is imposed on the error amplifier. For example, if TRK approaches the 0.6 V reference, the FB sees about 18 mV of negative offset at room temperature. For this reason, the soft start pins have a built-in negative offset and they charge to 0.8 V. If the TRK pins are not used, they should be tied high to VREG.

SOFT START

The ADP1823 employs a programmable soft start that reduces input current transients and prevents output overshoot. The SS1 and SS2 pins drive auxiliary positive inputs to their respective error amplifiers, thus the voltage at these pins regulate the voltage at their respective feedback control pins.

Program soft start by connecting capacitors from SS1 and SS2 to GND. On startup, the capacitor charges from an internal 90 kΩ resistor to 0.8 V. The regulator output voltage rises with the voltage at its respective soft start pin, allowing the output voltage to rise slowly, reducing inrush current. See the information about Soft Start in the Applications Information section.

When a controller is disabled or experiences a current fault, the soft start capacitor is discharged through an internal 6 kΩ resistor, so that at restart or recovery from fault the output voltage soft starts again.

POWER OK INDICATOR

The ADP1823 features open-drain, Power OK outputs, POK1 and POK2, which sink current when their respective output voltages drop, typically 8% below the nominal regulation voltage. The POK pins also go low for overvoltage of typically 25%. Use this output as a logical power-good signal by connecting pull-up resistors from POK1 and POK2 to VREG.

The POK1 comparator directly monitors FB1, and the threshold is fixed at 550 mV for undervoltage and 750 mV for overvoltage. However, the POK2 undervoltage and overvoltage comparator input is connected to UV2 rather than FB2. For the default thresholds at FB2, connect UV2 directly to FB2.

In a ratiometric tracking configuration, however, Channel 2 can be configured to be a fraction of a master voltage, and thus FB2 regulated to a voltage lower than the 0.6 V internal reference. In this configuration, UV2 can be tied to a different tap on the feedback divider, allowing a POK2 indication at an appropriate output voltage threshold. See the Setting the Channel 2 Undervoltage Threshold for Ratiometric Tracking section.

TRACKING

The ADP1823 features tracking inputs, TRK1 and TRK2, which make the output voltages track another, master voltage. This is especially useful in core and I/O voltage sequencing applications where one output of the ADP1823 can be set to track and not exceed the other, or in other multiple output systems where specific sequencing is required.

The internal error amplifiers include three positive inputs, the internal 0.6 V reference voltage and their respective SS and TRK pins. The error amplifiers regulate the FB pins to the lowest of the three inputs. To track a supply voltage, tie the TRK pin to a resistor divider from the voltage to be tracked. See the Voltage Tracking section.

MOSFET DRIVERS

The DH1 and DH2 pins drive the high-side switch MOSFETs. These are boosted 5 V gate drivers that are powered by bootstrap capacitor circuits. This configuration allows the high-side, n-channel MOSFET gate to be driven above the input voltage, allowing full enhancement and a low voltage drop across the MOSFET. The bootstrap capacitors are connected from the SW pins to their respective BST pins. The bootstrap Schottky diodes from the PV pins to the BST pins recharge the bootstrap capacitors every time the SW nodes go low. Use a bootstrap capacitor value greater than 100× the high-side MOSFET input capacitance.

In practice, the switch node can run up to 24 V of input voltage, and the boost nodes can operate more than 5 V above this to allow full gate drive. The IN pin can be run from 2.9 V to 20 V. This can provide an advantage, for example, in the case of high frequency operation from very high input voltage. Dissipation on the ADP1823 can be limited by running IN from a lower voltage rail while operating the switches from the high voltage rail.

The switching cycle is initiated by the internal clock signal. The high-side MOSFET is turned on by the DH driver, and the SW node goes high, pulling up on the inductor. When the internally generated ramp signal crosses the COMP pin voltage, the switch MOSFET is turned off and the low-side synchronous rectifier MOSFET is turned on by the DL driver. Active break-before-make circuitry, as well as a supplemental fixed dead time, are used to prevent cross-conduction in the switches.

The DL1 and DL2 pins provide gate drive for the low-side MOSFET synchronous rectifiers. Internal circuitry monitors the external MOSFETs to ensure break-before-make switching to prevent cross-conduction. An active dead time reduction circuit reduces the break-before-make time of the switching to limit the losses due to current flowing through the synchronous rectifier body diode.

The PV pin provides power to the low-side drivers. It is limited to 5.5 V maximum input and should have a local decoupling capacitor.

The synchronous rectifiers are turned on for a minimum time of about 200 ns on every switching cycle in order to sense the current. This and the nonoverlap dead times put a limit on the maximum high-side switch duty cycle based on the selected switching frequency. Typically, this is about 90% at 300 kHz switching, and at 1 MHz switching, it reduces to about 70% maximum duty cycle.

Because the two channels are 180° out of phase, if one is operating around 50% duty cycle, it is common for it to jitter when the other channel starts switching. The magnitude of the jitter depends somewhat on layout, but it is difficult to avoid in practice.

When the ADP1823 is disabled, the drivers shut off the external MOSFETs, so that the SW node becomes three-stated or changes to high impedance.

CURRENT LIMIT

The ADP1823 employs a unique, programmable, cycle-by-cycle lossless current-limit circuit that uses a small, ordinary, inexpensive resistor to set the threshold. Every switching cycle, the synchronous rectifier turns on for a minimum time and the voltage drop across the MOSFET R_{DSON} is measured to determine if the current is too high.

This measurement is done by an internal current-limit comparator and an external current-limit set resistor. The resistor is connected between the switch node (that is the drain of the rectifier MOSFET) and the CSL pin. The CSL pin, which is the inverting input of the comparator, forces 50 µA through the resistor to create an offset voltage drop across it.

When the inductor current is flowing in the MOSFET rectifier, its drain is forced below PGND by the voltage drop across its R_{DSON}. If the R_{DSON} voltage drop exceeds the preset drop on the external resistor, the inverting comparator input is similarly forced below PGND and an overcurrent fault is flagged.

The normal transient ringing on the switch node is ignored for 100 ns after the synchronous rectifier turns on, so the overcurrent condition must also persist for 100 ns in order for a fault to be flagged.

When an overcurrent event occurs, the overcurrent comparator prevents switching cycles until the rectifier current has decayed below the threshold. The overcurrent comparator is blanked for the first 100 ns of the synchronous rectifier cycle to prevent switch node ringing from falsely tripping the current limit. The ADP1823 senses the current limit during the off cycle. When the current-limit condition occurs, the ADP1823 resets the internal clock until the overcurrent condition disappears. This suppresses the start clock cycles until the overload condition is removed. At the same time, the SS cap is discharged through a 6 kΩ resistor. The SS input is an auxiliary positive input of the error amplifier, so it behaves like another voltage reference. The lowest reference voltage wins. Discharging the SS voltage causes the converter to use a lower voltage reference when switching is allowed again. Therefore, as switching cycles continue around the current limit, the output looks roughly like a constant current source due to the rectifier limit, and the output voltage droops as the load resistance decreases. When the overcurrent condition is removed, operation resumes in soft start mode.

See the Setting the Current Limit section for more information.

APPLICATIONS INFORMATION

SELECTING THE INPUT CAPACITOR

The input current to a buck converter is a pulse waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. The input capacitor needs sufficient ripple current rating to handle the input ripple and also ESR that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, good practice is to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs, one bulk capacitor of sufficiently high current rating as calculated in Equation 1, along with 10 µF of ceramic capacitor.

Select an input bulk capacitor based on its ripple current rating. If both Channel 1 and Channel 2 maximum output load currents are about the same, the input ripple current is less than half of the higher of the output load currents. In this case, use an input capacitor with a ripple current rating greater than half of the highest load current.

$$I_{RIPPLE} > \frac{I_L}{2} \quad (1)$$

If the Output 1 and Output 2 load currents are significantly different (if the smaller is less than 50% of the larger), then the procedure in Equation 1 yields a larger input capacitor than required. In this case, the input capacitor can be chosen as in the case of a single phase converter with only the higher load current, so first determine the duty cycle of the output with the larger load current:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (2)$$

In this case, the input capacitor ripple current is approximately

$$I_{RIPPLE} \approx I_L \sqrt{D(1-D)} \quad (3)$$

where I_L is the maximum inductor or load current for the channel and D is the duty cycle. Use this method to determine the input capacitor ripple current rating for duty cycles between 20% and 80%.

For duty cycles less than 20% or greater than 80%, use an input capacitor with ripple current rating $I_{RIPPLE} > 0.4\ I_L$.

Selecting the Output LC Filter

The output LC filter attenuates the switching voltage, making the output an almost dc voltage. The output LC filter characteristics determine the residual output ripple voltage.

Choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than is required, and using a smaller value results in increased losses in the inductor and MOSFETs.

Choose the inductor value by the equation

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_L\ f_{SW}} \left(\frac{V_{OUT}}{V_{IN}} \right) \quad (4)$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current, typically 1/3 of the maximum dc load current.

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the equivalent series resistance (ESR) and the equivalent series inductance (ESL). The output voltage ripple can be approximated with

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 f_{SW} C_{OUT}} + 4 f_{SW}\ ESL \right) \quad (5)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
ESL is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Note that the factors of 8 and 4 in Equation 5 would normally be 2π for sinusoidal waveforms, but the ripple current waveform in this application is triangular. Parallel combinations of different types of capacitors, for example, a large aluminum electrolytic in parallel with MLCCs, may give different results.

Usually, the impedance is dominated by ESR at the switching frequency, as stated in the maximum ESR rating on the capacitor data sheet, so this equation reduces to

$$\Delta V_{OUT} \cong \Delta I_L ESR \quad (6)$$

Electrolytic capacitors have significant ESL also, on the order of 5 nH to 20 nH, depending on type, size, and geometry, and PCB traces contribute some ESR and ESL as well. However, using the maximum ESR rating from the capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output cap is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the ripple equation reduces to

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{8\, C_{OUT}\, f_{SW}} \quad (7)$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation due to a change in load is dependent on the output capacitor characteristics. Again, usually the capacitor ESR dominates this response, and the ΔV_{OUT} in Equation 6 can be used with the load step current value for ΔI_L.

SELECTING THE MOSFETS

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance (R_{DSON}) to reduce I^2R losses and low gate-charge to reduce switching losses. In addition, the MOSFET must have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in overheating.

The power switch, or high-side MOSFET, carries the load current during the PWM on-time, carries the transition loss of the switching behavior, and requires gate charge drive to switch. Typically, the smaller the MOSFET R_{DSON}, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances those two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong I_L^2 R_{DSON} \frac{V_{OUT}}{V_{IN}} \quad (8)$$

where:
P_C = conduction power loss.
R_{DSON} = MOSFET on resistance.

The gate charge losses are dissipated by the ADP1823 regulator and gate drivers and affect the efficiency of the system. The gate charge loss is approximated by the equation

$$P_G \cong V_{IN} Q_G f_{SW} \quad (9)$$

where:
P_G = gate charge power.
Q_G = MOSFET total gate charge.
f_{SW} = converter switching frequency.

Making the conduction losses balance the gate charge losses usually yields the most efficient choice.

Furthermore, the high-side MOSFET transition loss is approximated by the equation

$$P_T \cong \frac{V_{IN} I_L (t_R + t_F) f_{SW}}{2} \quad (10)$$

where t_R and t_F are the rise and fall times of the selected MOSFET as stated in the MOSFET data sheet.

The total power dissipation of the high-side MOSFET is the sum of the previous losses:

$$P_D = P_C + P_G + P_T \quad (11)$$

where P_D is the total high-side MOSFET power loss. This dissipation heats the high-side MOSFET.

The conduction losses may need an adjustment to account for the MOSFET R_{DSON} variation with temperature. Note that MOSFET R_{DSON} increases with increasing temperature. The MOSFET data sheet should list the thermal resistance of the package, θ_{JA}, along with a normalized curve of the temperature coefficient of the R_{DSON}. For the power dissipation estimated above, calculate the MOSFET junction temperature rise over the ambient temperature of interest:

$$T_J = T_A + \theta_{JA} P_D \quad (12)$$

Then calculate the new R_{DSON} from the temperature coefficient curve and the R_{DSON} spec at 25°C. A typical value of the temperature coefficient (TC) of the R_{DSON} is 0.004/°C, so an alternate method to calculate the MOSFET R_{DSON} at a second temperature, T_J, is

$$R_{DSON} @ T_J = R_{DSON} @ 25°C\,[1 + TC(T_J - 25°C)] \quad (13)$$

Then the conduction losses can be recalculated and the procedure iterated once or twice until the junction temperature calculations are relatively consistent.

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time, and therefore, to achieve high efficiency it is critical to optimize the low-side MOSFET for small on resistance. In cases where the power loss exceeds the MOSFET rating, or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET power loss is

$$P_{LS} \cong I_L^2 R_{DSON} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (14)$$

where:
P_{LS} is the low-side MOSFET on resistance.
R_{DSON} is the parallel combination of the resistances of the low-side MOSFETs.

Check the gate charge losses of the synchronous rectifier(s) using the P_G equation (Equation 9) to be sure they are reasonable.

SETTING THE CURRENT LIMIT

The current-limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set through the current-limit resistor, R_{CL}. The current sense pins, CSL1 and CSL2, source 50 µA through their respective R_{CL}. This creates an offset voltage of R_{CL} multiplied by the 50 µA CSL current. When the drop across the low-side MOSFET R_{DSON} is equal to or greater than this offset voltage, the ADP1823 flags a current-limit event.

Because the CSL current and the MOSFET R_{DSON} vary over process and temperature, the minimum current limit should be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired current-limit level plus the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum CSL current:

$$R_{CL} = \frac{I_{LPK} \; R_{DSON\,(MAX)}}{44\ \mu A} \tag{15}$$

where I_{LPK} is the peak inductor current.

Because the buck converters are usually running fairly high current, PCB layout and component placement may affect the current-limit setting. An iteration of the R_{CL} values may be required for a particular board layout and MOSFET selection. If alternate MOSFETs are substituted at some point in production, the values of the R_{CL} resistor may also need an iteration.

FEEDBACK VOLTAGE DIVIDER

The output regulation voltage is set through the feedback voltage divider. The output voltage is reduced through the voltage divider and drives the FB feedback input. The regulation threshold at FB is 0.6 V. The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, R_{BOT}, needs to be less than 9 kΩ, which results in 67 µA of divider current. For R_{BOT}, use 1 kΩ to 10 kΩ. A larger value resistor can be used, but results in a reduction in output voltage accuracy due to the input bias current at the FB pin, while lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \tag{16}$$

where:
R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

COMPENSATING THE VOLTAGE MODE BUCK REGULATOR

Assuming the LC filter design is complete, the feedback control system can then be compensated. Good compensation is critical to proper operation of the regulator. Calculate the quantities in Equation 17 through Equation 58 to derive the compensation values. For convenience, Table 4 provides a summary of the design equations and space for calculations. The information can then be added to a spread-sheet for automated calculation.

The goal is to guarantee that the voltage gain of the buck converter crosses unity at a slope that provides adequate phase margin for stable operation. Additionally, at frequencies above the crossover frequency, f_{CO}, guaranteeing sufficient gain margin and attenuation of switching noise are important secondary goals. For initial practical designs, a good choice for the crossover frequency is one tenth of the switching frequency, so first calculate

$$f_{CO} = \frac{f_{SW}}{10} \tag{17}$$

This gives sufficient frequency range to design a compensation that attenuates switching artifacts, while also giving sufficient control loop bandwidth to provide good transient response.

The output LC filter is a resonant network that inflicts two poles upon the response at a frequency f_{LC}, so next calculate

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \tag{18}$$

Generally speaking, the LC corner frequency is about two orders of magnitude below the switching frequency, and therefore about one order of magnitude below crossover. To achieve sufficient phase margin at crossover to guarantee stability, the design must compensate for the two poles at the LC corner frequency with two zeros to boost the system phase prior to crossover. The two zeros require an additional pole or two above the crossover frequency to guarantee adequate gain margin and attenuation of switching noise at high frequencies.

Depending on component selection, one zero might already be generated by the equivalent series resistance (ESR) of the output capacitor. Calculate this zero corner frequency, f_{ESR}, as

$$f_{ESR} = \frac{1}{2\pi\, R_{ESR} C_{OUT}} \tag{19}$$

This zero is often near or below crossover and is useful in bringing back some of the phase lost at the LC corner.

Figure 25 shows a typical Bode plot of the LC filter by itself.

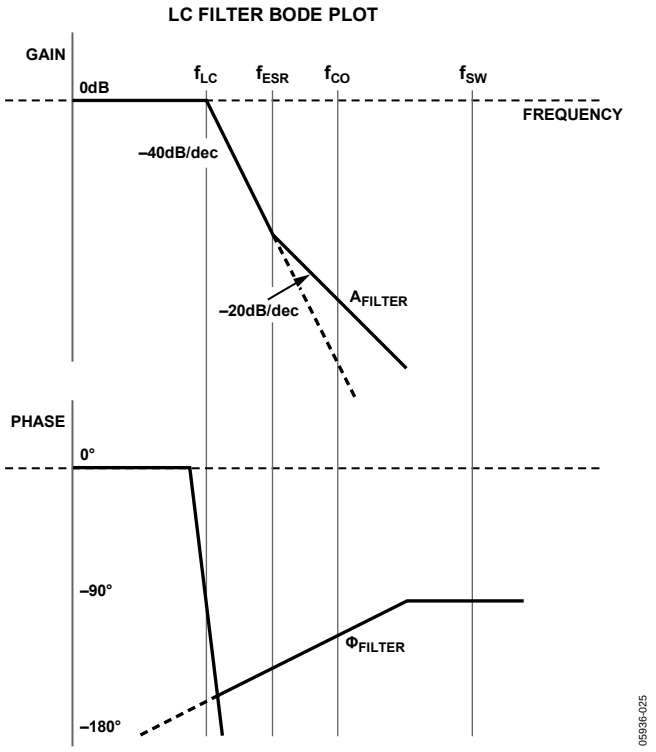


Figure 25. LC Filter Bode Plot

The gain of the LC filter at crossover can be linearly approximated from Figure 25 as

$$A_{FILTER} = A_{LC} + A_{ESR}$$

$$A_{FILTER} = -40\ \text{dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\ \text{dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right) \quad (20)$$

If $f_{ESR} \approx f_{CO}$, then add another 3 dB to account for the local difference between the exact solution and the linear approximation above.

To compensate the control loop, the gain of the system must be brought back up so that it is 0 dB at the desired crossover frequency. Some gain is provided by the PWM modulation itself, so next calculate

$$A_{MOD} = 20 \log\left(\frac{V_{IN}}{V_{RAMP}}\right) \quad (21)$$

For systems using the internal oscillator, this becomes

$$A_{MOD} = 20 \log\left(\frac{V_{IN}}{1.3\ V}\right) \quad (22)$$

Note that if the converter is being synchronized, the ramp voltage, V_{RAMP}, is lower than 1.3 V by the percentage of frequency increase over the nominal setting of the FREQ pin:

$$V_{RAMP} = 1.3\ \text{V}\left(\frac{2\ f_{FREQ}}{f_{SYNC}}\right) \quad (23)$$

The factor of 2 in the numerator takes into account that the SYNC frequency is divided by 2 to generate the switching frequency. For example, if the FREQ pin is set high for the 600 kHz range and a 2 MHz SYNC signal is applied, the ramp voltage is 0.78 V. This increases the gain of the modulator by 4.4 dB in this example.

The rest of the system gain needed to reach 0 dB at crossover is provided by the error amplifier and is covered in the compensation design information that follows. The total gain of the system, therefore, is given by

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (24)$$

where:
A_{MOD} is the gain of the PWM modulator
A_{FILTER} is the gain of the LC filter including the effects of the ESR zero
A_{COMP} is the gain of the compensated error amplifier.

Additionally, the phase of the system must be brought back up to guarantee stability. Note from the bode plot of the filter that the LC contributes −180° of phase shift. Additionally, because the error amplifier is an integrator at low frequency, it contributes an initial −90°. Therefore, before adding compensation or accounting for the ESR zero, the system is already down −270°. To avoid loop inversion at crossover, or −180° phase shift, a good initial practical design is to require a phase margin of 60°, which is therefore an overall phase loss of −120° from the initial low frequency dc phase. The goal of the compensation is to boost the phase back up from −270° to −120° at crossover.

Two common compensation schemes are used, which are sometimes referred to as Type II or Type III compensation, depending on whether the compensation design includes two or three poles. (Dominant pole compensations, or single pole compensation, is referred to as Type I compensation, but unfortunately, it is not very useful for dealing successfully with switching regulators.)

If the zero produced by the ESR of the output capacitor provides sufficient phase boost at crossover, Type II compensation is adequate. If the phase boost produced by the ESR of the output capacitor is not sufficient, another zero is added to the compensation network, and thus Type III is used. A general rule to determine the scheme is whether the phase contribution of the ESR zero is greater than 70° at crossover.

In Figure 26, the location of the ESR zero corner frequency gives significantly different net phase at the crossover frequency.

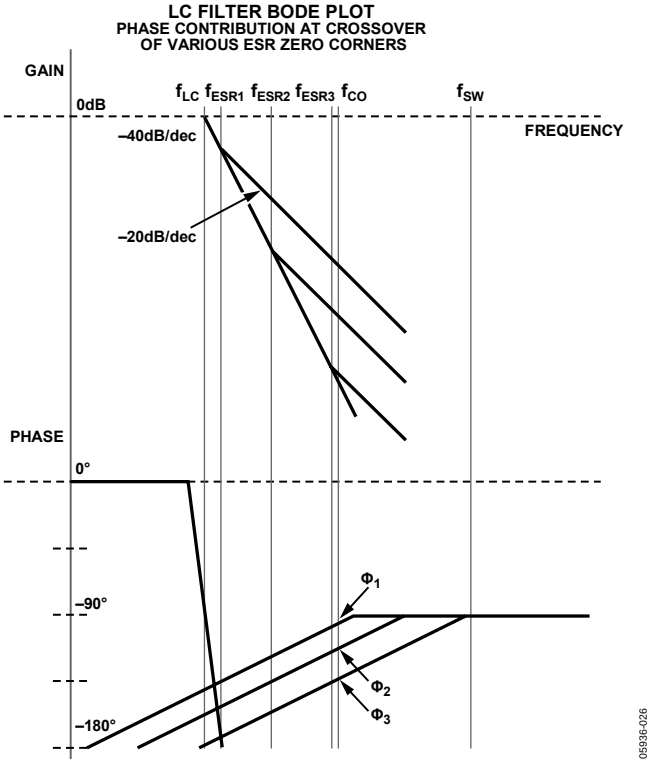


Figure 26. LC Filter Bode Plot

Using a linear approximation from Figure 26, the phase contribution of the ESR zero at crossover can be estimated by

$$\phi_{ESR} = 45° \times \log \frac{10 \times f_{CO}}{f_{ESR}} \quad (25)$$

If $\varphi_{ESR} \geq 70°$, then Type II compensation is adequate.

If $\varphi_{ESR} < 70°$, use Type III, as an additional zero is needed.

The total phase of the system at crossover is the sum of the contributing elements, namely:

$$\varphi_T = \varphi_{LC} + \varphi_{ESR} + \varphi_{COMP} \quad (26)$$

where:

$\varphi_{LC} = -180°$

φ_{ESR} is as calculated in Equation 25

$$\varphi_{COMP} = -90° + \varphi_P + \varphi_Z \quad (27)$$

Note in the compensator phase expression shown in Equation 27, the −90° term is the phase contributed by the initial integrator pole. The φ_P is the additional phase contributed by the high frequency compensation poles placed above crossover, and φ_Z is the phase contributed by the compensation zeros placed below crossover. For the system to be stable at crossover, phase boost is required from the compensator.

For stability, the total phase at crossover is designed to be equal to −120°:

$$\varphi_T = \varphi_{LC} + \varphi_{ESR} + \varphi_{COMP} \quad (28)$$

$$-120° = -180° + \varphi_{ESR} + -90° + \varphi_P + \varphi_Z \quad (29)$$

Define phase boost, φ_B, to be the portion of the phase at crossover contributed by the compensator's higher order poles and zeros:

$$\varphi_B = \varphi_P + \varphi_Z \quad (30)$$

$$\varphi_B = 150° - \varphi_{ESR} \quad (31)$$

Venable[1] showed that an optimum compensation solution was to place the zeros and poles symmetrically around the crossover frequency. He derived a factor known as K with which the frequencies of the compensation zeros and poles may be calculated. K is calculated for the type of compensation selected in Figure 27.

Type II Compensator

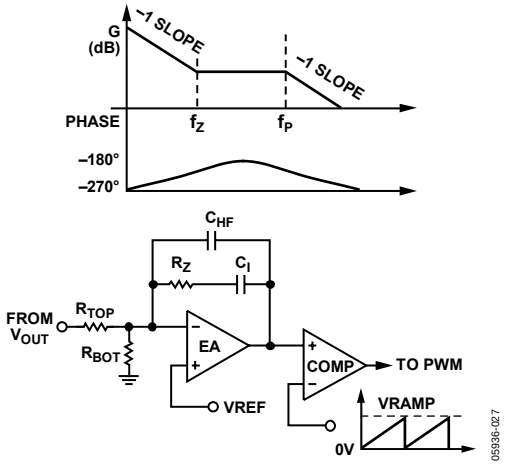


Figure 27. Type II Compensation

To calculate K for Type II compensation, use

$$K = \tan\left(\frac{\phi_B}{2} + 45°\right) \quad (32)$$

Values of K between 4 and 15 are practical for implementation; if the selected type of compensation does not yield a reasonable value of K, try the other type.

From K, the frequency of the added zeros, f_Z, is below crossover by

$$f_Z = \frac{f_{CO}}{K} \text{ for Type II} \quad (33)$$

Similarly, the frequency of the added poles, f_P, should be above crossover:

$$f_P = f_{CO} K \text{ for Type II} \quad (34)$$

[1] D. Venable, "The K Factor: A New Mathematical Tool for Stability Analysis and Synthesis," 1983.

Select R_{TOP} between 1 kΩ and 10 kΩ. A good starting value is 2 kΩ.

Next, calculate R_{BOT} as

$$R_{BOT} = \frac{V_{FB} R_{TOP}}{V_{OUT} - V_{FB}} \quad (35)$$

$$R_{BOT} = \frac{0.6\ \text{V} \times R_{TOP}}{V_{OUT} - 0.6\ \text{V}} \quad (36)$$

Note that if ratiometric tracking is used, substitute the actual FB voltage for the 0.6 V term used in Equation 36.

Calculate the compensator gain needed at crossover to achieve 0 dB total system gain:

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (37)$$

$$0\ \text{dB} = A_{MOD} + A_{FILTER} + A_{COMP} \quad (38)$$

$$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER} \quad (39)$$

Calculate the value of R_Z to achieve that gain:

$$A_{COMP} = 20 \times \log\left(\frac{R_Z}{R_{TOP}}\right) \quad (40)$$

$$R_Z = R_{TOP} \times 10^{\left(\frac{A_{COMP}}{20}\right)} \quad (41)$$

Calculate the integrator cap value to place the compensation zero at the desired frequency:

$$C_I = \frac{1}{2\pi R_Z f_Z} \quad (42)$$

Calculate the capacitor value for the high frequency pole:

$$C_{HF} = \frac{1}{2\pi R_Z f_P} \quad (43)$$

Type III Compensator

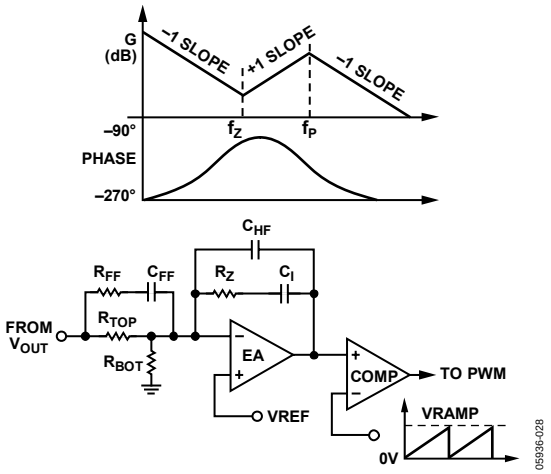


Figure 28. Type III Compensation

$$K = \left(\tan\left(\frac{\phi_B}{2} + 45\right)\right)^2 \quad (44)$$

and

$$f_Z = \frac{f_{CO}}{\sqrt{K}} \quad (45)$$

and

$$f_P = f_{CO} \sqrt{K} \quad (46)$$

Select R_{TOP} between 1 kΩ and 10 kΩ. A good starting point is 2 kΩ.

Next, calculate R_{BOT} as

$$R_{BOT} = \frac{V_{FB} R_{TOP}}{V_{OUT} - V_{FB}} \quad (47)$$

$$R_{BOT} = \frac{0.6\ \text{V} \times R_{TOP}}{V_{OUT} - 0.6\ \text{V}} \quad (48)$$

Note that if ratiometric tracking is used, substitute the actual FB voltage for the 0.6 V term in Equation 48.

Calculate the feedforward capacitor to produce the first compensator zero:

$$C_{FF} = \frac{1}{2\pi R_{TOP} f_Z} \quad (49)$$

Calculate the resistor of the feedforward network to provide the first high frequency compensator pole:

$$R_{FF} = \frac{1}{2\pi C_{FF} f_P} \quad (50)$$

Calculate the impedance of the feedforward network at the crossover frequency, as this is required to set the gain of the compensator:

$$Z_{FF} = \frac{1}{2\pi C_{FF} f_{CO}} + R_{FF} \quad (51)$$

Calculate the compensator gain needed at crossover to achieve 0 dB total system gain:

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (52)$$

$$0\ \text{dB} = A_{MOD} + A_{FILTER} + A_{COMP} \quad (53)$$

$$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER} \quad (54)$$

Calculate the value of R_Z to achieve that gain:

$$A_{COMP} = 20 \times \log\left(\frac{R_Z}{R_{TOP} \,||\, Z_{FF}}\right) \quad (55)$$

$$R_Z = \left(R_{TOP} \,||\, Z_{FF}\right) \times 10^{\left(\frac{A_{COMP}}{20}\right)} \quad (56)$$

Calculate the integrator cap value to place the compensation zero at the desired frequency:

$$C_I = \frac{1}{2\pi R_Z f_Z} \quad (57)$$

Calculate the capacitor value for the high frequency pole:

$$C_{HF} = \frac{1}{2\pi R_Z f_P} \quad (58)$$

Check that the calculated component values are reasonable. For instance, capacitors smaller than about 10 pF should be avoided. In addition, the ADP1823 error amplifier has finite output current drive, so R_Z values less than a few kΩ and C_I values greater than 10 nF should be avoided. If necessary, recalculate the compensation network with a different starting value of R_{TOP}. If C_{HF} is too small, start with a smaller value R_{TOP}. If R_Z is too small and C_I is too big, start with a larger value of R_{TOP}.

This compensation technique should yield a good working solution. For a more exact method or to optimize for other system characteristics, a number of references and tools are available from your Analog Devices, Inc., application support team.

SOFT START

The ADP1823 uses an adjustable soft start to limit the output voltage ramp-up period, thus limiting the input inrush current. The soft start is set by selecting the capacitor, C_{SS}, from SS1 and SS2 to GND. The ADP1823 charges C_{SS} to 0.8 V through an internal 90 kΩ resistor. The voltage on the soft start capacitor while it is charging is

$$V_{CSS} = 0.8\ \text{V}\left(1 - e^{\frac{t}{RC_{SS}}}\right) \quad (59)$$

The soft start period ends when the voltage on the soft start pin reaches 0.6 V. Substituting 0.6 V for V_{SS} and solving for the number of RC time constants:

$$0.6\,\text{V} = 0.8\ \text{V}\left(1 - e^{\frac{t_{SS}}{90\,\text{k}\Omega\,(C_{SS})}}\right) \quad (60)$$

$$t_{SS} = 1.386\,RC_{SS} \quad (61)$$

Because R = 90 kΩ:

$$C_{SS} = t_{SS} \times 8\ \mu\text{F/sec} \quad (62)$$

where t_{SS} is the desired soft start time in seconds.

VOLTAGE TRACKING

The ADP1823 includes a tracking feature that prevents an output voltage from exceeding a master voltage. This is especially important when the ADP1823 is powering separate power supply voltages on a single integrated circuit, such as the core and I/O voltages of a DSP or microcontroller. In these cases, improper sequencing can cause damage to the load.

The ADP1823 tracking input is an additional positive input to the error amplifier. The feedback voltage is regulated to the lower of the 0.6 V reference or the voltage at TRK, so a lower voltage on TRK limits the output voltage. This feature allows implementation of two different types of tracking, coincident tracking where the output voltage is the same as the master voltage until the master voltage reaches regulation, or ratiometric tracking, where the output voltage is limited to a fraction of the master voltage.

In all tracking configurations, the master voltage should be higher than the slave voltage.

Note that the soft start time setting of the master voltage should be longer than the soft start of the slave voltage. This forces the rise time of the master voltage to be imposed on the slave voltage. If the soft start setting of the slave voltage is longer, the slave comes up more slowly and the tracking relationship is not seen at the output. The slave channel should still have a soft start capacitor to give a small but reasonable soft start time to protect in case of restart after a current-limit event.

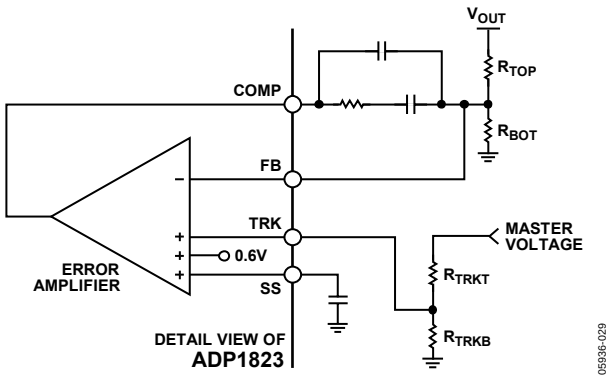


Figure 29. Voltage Tracking

COINCIDENT TRACKING

The most common application is coincident tracking, used in core vs. I/O voltage sequencing and similar applications. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the slave TRK input to a resistor divider from the master voltage that is the same as the divider used on the slave FB pin. This forces the slave voltage to be the same as the master voltage.

For coincident tracking, use $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$, where R_{TOP} and R_{BOT} are the values chosen in the Compensating the Voltage Mode Buck Regulator section.

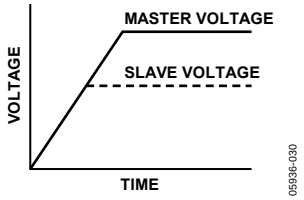


Figure 30. Coincident Tracking

As the master voltage rises, the slave voltage rises identically. Eventually, the slave voltage reaches its regulation voltage, where the internal reference takes over the regulation while the TRK input continues to increase and thus removes itself from influencing the output voltage.

To ensure that the output voltage accuracy is not compromised by the TRK pin being too close in voltage to the 0.6 V reference, make sure that the final value of the master voltage is greater than the slave regulation voltage by at least 10%, or 60 mV as seen at the FB node, and the higher, the better. A difference of 60 mV between TRK and the 0.6 V reference produces about 3 mV of offset in the error amplifier, or 0.5%, at room temperature, while 100 mV between them produces only 0.6 mV or 0.1% offset.

RATIOMETRIC TRACKING

Ratiometric tracking limits the output voltage to a fraction of the master voltage. For example, the termination voltage for DDR memories, VTT, is set to half the VDD voltage.

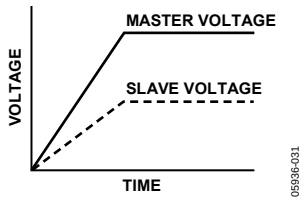


Figure 31. Ratiometric Tracking

For ratiometric tracking, the simplest configuration is to tie the TRK pin of the slave channel to the FB pin of the master channel. This has the advantage of having the fewest components, but the accuracy suffers as the TRK pin voltage becomes equal to the internal reference voltage and an offset is imposed on the error amplifier of about −18 mV at room temperature.

A more accurate solution is to provide a divider from the master voltage that sets the TRK pin voltage to be something lower than 0.6 V at regulation, for example, 0.5 V. The slave channel can be viewed as having a 0.5 V external reference supplied by the master voltage.

Once this is complete, then the FB divider for the slave voltage is designed as in the Compensating the Voltage Mode Buck Regulator section, except to substitute the 0.5 V reference for the V_{FB} voltage. The ratio of the slave output voltage to the master voltage is a function of the two dividers:

$$\frac{V_{OUT}}{V_{MASTER}} = \frac{\left(1 + \frac{R_{TOP}}{R_{BOT}}\right)}{\left(1 + \frac{R_{TRKT}}{R_{TRKB}}\right)} \quad (63)$$

Another option is to add another tap to the divider for the master voltage. Split the R_{BOT} resistor of the master voltage into two pieces, with the new tap at 0.5 V when the master voltage is in regulation. This saves one resistor, but be aware that Type III compensation on the master voltage causes the feedforward signal of the master voltage to appear at the TRK input of the slave channel.

By selecting the resistor values in the divider carefully, Equation 63 shows that the slave voltage output can be made to have a faster ramp rate than that of the master voltage by setting the TRK voltage at the slave larger than 0.6 V and R_{TRKB} greater than R_{TRKT}. Make sure that the master SS period is long enough (that is, sufficiently large SS capacitor) such that the input inrush current does not run into the current limit of the power supply during startup.

Setting the Channel 2 Undervoltage Threshold for Ratiometric Tracking

If FB2 is regulated to a voltage lower than 0.6 V by configuring TRK2 for ratiometric tracking, the Channel 2 undervoltage threshold can be set appropriately by splitting the top resistor in the voltage divider, as shown in Figure 32. R_{BOT} is the same as calculated for the compensation in Equation 63, and

$$R_{TOP} = R_A + R_B \quad (64)$$

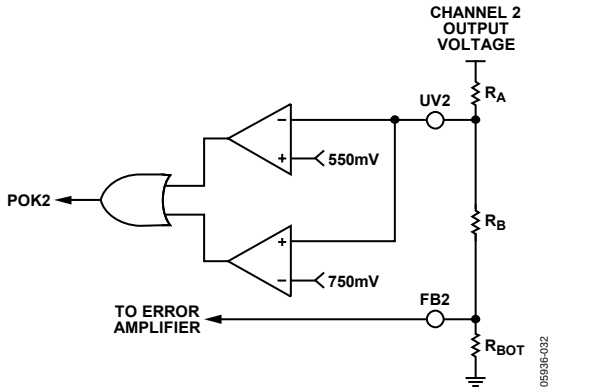


Figure 32. Setting the Channel 2 Undervoltage Threshold

The current in all the resistors is the same:

$$\frac{V_{FB2}}{R_{BOT}} = \frac{V_{UV2} - V_{FB2}}{R_B} = \frac{V_{OUT2} - V_{UV2}}{R_A} \quad (65)$$

where:
V_{UV2} is 600 mV.
V_{FB2} is the feedback voltage value set during the ratiometric tracking calculations.
V_{OUT2} is the Channel 2 output voltage.

Solving for R_A and R_B:

$$R_A = R_{BOT} \frac{\left(V_{OUTA2} - V_{UV2}\right)}{V_{FB2}} \quad (66)$$

$$R_B = R_{BOT} \frac{\left(V_{UV2} - V_{FB2}\right)}{V_{FB2}} \quad (67)$$

THERMAL CONSIDERATIONS

The current required to drive the external MOSFETs comprises the vast majority of the power dissipation of the ADP1823. The on-chip LDO regulates down to 5 V, and this 5 V supplies the drivers. Because the full gate drive current passes through the LDO and then is dissipated in the gate drive, effectively the full gate charge comes from the input voltage and dissipated on the ADP1823 is

$$P_D = V_{IN} f_{SW} (Q_{DH1} + Q_{DL1} + Q_{DH2} + Q_{DL2}) \quad (68)$$

where:
V_{IN} is the voltage applied to IN.
f_{SW} is the switching frequency.
Q numbers are the total gate charge specifications from the selected MOSFET data sheets.

The power dissipation heats the ADP1823. As the switching frequency, the input voltage, and the MOSFET size increase, the power dissipation on the ADP1823 increases. Care must be taken not to exceed the maximum junction temperature. To calculate the junction temperature from the ambient temperature and power dissipation:

$$T_J = T_A + P_D \theta_{JA} \quad (69)$$

The thermal resistance, θ_{JA}, of the package is typically 40°C/W depending on board layout, and the maximum specified junction temperature is 125°C, which means that at maximum ambient of 85°C without airflow, the maximum dissipation allowed is about 1 W.

A thermal shutdown protection circuit on the ADP1823 shuts off the LDO and the controllers if the die temperature exceeds approximately 145°C, but this is a gross fault protection only and should not be relied upon for system reliability.

PCB LAYOUT GUIDELINES

In any switching converter, some circuit paths carry high dI/dt, which can create spikes and noise. Other circuit paths are sensitive to noise. Still others carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for the ADP1823, arranged in approximately decreasing order of importance.

- The current waveform in the top and bottom FETs is a pulse with very high dI/dt, so the path to, through, and from each individual FET should be as short as possible and the two paths should be commoned as much as possible. In designs that use a pair of D-Pak or SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair and the high side drain can be bypassed to the low side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs in order to minimize inductance around this loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 µF to 22 µF depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor and should be grounded to the PGND plane.
- GND, PV bypass, VREG bypass, soft start capacitor, and the bottom end of the output feedback divider resistors should be tied to an (almost isolated) small AGND plane. All of these connections should have connections from the pin to the AGND plane that are as short as possible. No high current or high dI/dt signals should be connected to this AGND plane. The AGND area should be connected through one wide trace to the negative terminal of the output filter capacitors.
- The PGND pin handles high dI/dt gate drive current returning from the source of the low side MOSFET. The voltage at this pin also establishes the 0 V reference for the overcurrent limit protection (OCP) function and the CSL pin. A small PGND plane should connect the PGND pin and the PVCC bypass capacitor through a wide and direct path to the source of the low side MOSFET. The placement of C_{IN} is critical for controlling ground bounce. The negative terminal of C_{IN} needs to be placed very close to the source of the low-side MOSFET.
- Avoid long traces or large copper areas at the FB and CSL pins, which are low signal level inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as closely as possible to these pins. Avoid running these traces close and parallel to high dI/dt traces.
- The switch node is the noisiest place in the switcher circuit with large ac and dc voltage and current. This node should be wide to keep resistive voltage drop down. However, to minimize the generation of capacitively coupled noise, the total area should be small. Place the FETs and inductor all close together on a small copper plane in order to minimize series resistance and keep the copper area small.
- Gate drive traces (DH and DL) handle high dI/dt so tend to produce noise and ringing. They should be as short and direct as possible. If possible, avoid using feedthrough vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors (such as 5 Ω or 10 Ω) in series with the gate leads, mainly DH traces to the high side FET gates. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, and that also increases the switching power loss in the MOSFET.
- The negative terminal of output filter capacitors should be tied closely to the source of the low side FET. Doing this helps to minimize voltage difference between GND and PGND at the ADP1823.
- Generally, be sure that all traces are sized according to the current that will be handled as well as their sensitivity in the circuit. Standard PCB layout guidelines mainly address heating effects of current in a copper conductor. While these are completely valid, they do not fully cover other concerns such as stray inductance or dc voltage drop. Any dc voltage differential in connections between ADP1823 GND and the converter power output ground can cause a significant output voltage error, as it affects converter output voltage according to the ratio with the 600 mV feedback reference. For example, a 6 mV offset between ground on the ADP1823 and the converter power output will cause a 1% error in the converter output voltage.

LFCSP PACKAGE CONSIDERATIONS

The CSP package has an exposed die paddle on the bottom that efficiently conducts heat to the PCB. To achieve the optimum performance from the CSP package, give special consideration to the layout of the PCB. Use the following layout guidelines for the LFCSP package.

- The pad pattern is given in Figure 35. The pad dimension should be followed closely for reliable solder joints while maintaining reasonable clearances to prevent solder bridging.
- The thermal pad of the CSP package provides a low thermal impedance path to the PCB. Therefore, the PCB must be properly designed to effectively conduct the heat away from the package. This is achieved by adding thermal vias to the PCB, which provide a thermal path to the inner or bottom layers. See Figure 35 for the recommended via pattern. Note that the via diameter is small. This prevents the solder from flowing through the via and leaving voids in the thermal pad solder joint.

  Note that the thermal pad is attached to the die substrate, so the planes that the thermal pad is connected to must be electrically isolated or connected to GND.
- The solder mask opening should be about 120 microns (4.7 mils) larger than the pad size, resulting in a minimum 60 microns (2.4 mils) clearance between the pad and the solder mask.
- The paste mask opening is typically designed to match the pad size used on the peripheral pads of the LFCSP package. This should provide a reliable solder joint as long as the stencil thickness is about 0.125 mm.
- The paste mask for the thermal pad needs to be designed for the maximum coverage to effectively remove the heat from the package. However, due to the presence of thermal vias and the large size of the thermal pad, eliminating voids may not be possible. In addition, if the solder paste coverage is too large, solder joint defects may occur. Therefore, it is recommended to use multiple small openings over a single big opening in designing the paste mask. The recommended paste mask pattern is given in Figure 35. This pattern results in about 80% coverage, which should not degrade the thermal performance of the package significantly.
- The recommended paste mask stencil thickness is 0.125 mm. A laser cut stainless steel stencil with trapezoidal walls should be used.
- A no clean, Type 3 solder paste should be used for mounting the LFCSP package. In addition, a nitrogen purge during the reflow process is recommended.
- The package manufacturer recommends that the reflow temperature should not exceed 220°C and the time above liquid is less than 75 seconds. The preheat ramp should be 3°C/second or lower. The actual temperature profile depends on the board density; the assembly house must determine what works best.

Table 4. Compensation Equations

Equations	Calculations
$f_{CO} = \frac{f_{SW}}{10}$ (70)	
$f_{LC} = \frac{1}{2\pi\sqrt{LC}}$ (71)	
$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$ (72)	
$A_{FILTER} = -40\ \text{dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\ \text{dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right)$ (73)	
$A_{MOD} = 20 \log\left(\frac{V_{IN}}{V_{RAMP}}\right)$ (74)	
$\varphi_{ESR} = 45° \times \log\frac{10 \times f_{CO}}{f_{ESR}}$ (75)	
$\varphi_B = 150° - \varphi_{ESR}$ (76)	
If $\varphi_{ESR} \geq 70°$, use Type II compensation.	
If $\varphi_{ESR} < 70°$, use Type III compensation.	
Type II Compensation	**Calculations**
$K = \tan\left(\frac{\varphi_B}{2} + 45°\right)$ (77)	
$f_Z = \frac{f_{CO}}{K}$ (78)	
$f_P = f_{CO}K$ (79)	
Select R_{TOP} between 1 kΩ and 10 kΩ. A good starting value is 2 kΩ.	
$R_{BOT} = \frac{V_{FB}R_{TOP}}{V_{OUT} - V_{FB}}$ (80)	
$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER}$ (81)	
$R_Z = R_{TOP} \times 10^{\left(\frac{A_{COMP}}{20}\right)}$ (82)	
$C_I = \frac{1}{2\pi R_Z f_Z}$ (83)	
$C_{HF} = \frac{1}{2\pi R_Z f_P}$ (84)	

Type III Compensation	Calculations
$K = \left(\tan\left(\frac{\varphi_B}{2} + 45° \right) \right)^2$ (85)	
$f_Z = \frac{f_{CO}}{\sqrt{K}}$ (86)	
$f_P = f_{CO}\sqrt{K}$ (87)	
Select R_{TOP} between 1 kΩ and 10 kΩ. A good starting value is 2 kΩ.	
$R_{BOT} = \frac{0.6\ \text{V} \times R_{TOP}}{V_{OUT} - 0.6\ \text{V}}$ (88)	
$C_{FF} = \frac{1}{2\pi R_{TOP} f_Z}$ (89)	
$R_{FF} = \frac{1}{2\pi C_{FF} f_P}$ (90)	
$Z_{FF} = \frac{1}{2\pi C_{FF} f_{CO}} + R_{FF}$ (91)	
$A_{COMP} = 0\ \text{dB} - A_{MOD} - A_{FILTER}$ (92)	
$R_Z = \left(R_{TOP} \parallel Z_{FF}\right) \times 10^{\left(\frac{A_{COMP}}{20}\right)}$ (93)	
$C_I = \frac{1}{2\pi R_Z f_Z}$ (94)	
$C_{HF} = \frac{1}{2\pi R_Z f_P}$ (95)	

APPLICATION CIRCUITS

The ADP1823 controller can be configured to regulate outputs with loads of more than 20 A if the power components, such as the inductor, MOSFETs and the bulk capacitors, are chosen carefully to meet the power requirement. The maximum load and power dissipation are limited by the powertrain components. Figure 1 shows a typical application circuit that can drive an output load of 8 A.

Figure 33 shows an application circuit that can drive 20 A loads. Note that two low-side MOSFETs are needed to deliver the 20 A load. The bulk input and output capacitors used in this example are Sanyo's OSCON™ capacitors, which have low ESR and high current ripple rating. An alternative to the OSCON capacitors are the polymer aluminum capacitors that are available from other manufacturers such as United Chemi-con. Aluminum electrolytic capacitors, such as Rubycon's ZLG low-ESR series, can also be paralleled up at the input or output to meet the ripple current requirement. Since the aluminum electrolytic capacitors have higher ESR and much larger variation in capacitance over the operating temperature range, a larger bulk input and output capacitance is needed to reduce the effective ESR and suppress the current ripple. Figure 33 shows that the polymer aluminum or the aluminum electrolytic capacitors can be used at the outputs.

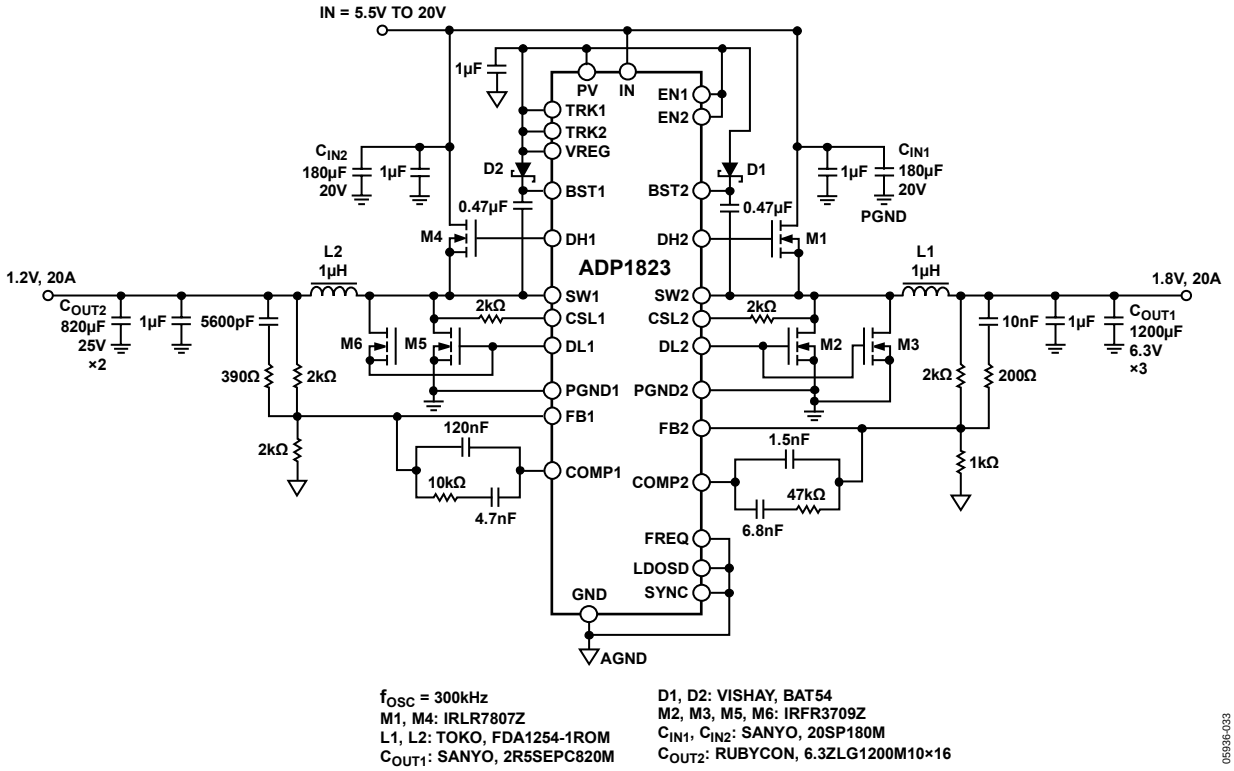


Figure 33. Application Circuit with 20 A Output Loads

The ADP1823 can also be configured to drive an output load of less than 1 A. Figure 34 shows a typical application circuit that drives a 1.5 A and a 3 A loads in an all multilayer ceramic capacitor (MLCC) solutions. Notice that the two MOSFETs used in this example are dual-channel MOSFETs in a PowerPAK® SO-8 package, which reduces cost and saves layout space. An alternative to using the dual-channel SO-8 package is using two single MOSFETs in SOT-23 or TSOP-6 packages, which are low cost and small in size. For input voltages less than 3.7 V, it is recommended to use MOSFETs that are fully turned on at V_{GS} less than 3 V. Because there is a forward voltage (V_F) drop across the Schottky diode D1 or D2, for input voltages less than 3.3 V, the effective voltage to the internal gate drivers may not be enough to drive a large load at the output. A Schottky diode with V_F less than 0.5 V at I_F of 100 mA is recommended for input voltages less than 3.3 V.

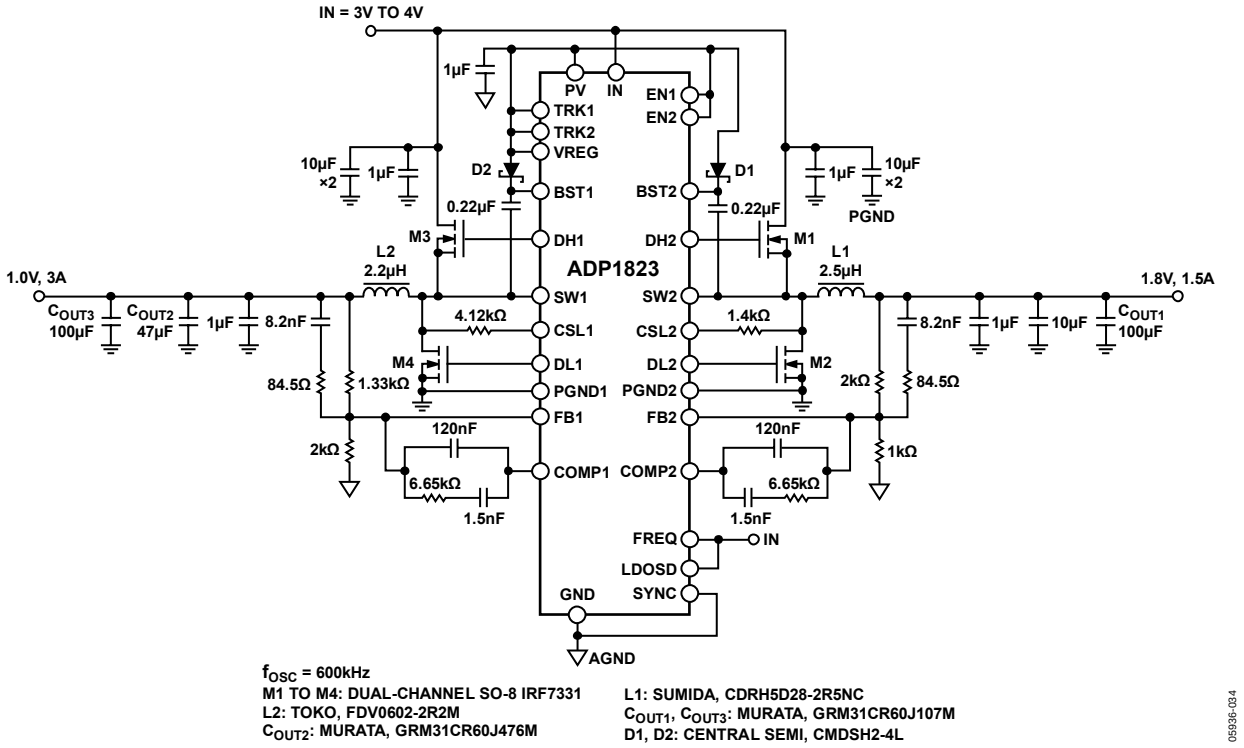
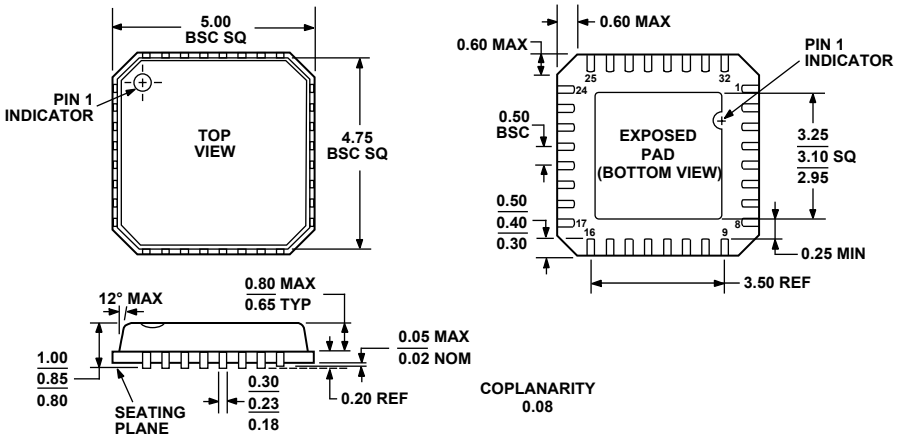


Figure 34. Application Circuit with all Multilayer Ceramic Capacitors (MLCC)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2

Figure 35. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP1823ACPZ-R7[1]	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
ADP1823-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

D05936-0-11/06(A)