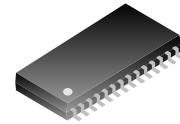


THREE-PHASE HALFBRIDGE GATE DRIVER

DESCRIPTION

The SDH2136U is a high voltage, high speed gate driver IC, with three independent high side and low side output channels for 3-phase applications. Built-in dead time avoids the cross conduction of both high side and low side power devices, such as N-Channel MOSFETs and IGBTs. Built-in input filter avoids input noise interference. External enable control is available to terminate all six channel outputs simultaneously. Meanwhile, it integrates under-voltage protection and over-current protection functionality, which terminates channels output when under voltage or over current occurs.



SOP-28-375-1.27

FEATURES

- ◆ High-side floating supply offset voltage: 600V
- ◆ Output current: +0.35A / -0.70A
- ◆ 3.3V / 5V input logic compatible
- ◆ Dead time control
- ◆ Undervoltage lockout (UVLO) for VCC&VBS
- ◆ Overcurrent protection turns off all channels
- ◆ Enable control
- ◆ Outputs out of phase with inputs
- ◆ Three independent half bridge drivers
- ◆ dV/dt immune

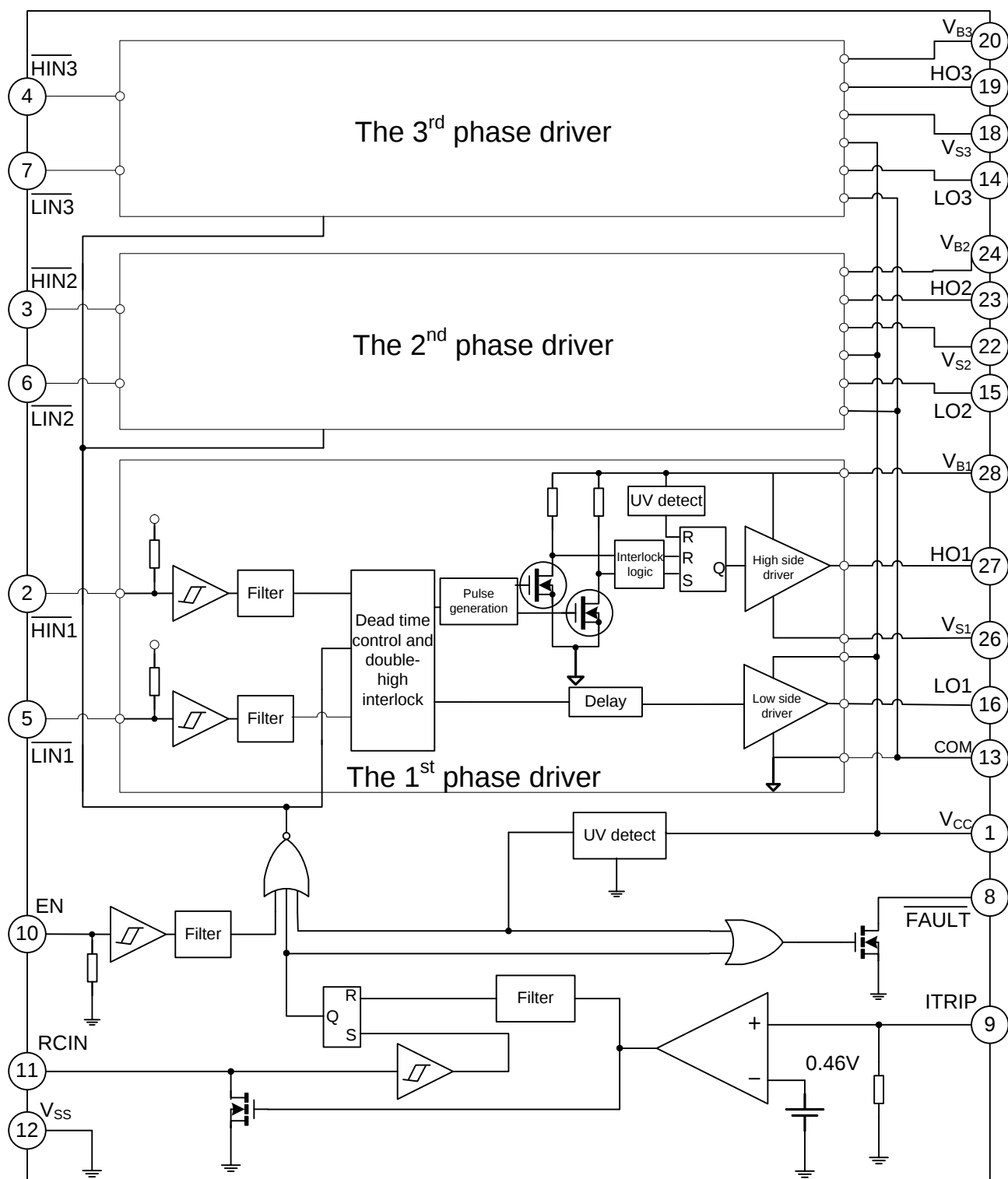
APPLICATIONS

- ◆ 3-phase motor driver
- ◆ SMPS
- ◆ Air Conditioner, Refrigerator, Washing Machine

ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing Type
SDH2136U	SOP-28-375-1.27	SDH2136U	Halogen free	Tube
SDH2136UTR	SOP-28-375-1.27	SDH2136U	Halogen free	Tape&Reel

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE SPECIFIED, $T_{amb}=25^{\circ}\text{C}$,)

Characteristics	Symbol	Ratings	Unit
High Side Floating Supply Absolute Voltage	V_B	-0.3~625	V
High Side Floating Supply Offset Voltage	V_S	$V_{B1,2,3}-25-V_{B1,2,3}+0.3$	V
High Side Output Voltage	V_{HO}	$V_{S1,2,3}-0.3-V_{B1,2,3}+0.3$	V
Low Side and Fixed Supply Voltage	V_{CC}	-0.3~25	V
Powerground	COM	$V_{CC}-25-V_{CC}+0.3$	V
Low Side Output Voltage	V_{LO}	COM-0.3~ $V_{CC}+0.3$	V
Logic Input Voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, EN)	V_{IN}	$V_{SS}-0.3 \sim V_{SS}+5.5$	V
RCIN input voltage	V_{RCIN}	$V_{SS}-0.3-V_{CC}+0.3$	V
FAULT output voltage	V_{FAULT}	$V_{SS}-0.3-V_{CC}+0.3$	V
Allowable offset voltage slew-rate	dV/dt	≤ 50	V/ns
Package Power Dissipation@ $T_A \leq 25^{\circ}\text{C}$	P_D	≤ 1.6	W
Thermal resistance, junction to ambient	R_{thJA}	≤ 78	$^{\circ}\text{C/W}$
Junction Temperature Range	T_j	≤ 150	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-55~150	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
High Side Floating Supply Absolute Voltage	V_B	--	$V_{S1,2,3}+10$	--	$V_{S1,2,3}+20$	V
High Side Floating Supply Offset Voltage	V_S	--	-5	--	600	V
High Side Output Voltage	V_{HO}	--	$V_{S1,2,3}$	--	$V_{B1,2,3}$	V
Low Side and logic fixed Supply Voltage	V_{CC}	--	10	--	20	V
Powerground	COM	--	-5	--	5	V
Low Side Output Voltage	V_{LO}	--	COM	--	V_{CC}	V
Logic Input Voltage ($\overline{HIN}$, $\overline{LIN}$, ITRIP, EN)	V_{IN}	--	V_{SS}	--	$V_{SS}+5$	V
RCIN input voltage	V_{RCIN}	--	V_{SS}	--	V_{CC}	V
FAULT output voltage	V_{FAULT}	--	V_{SS}	--	V_{CC}	V
Ambient temperature	T_A	--	-40	--	125	$^{\circ}\text{C}$

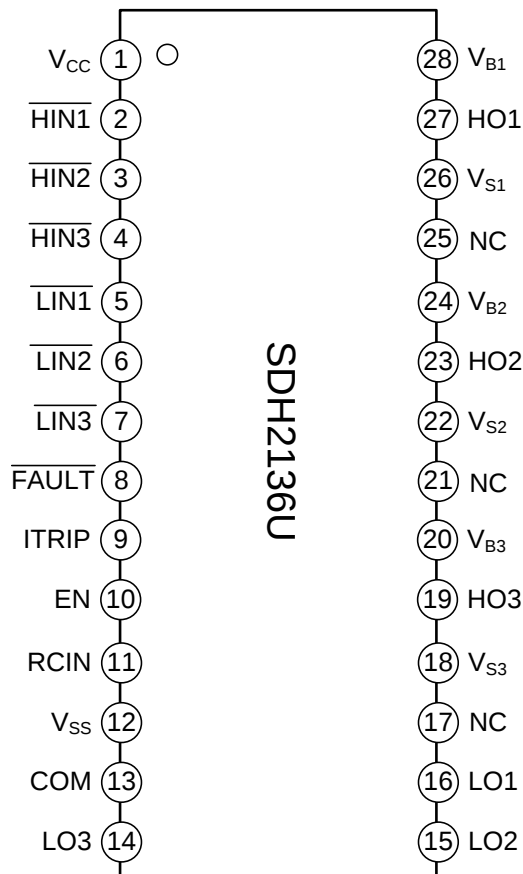
Note: all input pins ($\overline{HIN}$, $\overline{LIN}$, ITRIP, EN) integrate the 6.0V clamp diode.

ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE SPECIFIED, $T_{amb}=25^{\circ}\text{C}$, $V_{CC}=V_{BS1,2,3}=15\text{V}$, $V_{SS}=0\text{V}$)

Characteristics	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
High Level Input Threshold Voltage	V_{IH}		2.6	--	--	V
Low Level Input Threshold Voltage	V_{IL}		--	--	0.8	V
EN positive going threshold	$V_{EN,TH+}$		--	--	2.6	V
EN negative going threshold	$V_{EN,TH-}$		0.8	--	--	V
ITRIP positive going threshold	$V_{IT,TH+}$		0.37	0.46	0.55	V
ITRIP input hysteresis	$V_{IT,HYS}$		--	0.07	--	V
RCIN positive going threshold	$V_{RCIN,TH+}$		--	8	--	V
RCIN input hysteresis	$V_{RCIN,HYS+}$		--	3	--	V
VCC/VBS supply undervoltage positive going threshold	V_{CCUV+} V_{BSUV+}		7.9	8.9	9.9	V
VCC/VBS supply undervoltage negative going threshold	V_{CCUV-} V_{BSUV-}		7.2	8.2	9.2	V
VCC/VBS supply undervoltage lockout hysteresis	V_{CCUVH} V_{BSUVH}		0.3	0.7	--	V
Offset Supply Leakage Current	I_{LK}	$V_{B1,2,3}=V_{S1,2,3}=600\text{V}$	--	--	50.0	μA
Quiescent V_{BS} Supply Current	I_{QBS}	$V_{IN}=0\text{V}$ or 5V	--	70	120	μA
Quiescent Vcc Supply Current	I_{QCC}	$V_{IN}=0\text{V}$ or 5V	--	1.6	2.3	mA
Input Clamp Voltage ($\overline{HIN}$, $\overline{LIN}$, EN, ITRIP)	$V_{IN,CLAMP}$	$I_{IN}=100\mu\text{A}$	5.5	6.0	6.5	V
$\overline{LIN}$ high Level Input Bias Current	I_{LIN+}	$V_{LIN}=5\text{V}$	--	100	200	μA
$\overline{LIN}$ low Level Input Bias Current	I_{LIN-}	$V_{LIN}=0\text{V}$	--	150	300	μA
$\overline{HIN}$ high Level Input Bias Current	I_{HIN+}	$V_{HIN}=5\text{V}$	--	100	200	μA
$\overline{HIN}$ low Level Input Bias Current	I_{HIN-}	$V_{HIN}=0\text{V}$	--	150	300	μA
High ITRIP Input Bias Current	I_{ITRIP+}	$V_{ITRIP}=5\text{V}$	--	5	10	μA
Low ITRIP Input Bias Current	I_{ITRIP-}	$V_{ITRIP}=0\text{V}$	--	--	1	μA
High EN Input Bias Current	I_{EN+}	$V_{EN}=5\text{V}$	--	5	10	μA
Low EN Input Bias Current	I_{EN-}	$V_{EN}=0\text{V}$	--	--	1	μA
RCIN Input Bias Current	I_{RCIN}	$V_{RCIN}=0\text{V}$ or 15V	--	--	1	μA
High Output Voltage	V_{OH}	$I_O=20\text{mA}$	13.8	14.5	--	V
Low Output Voltage	V_{OL}	$I_O=20\text{mA}$	--	0.2	0.5	V
Output High Short Circuit Pulsed Current	I_{OH}	$V_O=15\text{V}$, $V_{IN}=0\text{V}$, $PW\leq 10\mu\text{s}$	0.18	0.35	--	A
Output Low Short Circuit Pulsed Current	I_{OL}	$V_O=0\text{V}$, $V_{IN}=5\text{V}$, $PW\leq 10\mu\text{s}$	0.30	0.70	--	A
RCIN low on resistance	R_{ON_RCIN}		--	50	100	Ω
FAULT low on resistance	R_{ON_FAULT}		--	50	100	Ω
Turn-On propagation delay	t_{on}	$C_L=1000\text{pF}$	300	425	550	ns

Characteristics	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Turn-Off propagation delay	t_{off}	$C_L=1000pF$	250	400	550	ns
Turn-On Rise Time	t_r	$C_L=1000pF$	--	60	120	ns
Turn-Off Fall Time	t_f	$C_L=1000pF$	--	40	90	ns
EN Turn-Off delay	t_{EN}	$V_{IN}, V_{EN}=0V$ or 5V	300	450	600	ns
ITRIP to output shutdown propagation delay	t_{ITRIP}	$V_{ITRIP}=5V$	500	750	1000	ns
ITRIP blanking time	t_{bl}	$V_{IN}=0V$ or 5V, $V_{ITRIP}=5V$	150	350	--	ns
ITRIP to $\overline{FAULT}$ propagation delay	t_{FLT}	$V_{IN}=0V$ or 5V, $V_{ITRIP}=5V$	400	600	800	ns
Input filter time	t_{FILIN}	$V_{IN}=0V$ or 5V	100	260	--	ns
$\overline{FAULT}$ clear time	t_{FLTCLR}	$R1=2M\Omega$, $C2=1nF$	1.3	1.65	2	ms
Dead time	DT	$V_{IN}=0V$ or 5V	200	290	380	ns
Matching delay ON and OFF	MT		--	40	75	ns
Dead time matching	MDT		--	25	70	ns
Output pulse width matching	PM	$PW_{IN}>1\mu s$	--	40	75	ns

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Description
1	V _{CC}	I	Low side and logic fixed Supply
2,3,4	$\overline{\text{HIN}}_{1,2,3}$	I	Logic inputs for high side gate driver outputs, negative logic
5,6,7	$\overline{\text{LIN}}_{1,2,3}$	I	Logic inputs for low side gate driver outputs, negative logic
8	$\overline{\text{FAULT}}$	O	Indicates overcurrent or undervoltage lockout has occurred, negative logic
9	ITRIP	I	Overcurrent protection input pin
10	EN	I	Enable pin
11	RCIN	I	Connected to RC, defining FAULT clear delay
12	V _{SS}	I	Logic ground
13	COM	I	Low side gate drive return
14,15,16	LO _{3,2,1}	O	Low side gate driver outputs
18,22,26	V _{S3,2,1}	I	High side floating supply return
19,23,27	HO _{3,2,1}	O	High side gate driver outputs
20,24,28	V _{B3,2,1}	I	High side floating supply
17,21,25	NC	--	NC

FUNCTION DESCRIPTION

The SDH2136U is a high voltage, high speed gate driver IC, with three independent high side and low side output channels for 3-phase applications. In normal operation, outputs out of phase with $\overline{\text{LIN}}$ and $\overline{\text{HIN}}$ inputs.

SDH2136U features undervoltage (UV) lockout, when V_{CC} is lower than the undervoltage protection negative threshold, LO and HO of all channels are shutdown when V_{BS} is lower than undervoltage protection negative threshold, high side outputs low and low side channels work normally. This function is used to prevent MOSFETs or IGBTs working under high voltage & high current, then prevent follow-stage devices operating in low efficiency.

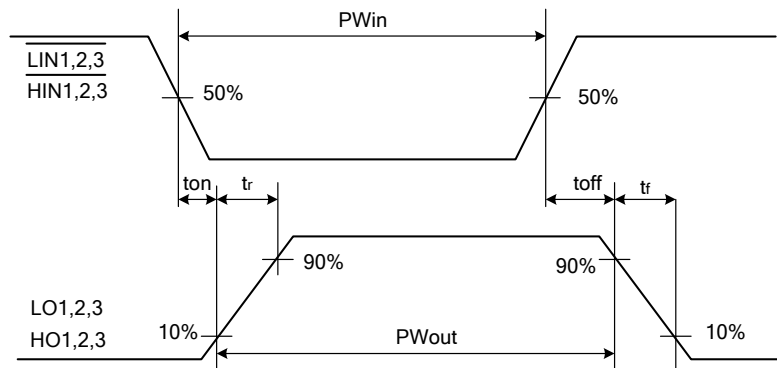
SDH2136U integrates input filter avoiding input noise interference.

SDH2136U builds-in dead time ,avoiding the MOSFETs and IGBTs damaged by cross conduction.

SDH2136U integrates overcurrent protection with open-drain fault (under-voltage, over-current) signal output, and six channels can be shutdown simultaneously when over current occurs.

SDH2136U integrates enable functionality and six channels can be shutdown simultaneously.

TIMING REQUIREMENT



Static logic table

V_{CC}	V_{BS}	ITRIP	ENABLE^*	$\overline{\text{FAULT}}$	LO1,2,3	HO1,2,3
$< V_{\text{CCUV-}}$	X	X	X	0 (note 1)	0	0
15V	$< V_{\text{BSUV-}}$	0V	5V	High impedance	$\overline{\text{LIN1,2,3}}$	0
15V	15V	0V	5V	High impedance	$\overline{\text{LIN1,2,3}}$ (note 2)	$\overline{\text{HIN1,2,3}}$
15V	15V	$> V_{\text{IT,TH+}}$	5V	0(note 3)	0	0
15V	15V	0V	0V	High impedance	0	0

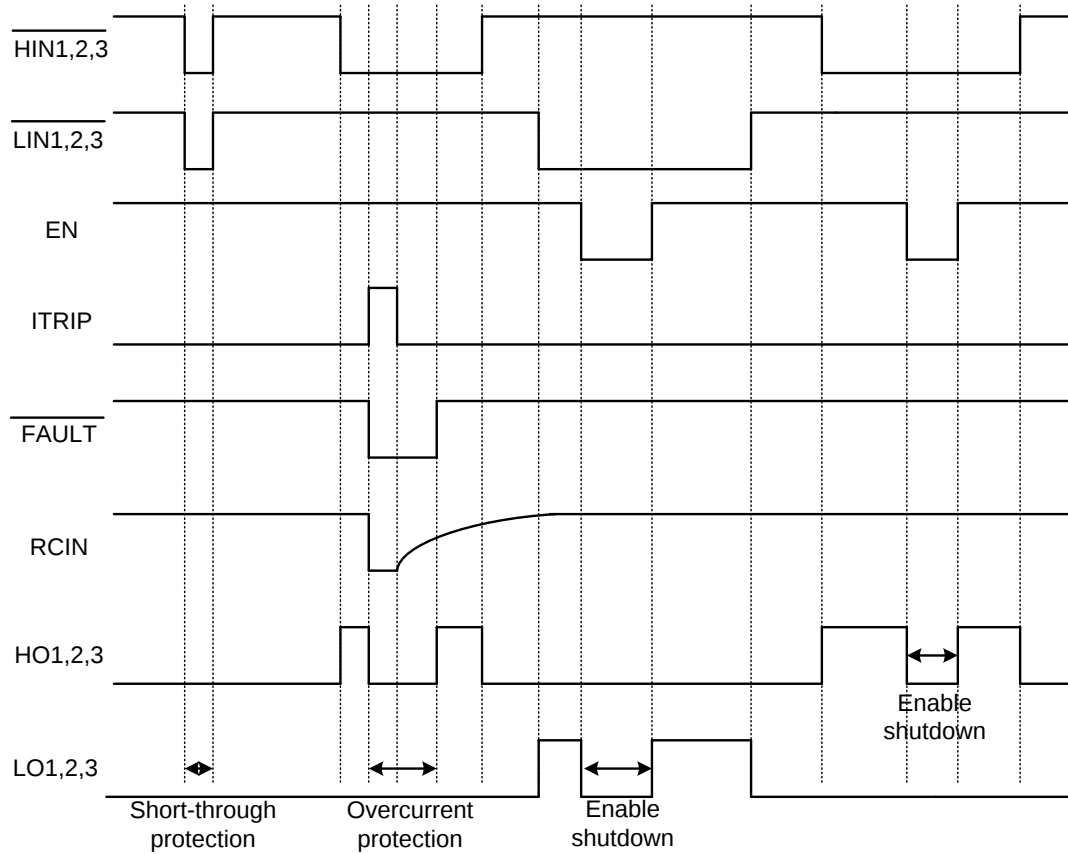
Note 1: when $V_{\text{CC}} > V_{\text{CCUV-}}$, $V_{\text{CCUV-}}$ will not be latched and $\overline{\text{FAULT}}$ is high impedance.

Note 2: short-through protection is used for preventing simultaneously conduction of LO1,2,3 and HO1,2,3 ;

Note 3: when $\text{ITRIP} < V_{\text{IT,TH+}}$, RCIN voltage $> 8\text{V}$ ($@V_{\text{CC}}=15\text{V}$), $\overline{\text{FAULT}}$ is high impedance.

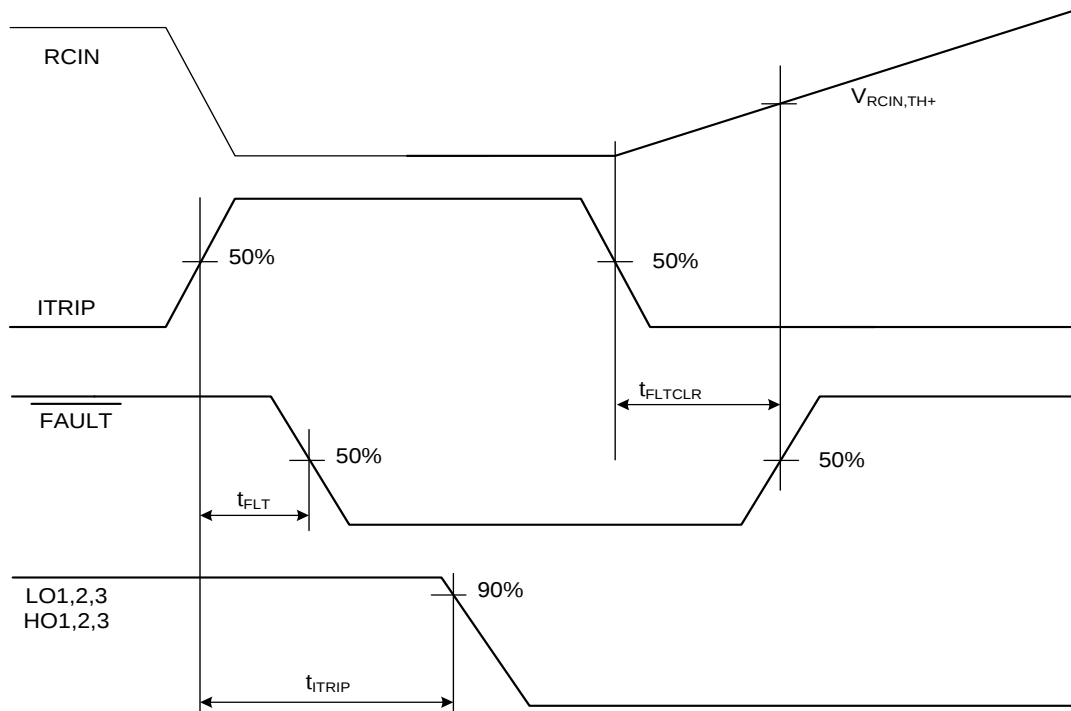
LOGIC TIMING DIAGRAM

1. Input/output timing diagram



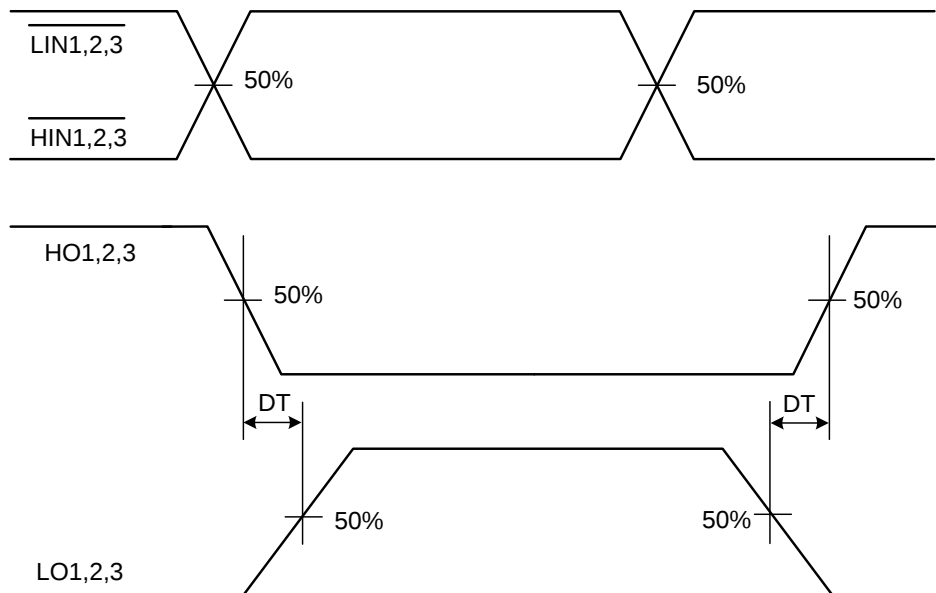
Input/output timing diagram

2. Overcurrent timing diagram



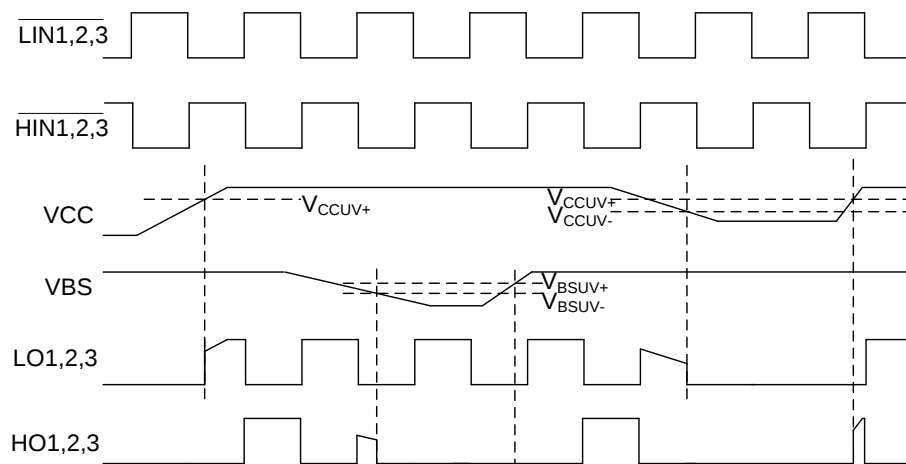
Overcurrent timing diagram

3. Deadtime timing diagram



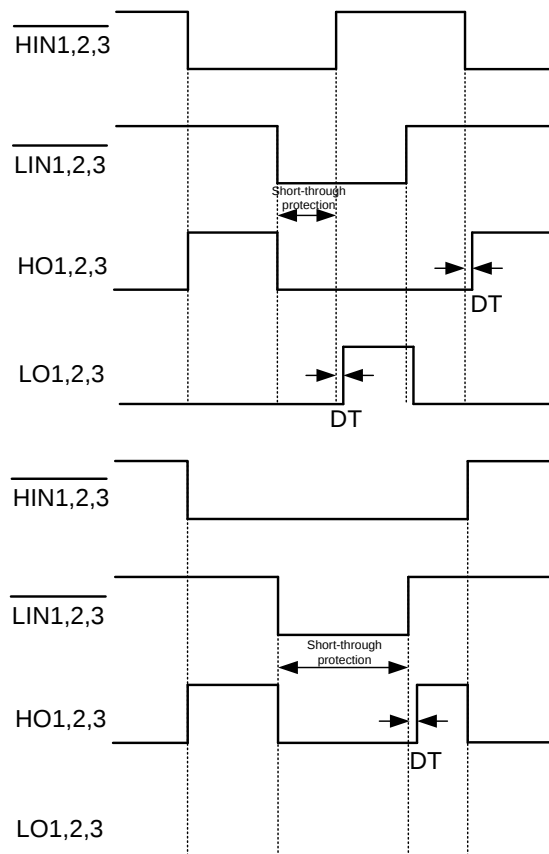
Deadtime timing diagram

4. UVLO functionality



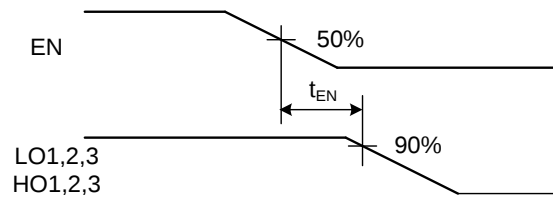
UVLO protection timing diagram

5. Short-circuit protection timing diagram



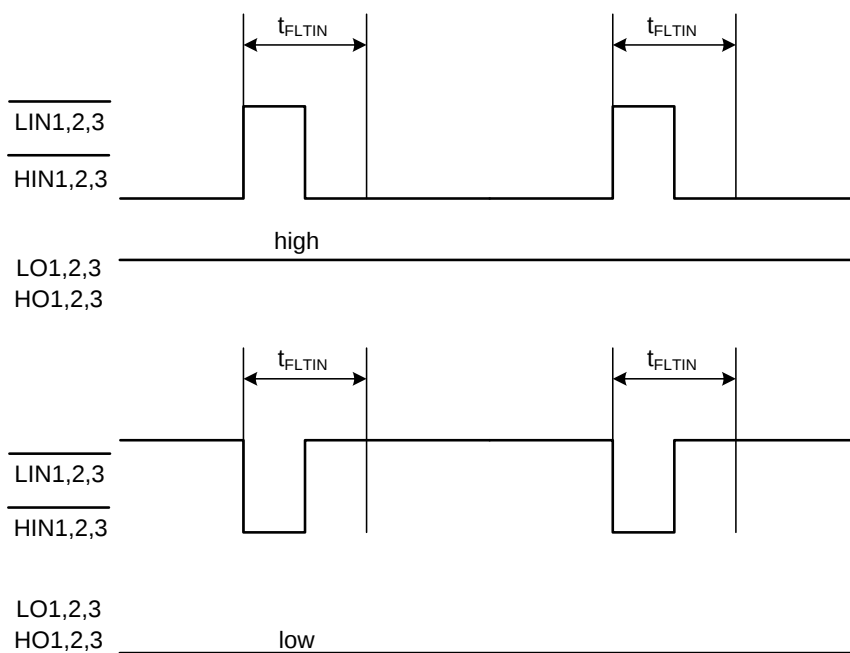
Short-circuit protection timing diagram

6. Enable shutdown timing diagram



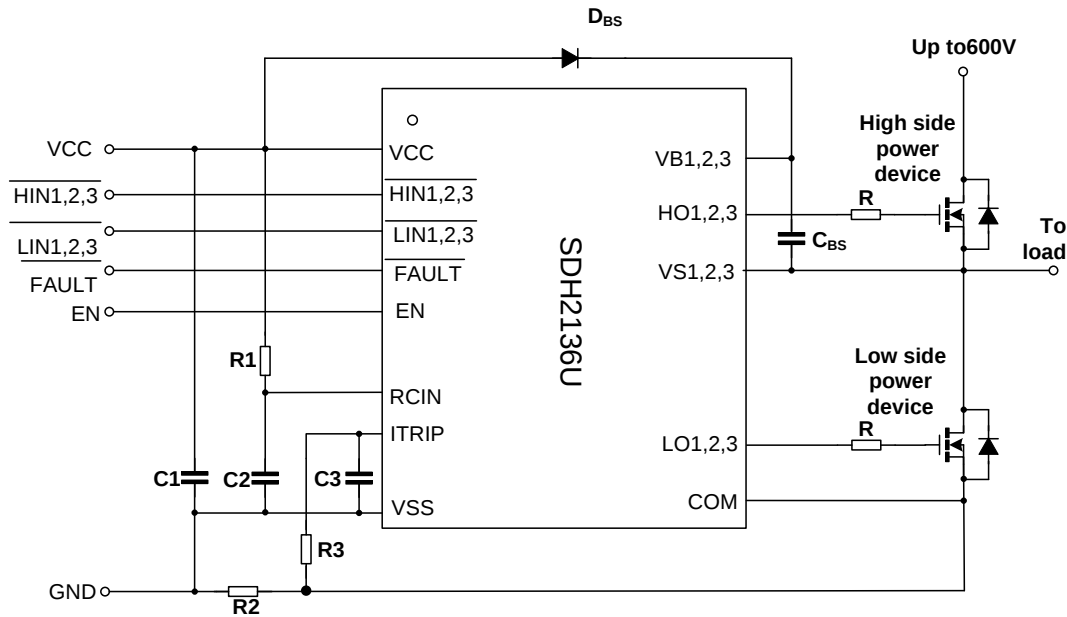
Enable shutdown timing diagram

7. Input noise filter timing diagram



Input noise filter timing diagram

TYPICAL APPLICATION CIRCUIT



C1: Power supply capacitor, selectable range: 0.1μF~1μF.

R: Gate protection resistor, with resistance determined by the device to be drove.

R1: overcurrent protection clear time set resistor, 2MΩ is recommended.

C2: overcurrent protection clear time set capacitor, 1nF is recommended.

R3: overcurrent protection filtering resistor, 1KΩ is recommended.

C3: overcurrent protection filter capacitor, 1nF is recommended.

R2: overcurrent threshold value set resistor, decided by practical application.

DBS: Bootstrap diode, a diode with high reverse breakdown voltage (>600V) is recommended, meanwhile its recovery time should be as short as possible.

CBS: Bootstrap capacitor, a ceramic capacitor or tantalum capacitor is recommended, and the min. capacitance is given by:

$$C_{bs} \geq \frac{2 \cdot [2 \cdot Q_g + Q_{period} + \frac{I_{bs(staic)}}{f} + \frac{I_{bs(leak)}}{f}]}{V_{CC} - V_F - V_{ds(L)} - V_{BSmin}}$$

Where: Q_g is the gate charge of the high side power device;

Q_{period} is the required charge per cycle in level shift circuit, approximately 5nC;

$I_{bs(static)}$ is the quiescent current for the high side driver circuitry;

$I_{bs(leak)}$ is the leakage current of bootstrap capacitor;

f is the operating frequency;

V_{CC} is the charge voltage of the bootstrap capacitor(the low side fixed supply voltage);

V_F is the forward voltage drop across the bootstrap diode;

$V_{ds(L)}$ is the voltage drop across the low side power device.

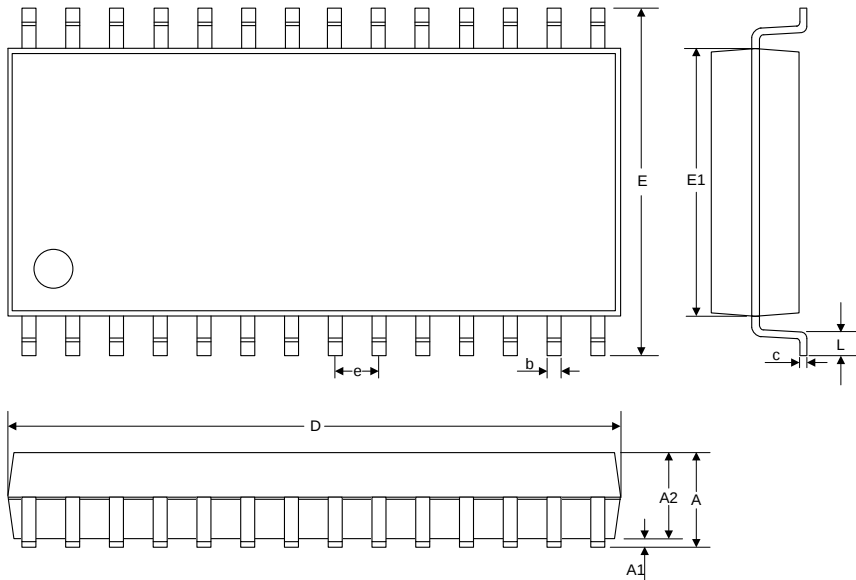
V_{BSmin} is the minimum V_{BS} voltage determined by application.

Note: The circuit and parameters are for reference only, please set the parameters of application circuits based on real tests.

PACKAGE OUTLINE

SOP-28-375-1.27

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.80
A1	0.10	0.20	0.30
A2	2.25	2.45	2.65
b	0.39	—	0.54
c	0.15	—	0.29
D	17.40	—	18.10
E	10.10	—	10.60
E1	7.40	—	7.70
e	1.27 BSC		
L	0.40	—	1.00

Important notice :

- The instructions are subject to change without notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
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Rev.: 1.0

Revision History:

1. First release
